Quad Parametric Measurement Unit With Integrated 16-Bit Level Setting DACs

Preliminary Technical Data

AD5522

FEATURES

Quad Parametric Measurement Unit
FV, FI, FN, MV, MI Functions
4 Programmable Current Ranges (Internal R_{SENSE})
5uA, 20uA, 200uA and 2mA
1 Programmable Current Range up to 64mA (external R_{SENSE})
22.5 V FV Range with Asymmetrical Operation
Integrated 16-Bit DACs Provide Programmable Levels
Offset and Gain Correction on Chip
Low Capacitance Outputs Suited to Relay Less Systems
On-chip Comparators Per Channel
FI Voltage Clamps & FV Current Clamps
Guard Drive Amplifier
System PMU connections
Programmable Temperature Shutdown Feature
SPI/Microwire/DSP & LVDS Compatible Interfaces
Compact 80 lead TQFP Package with Exposed Pad (Top Or Bottom)

APPLICATIONS

Automatic Test Equipment (ATE)
per pin Parametric Measurement Unit
Continuity & Leakage Testing
Device Power Supply
Instrumentation
SMU (Source Measure Unit)
Precision Measurement

PRODUCT OVERVIEW

The AD5522 is a high performance, highly integrated parametric measurement unit consisting of four independent channels. Each PPMU channel includes five, 16-bit, voltage out DACs setting the programmable inputs levels for the force voltage input, clamp and comparator inputs (high and low). Five programmable force and measure current ranges are available ranging from 5µA to 64mA. Four of these ranges use on chip sense resistors, while a high current range up to 64mA is available per channel using off chip sense resistors. Currents in excess of 64mA require an external amplifier. Low capacitance DUT connections (FOH, EXT FOH) ensure the device is suited to relay less test systems.

The PMU functions are controlled via a simple three wire serial interface compatible with SPI/QSPI/Microwire and DSP interface standards. Interface clocks of 50MHz allow fast updating of modes. LVDS (Low Voltage Differential Signaling) interface protocol at 100MHz is also supported. Comparator outputs are provided per channel for device go no-go testing and characterization. Control registers provide easy way of changing force or measure conditions, DAC levels and selected current ranges. SDO (serial data out) allows the user to readback information for diagnostic purposes.

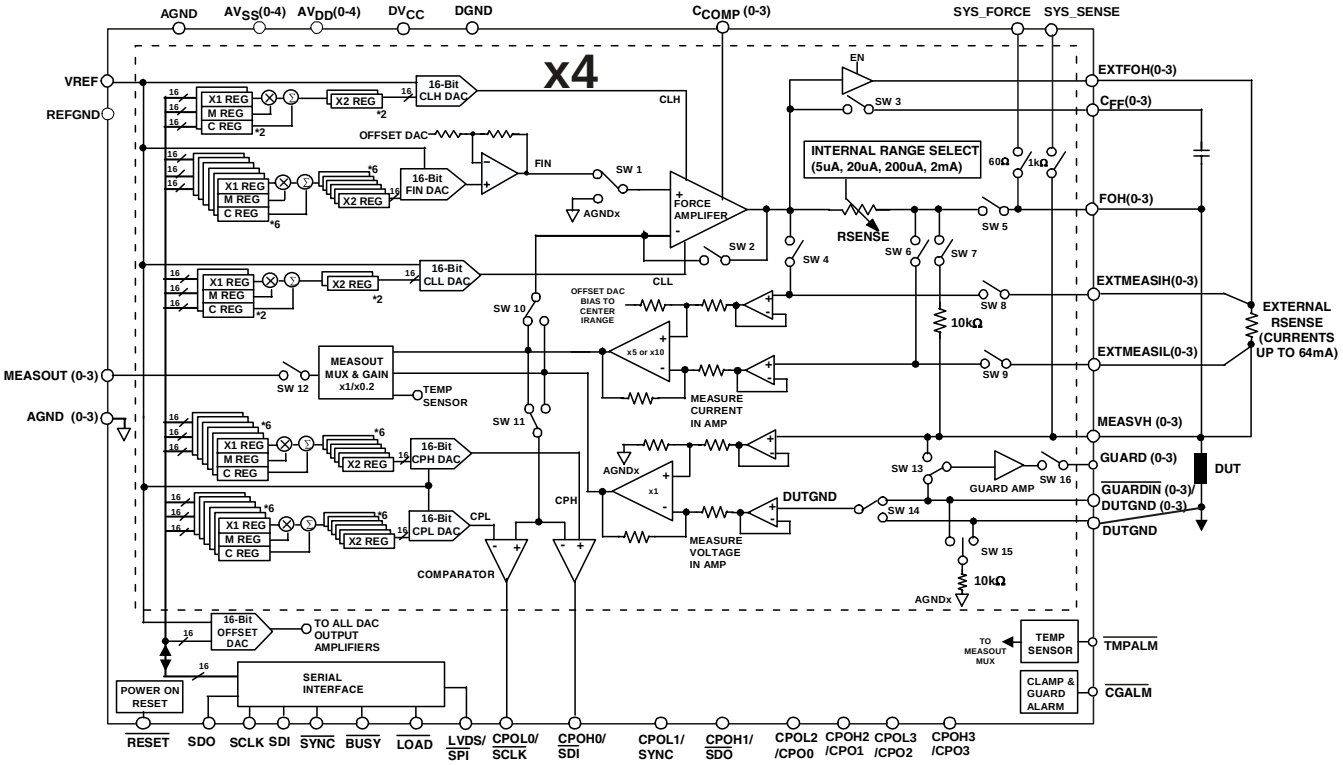

Figure 1. Functional Block Diagram

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REVISION HISTORY

5th Sept, Update to block diagram, timing and READ functions. .

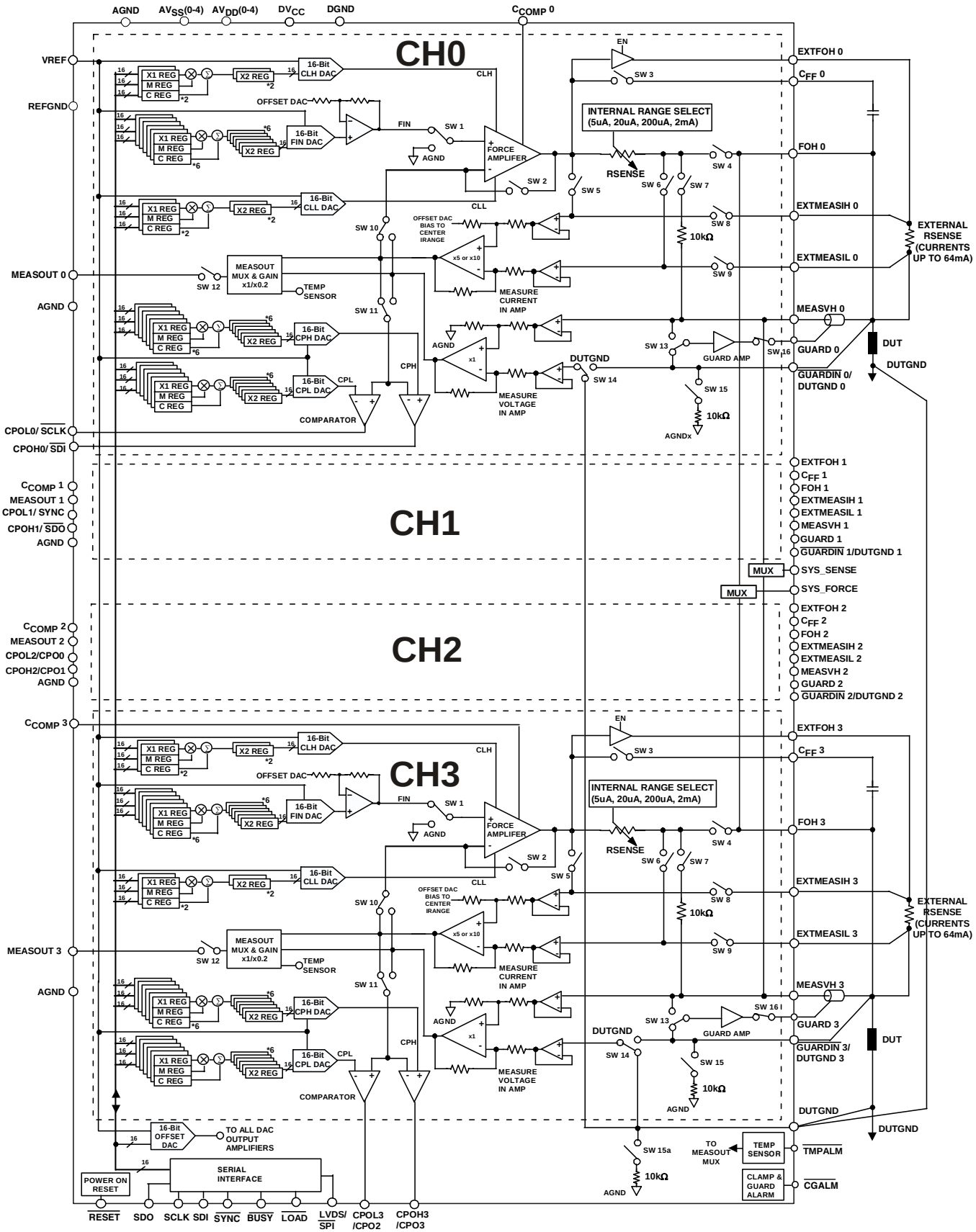


Figure 2. Detailed Block Diagram

SPECIFICATIONS

Table 1. $AV_{DD} \geq 10V$, $AV_{SS} \leq -5V$, $|AV_{DD} - AV_{SS}| \geq 20V$ and $\leq 33V$, $DV_{CC} = 2.3V$ to $5.25V$, $V_{REF}=5V$, Gain (m), Offset (c) and DAC Offset registers at default values ($T_J = +25$ to $+90°C$, max specs unless otherwise noted.)

Parameter	Min	Typ[1]	Max	Units	Test Conditions/Comments
FORCE VOLTAGE					
FOH Output Voltage Range	$AV_{SS}+4$		$AV_{DD}-4$	V	All current ranges from FOH at full scale current. Includes ±1V dropped across sense resistor
EXTFOH Output Voltage Range	$AV_{SS}+3$		$AV_{DD}-3$	V	External high current range at full scale current. Does not include ±1V dropped across sense resistor
Output Voltage Span			22.5	V	
Offset Error	-100		100	mV	
Offset Error Tempco[2]		±100		µV/°C	
Gain Error	-0.5		0.5	%	
Gain Error Tempco[2]		±10		ppm/°C	
Linearity Error	-0.02		0.02	% FSR	FSR = Fullscale Range. ±10 V range, Gain and offset errors calibrated out.
Short Circuit Current Limit[2]	-120		120	mA	On 64mA range.
	-10		10	mA	In all other ranges.
MEASURE CURRENT					MEASURE = (IDUT X RSENSE x GAIN)
Offset Error	-1		1	%	V(Rsense)= ±1V
Offset Error Tempco[2]		±10		µV/°C	
Gain Error	-1		1	%	Instrumentation Amp Gain = 5 or 10
Gain Error Tempco[2]		25		ppm/°C	
Linearity Error	-0.01		0.01	% FSCR	Offset and Gain errors calibrated out
Output Voltage Span[2]			22.5	V	
CM Error	-0.005		0.005	%FSCR/V	% of FS Change at measure output per V change in DUT voltage
Measure Current Ranges		±5		µA	Set using internal sense resistor
		±20		µA	Set using internal sense resistor
		±200		µA	Set using internal sense resistor
		±2		mA	Set using internal sense resistor
			Up to ±64	mA	Set using external sense resistor, internal amplifier can drive to 64mA
FORCE CURRENT					
Voltage Compliance, FOH	$AV_{SS}+4$		$AV_{DD}-4$	V	
Voltage Compliance, EXTFOH	$AV_{SS}+3$		$AV_{DD}-3$	V	
Offset Error	-2		2	%FSCR	
Offset Error Tempco[2]		±10		ppm FS/°C	
Gain Error	-0.5		0.5	%	Gain = 1
Gain Error Tempco[2]		±25		ppm/°C	
Linearity Error	-0.02		0.02	% FSCR	
CM Error	-0.005		0.005	%FSCR/V	% of FS Change at measure output per V change in DUT voltage
Force Current Ranges		±5		µA	Set using internal sense resistor, 200kΩ
		±20		µA	Set using internal sense resistor, 50kΩ
		±200		µA	Set using internal sense resistor, 5kΩ
		±2		mA	Set using internal sense resistor, 500Ω
			Up to ±64	mA	Set using external sense resistor, internal amplifier can drive to 64mA
MEASURE VOLTAGE					
Measure Voltage Range			$AV_{DD}-4$	V	
	$AV_{SS}+4$			V	
Offset Error	-10		10	mV	
Offset Error Tempco[2]		±10		µV/°C	
Gain Error	-0.5		0.5	% FSR	Gain = 1
Gain Error Tempco[2]		±10		ppm/°C	
Linearity Error	-0.01		0.01	% FSR	

Parameter	Min	Typ[1]	Max	Units	Test Conditions/Comments
COMPARATOR					
Comparator Span			22.5	V	
Offset Error	-10		10	mV	
Propagation delay[2]		1	TBD	µs	
VOLTAGE CLAMPS					
Clamp Span			22.5	V	
Positive Clamp Accuracy			150	mV	
Negative Clamp Accuracy	-150			mV	
Recovery Time[2]		TBD	TBD	µs	
Activation Time[2]		TBD	TBD	µs	
CURRENT CLAMPS					
Clamp Accuracy	Prog'd Clamp value		Programmed Clamp value +15	% of FSC range	Clamp current scales with selected range
Recovery Time[2]		TBD	TBD	µs	
Activation Time[2]		TBD	TBD	µs	
FOH, EXTFOH, EXTMEASIL, EXTMEASIH, CFF					
Pin Capacitance[2]		3	TBD	pF	
Leakage Current	-3		3	nA	On or off switch leakage
Leakage Current Tempco[2]		±0.1		nA/°C	
MEASVH					
Pin Capacitance[2]		3	TBD	pF	
Leakage/Bias Current	-3		3	nA	
Leakage Current Tempco[2]		±0.1		nA/°C	
SYS_SENSE					SYS_Sense Connected, Force Amplifier Inhibited
Pin Capacitance[2]		3	TBD	pF	
SYS_SENSE Impedance		1	1.3	kΩ	
Leakage Current	-3		3	nA	
Leakage Current Tempco[2]		±0.1		nA/°C	
SYS_FORCE					SYS_Force Connected, Force Amplifier Inhibited
Pin Capacitance[2]		3	TBD	pF	
SYS_FORCE Impedance		60	80	Ω	
Leakage Current	-3		3	nA	
Leakage Current Tempco[2]		±0.1		nA/°C	
COMBINED LEAKAGE at DUT					Includes FOH, MEASVH, SYS_SENSE, SYS_FORCE, EXTMEASIL
Leakage Current	-15		15	nA	
Leakage Current Tempco[2]		±0.5		nA/°C typ	
DUTGND					
Voltage Range	-500		500	mV	
Leakage Current	-1		1	µA	
MEASURE OUTPUT (MEASOUT)					With respect to AGND
Measure Output Voltage Span			22.5	V	Software Programmable output range
Measure Pin output Impedance			100	Ω	
Output leakage current	-3		3	nA	With SW12 off
Output Capacitance[2]			15	pF	
Short Circuit Current[2]	-10		10	mA	
MEASOUT enable time		TBD	TBD	ns	Closing SW12
MEASOUT disable time		TBD	TBD	ns	Opening SW12
MEASOUT MI to MV switching time		TBD	TBD	ns	
GUARD OUTPUT					
Guard Output Voltage Span			22.5	V	
Guard Output Offset	-10		10	mV	
Short Circuit Current[2]	-10		10	mA	
Load Capacitance[2]			50	nF	
Guard Output Impedance		100		Ω	
Slew Rate[2]		3		V/µs	C_{LOAD} = TBD pf

Parameter	Min	Typ[1]	Max	Units	Test Conditions/Comments
FORCE AMPLIFIER					
Slew Rate[2]		0.4		V/us	Ccomp=100pF, Cff=220pF, Cload=200pF
Gain Bandwidth[2]		1		MHz	Ccomp=100pF, Cff=220pF, Cload=200pF
Max stable load Capacitance[2]			10,000	pF	C_{COMP} = 100pF. Larger Load cap requires larger C_{COMP}
FV SETTLING TIME TO 0.05% OF FSVR					FS step
64mA Range[2]		TBD	40	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
2mA range[2]		TBD	40	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
200µA range[2]		TBD	40	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
20µA range[2]		TBD	80	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
5µA range[2]		TBD	300	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
MI SETTLING TIME TO 0.05% OF FSCR					FS step
64mA Range[2]		TBD	TBD	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
2mA range[2]		TBD	TBD	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
200µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
20µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
5µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cff=220pF, Cload=200pF
FI SETTLING TIME TO 0.05% OF FSCR					FS step
64mA Range[2]		30	TBD	µs	Ccomp=100pF, Cload=200pF
2mA range[2]		30	TBD	µs	Ccomp=100pF, Cload=200pF
200µA range[2]		80	TBD	µs	Ccomp=100pF, Cload=200pF
20µA range[2]		680	TBD	µs	Ccomp=100pF, Cload=200pF
5µA range[2]		3000	TBD	µs	Ccomp=100pF, Cload=200pF
MV SETTLING TIME TO .05% OF FSVR					FS step
64mA Range[2]		TBD	TBD	µs	Ccomp=100pF, Cload=200pF
2mA range[2]		TBD	TBD	µs	Ccomp=100pF, Cload=200pF
200µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cload=200pF
20µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cload=200pF
5µA range[2]		TBD	TBD	µs	Ccomp=100pF, Cload=200pF
DAC SPECIFICATIONS					
Resolution			16	Bits	
Voltage Output Span[2]			22.5	V	V_{REF}=5V, within a range of -16.25 to 22.5V
Differential Nonlinearity[2]	-1		1	LSB	Guaranteed monotonic by design over temperature.
COMPARATOR DAC DYNAMIC SPECIFICATIONS					
Output Voltage Settling Time[2]			1.5	µs	1V change to ±1 LSB.
Slew Rate[2]		5		V/µs	
Digital-to-Analog Glitch Energy[2]		20		nV-s	
Glitch Impulse Peak Amplitude[2]			15	mV	
REFERENCE INPUT					
V_{REF} DC Input Impedance	1			MΩ	Typically 100 MΩ.
V_{REF} Input Current	-10		10	µA	Per input. Typically ±30 nA.
V_{REF} Range	2		5	V	
DIE TEMPERATURE SENSOR					
Accuracy		±7		°C	
Output Voltage at 25°C		1.5		V	
Output Scale Factor		5		mV/°C	
Output Voltage Range	0		3	V	
INTERACTION & CROSSTALK					
Crosstalk (VM)[2]	-0.01		0.01	% FSR	All channels in FIMV mode, measure the voltage for one channel in the highest current force range, once when all three other channels are at FI = 0mA and once when they are at 2mA
Crosstalk (MI)[2]	-0.01		0.01	% FSR	All channels in FVMI mode, measure the current for one channel in the lowest current measure range, once when all three other channels are at FV = -10V and once when they are at +10V
Crosstalk within a channel[2]			0.5	mV	All channels in FVMI mode, one channel at midscale, measure the current for one channel in the lowest current range, for a change in comparator or clamp DAC

Parameter	Min	Typ[1]	Max	Units	Test Conditions/Comments
					levels for that PMU.
Shorted DUT Crosstalk[2]		TBD	TBD		S/C applied to one PMU channel, measure effect on other channels.
SPI INTERFACE LOGIC					
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.7/2.0			V	(2.3 to 2.7)/(2.7 to 5.25V) Jedec Compliant Input Levels
V_{IL}, Input Low Voltage			0.7/0.8	V	(2.3 to 2.7)/(2.7 to 5.25V) Jedec Compliant Input Levels
I_{INH}, I_{INL}, Input Current	-1		1	µA	
C_{IN}, Input Capacitance[2]			10	pF	
CMOS LOGIC OUTPUTS					SDO, CPOX
V_{OH}, Output High Voltage	DV_{CC} – 0.4			V	
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA
Tristate leakage current	-1		1	µA	
Output Capacitance[2]			10	pF	
OPEN DRAIN LOGIC OUTPUTS					$\overline{BUSY}$, TMPALM, CGALM
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA, C_L = 50pF, R_{PULLUP} = 1kΩ
Output Capacitance[2]			10	pF	
LVDS INTERFACE LOGIC					
LOGIC INPUTS – Reduced Range Link					
Input Voltage Range	875		1575	mV	
Input Differential Threshold	-100		100	mV	
External Termination Resistance	80	100	120	Ω	
Differential Input Voltage	100			mV	
LOGIC OUTPUTS – Reduced Range Link					
Output Offset Voltage		1200		mV	
Output Differential Voltage		400		mV	
NOISE PERFORMANCE					
NSD of Measure Voltage In-Amp		TBD		nV/√Hz	@ 1kHz, measured at MEASOUT
NSD of Measure Current In-Amp		TBD		nV/√Hz	@ 1kHz, measured at MEASOUT
NSD of Force Amplifier		TBD		nV/√Hz	@ 1kHz, measured at FOH
POWER SUPPLIES					
AV_{DD}	10		28	V	$\lvert AV_{DD} - AV_{SS} \rvert \leq 33V$
AV_{SS}	-5		-23	V	
DV_{CC}	2.3		5.25	V	
AI_{DD}			25	mA	Excluding Load Conditions
AI_{SS}			25	mA	Excluding Load Conditions
DI_{CC}			3	mA	
Max Power Dissipation[2]			7	W	
Power Supply Sensitivity[2]					From DC to 1kHz
ΔForced Voltage/ΔAV_{DD}		-75		dB	
ΔForced Voltage/ΔAV_{SS}		-75		dB	
ΔMeasured Current/ΔAV_{DD}		-75		dB	
ΔMeasured Current/ΔAV_{SS}		-75		dB	
ΔForced Current/ΔAV_{DD}		-75		dB	
ΔForced Current/ΔAV_{SS}		-75		dB	
ΔMeasured Voltage/ΔAV_{DD}		-75		dB	
ΔMeasured Voltage/ΔAV_{SS}		-75		dB	
ΔForced Voltage/ΔDV_{CC}		-90		dB	
ΔMeasured Current/ΔDV_{CC}		-90		dB	
ΔForced Voltage/ΔDV_{CC}		-90		dB	
ΔMeasured Current/ΔDV_{CC}		-90		dB	

[1] Typical specifications are at 25°C and nominal supply, ±15.25V, unless otherwise noted.
[2] Guaranteed by design and characterization, not production tested.

FV = Force Voltage, FI = Force Current, MV = Measure Voltage, MI = Measure Current
FSR = Full Scale Range, FSCR = Full Scale Current Range, FS = Full Scale.
Specifications subject to change without notice.

TABLE 2. TIMING CHARACTERISTICS

$AV_{DD} \geq 10V$, $AV_{SS} \leq -5V$, $|AV_{DD} - AV_{SS}| \geq 20V$ and $\leq 33V$, $DV_{CC} = 2.3V$ to $5.25V$, $V_{REF}=5V$
($T_J = +25$ to $+90°C$, max specs unless otherwise noted.)

SPI INTERFACE (Figure 5 and Figure 6)			
Parameter[1, 2, 3]	**Limit at TMIN, TMAX**	**Unit**	**Description**
t_1	20	ns min	SCLK Cycle Time.
t_2	8	ns min	SCLK High Time.
t_3	8	ns min	SCLK Low Time.
t_4	10	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time.
t_5	15	ns min	Minimum $\overline{SYNC}$ High Time.
t_6	5	ns min	29th SCLK Falling Edge to $\overline{SYNC}$ Rising Edge.
t_7	5	ns min	Data Setup Time.
t_8	4.5	ns min	Data Hold Time.
t_9[3]	30	ns max	$\overline{SYNC}$ Rising Edge to $\overline{BUSY}$ Falling Edge.
t_{10}	1.2	µs max	$\overline{BUSY}$ Pulse Width Low
t_{11}	20	ns min	29th SLCK Falling EDGE to $\overline{LOAD}$ Falling Edge
t_{12}	20	ns min	$\overline{LOAD}$ pulse width low
t_{13}	150	ns min	$\overline{BUSY}$ rising edge to FOH Output Response time
t_{14}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LOAD}$ falling edge
t_{15}	100	ns max	$\overline{LOAD}$ rising edge to FOH Output Response time
t_{16}	10	ns min	$\overline{RESET}$ Pulse Width Low.
t_{17}	300	µs max	$\overline{RESET}$ Time Indicated by $\overline{BUSY}$ Low.
t_{18}	100	ns min	Minimum $\overline{SYNC}$ High Time in Readback Mode.
t_{19}[4]	25	ns max	SCLK Rising Edge to SDO Valid.
	595	ns min	Single channel write time
LVDS INTERFACE (Figure 7)			
Parameter[1, 2, 3]	**Limit at TMIN, TMAX**	**Unit**	**Description**
t_1	10	ns min	SCLK Cycle Time.
t_2	4	ns min	SCLK Pulse Width High and Low Time.
t_3	2	ns min	$\overline{SYNC}$ to SCLK Setup Time.
t_4	2	ns min	Data Setup Time.
t_5	2	ns min	Data Hold Time.
t_6	2	ns min	SCLK to $\overline{SYNC}$ Hold Time.
t_7	TBD	ns min	SCLK Rising Edge to SDO Valid.
t_8	TBD	ns min	$\overline{SYNC}$ high time

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f = 2$ ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 5 and Figure 6
[4] This is measured with circuit the load circuit of Figure 4

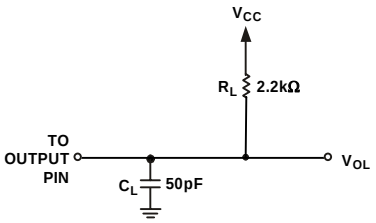


Figure 3.. Load Circuit for $\overline{CGALM}$, $\overline{TMPALM}$

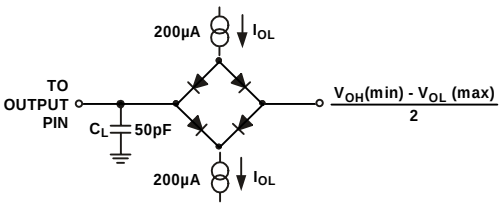


Figure 4. Load Circuit for SDO, $\overline{BUSY}$ Timing Diagram

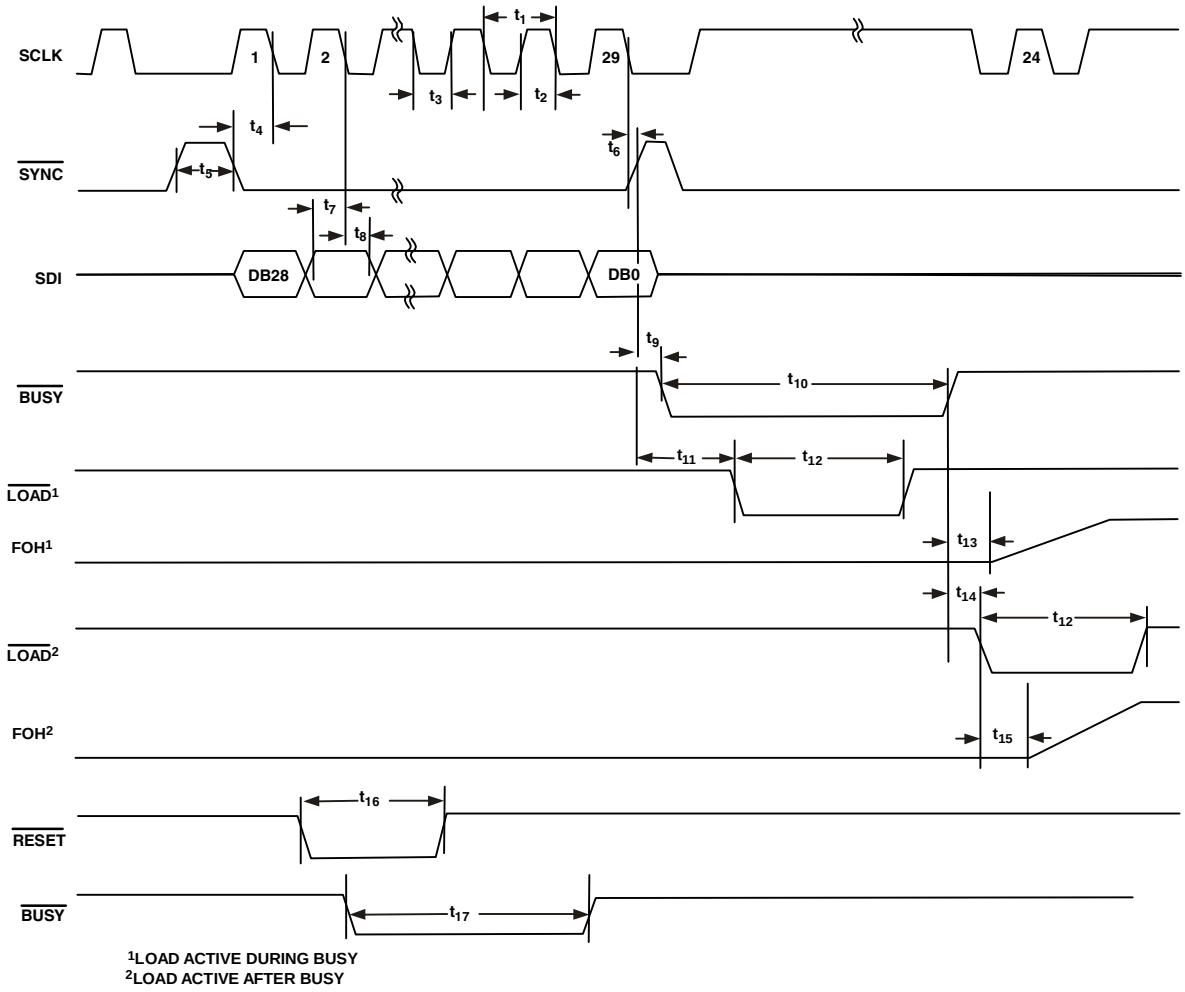


Figure 5. SPI Write Timing (Write word contains 29 bits)

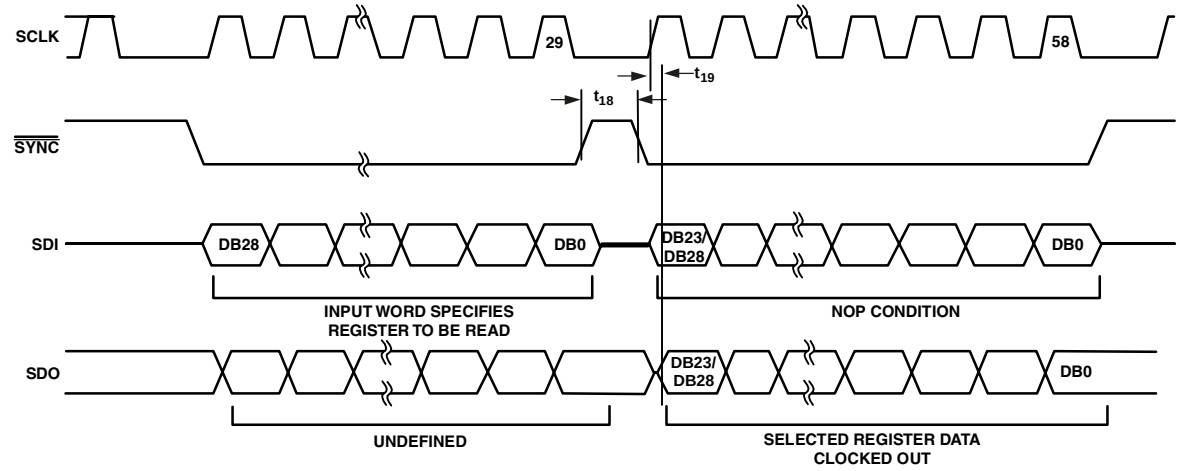


Figure 6. SPI Read Timing (Readback word contains 24 bits and can be clocked out with a minimum of 24 clock edges)

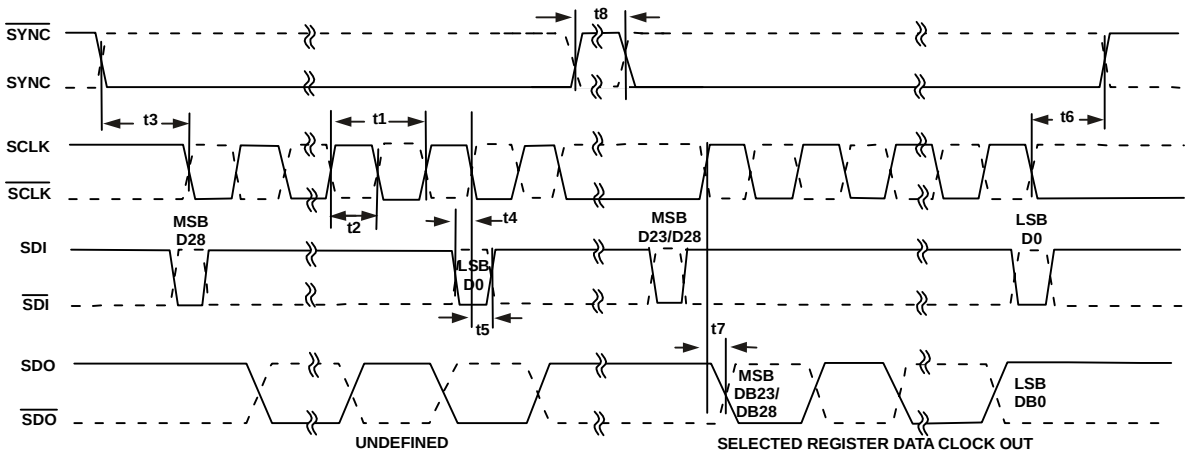


Figure 7. LVDS Read and Write Timing, (Readback word contains 24 bits and can be clocked out with a minimum of 24 clock edges)

ABSOLUTE MAXIMUM RATINGS

Table 3. AD5522 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage AV_{DD} to AV_{SS}	34V
AV_{DD} to AGND	-0.3V to 34V
AV_{SS} to AGND	0.3V to -34V
V_{REF} to AGND	-0.3 V, +7V
DUTGND, REFGND, AGND	AV_{DD} +0.3V to AV_{SS} -0.3V
DV_{CC} to DGND	- 0.3V to 7V
Digital Inputs to DGND	- 0.3V to DV_{CC} +0.3V
Analog Inputs to AGND	AV_{SS} - 0.3V to AV_{DD} +0.3V
Storage Temperature	–65°C to +125°C
Operating Junction Temperature	+25 to +90°C
Reflow Soldering	
Peak Temperature	230°C
Time at Peak Temperature	10s to 40s
Junction Temperature	150°C max

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE[3]

Thermal resistance values are specified for the worst-case conditions, i.e., specified for device soldered in circuit board for surface mount packages.

Table 4. Thermal Resistance (JEDEC 4 layer (1S2P) board)

Air Flow (LFPM)		0	200	500	Unit
TQFP Exposed Pad Down	θ_{JA}	22.3	17.2	15.1	°C/W
	θ_{JC}	0.3			°C/W
TQFP Exposed Pad Up	θ_{JA}	TBD	TBD	TBD	°C/W
	θ_{JC}	4.8			°C/W

Table 5. Thermal Resistance (JEDEC 4 layer (1S2P) board with cooling plate[4] at 45°C, natural convection at 55°C ambient)

Package Thermals	θ_{JA}	θ_{JA}	Unit
TQFP Exposed Pad Down	5.4	4.8	°C/W
TQFP Exposed Pad Up	3.0	0.3	°C/W

[3] Simulated Thermal information.
[4] Assumes perfect thermal contact between cooling plate and exposed paddle

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 8. Pin Configuration (Exposed Pad on bottom of package)

Table 6. Pin Function Descriptions

Pin No. Bottom	Pin No. Top	Mnemonic	Description
Bottom	**Top**	Exposed Pad	The exposed pad is electrically connected to AV_{SS}. TQFP with exposed pad on BOTTOM: For enhanced thermal, electrical and board level performance, the exposed paddle on the bottom of the package should be soldered to a corresponding thermal land paddle on the PCB.
22, 39, 62, 67, 79,	2, 14, 19, 42,59,	AV_{SS}(0-4)	Negative analog supply voltage
1, 20, 41, 60, 74	7, 21, 40, 61, 80	AV_{DD}(0-4)	Positive analog supply voltage
33	48	$\overline{\text{LOAD}}$	Active low logic input used for synchronizing updates within one device or across a group of devices. If synchronization is not required, $\overline{\text{LOAD}}$ may be tied low and updates to DAC channels or PMU modes will happen as they are presented to the device. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ FUNCTIONS section for detailed information.
34	47	DV_{CC}	Digital supply voltage
10, 11, 50, 51, 69	12, 30, 31, 70, 71	AGND	Analog ground, reference points for force and measure circuitry
30	51	DGND	Digital ground reference point.
23	58	$\overline{\text{BUSY}}$	Open Drain active low input/output indicating the status of interface.
24	57	SCLK	Clock input, active falling edge
25	56	CPOL0/ $\overline{\text{SCLK}}$	Comparator output low in SPI mode and $\overline{\text{SCLK}}$ in LVDS interface mode
26	55	CPOH0/ $\overline{\text{SDI}}$	Comparator output high in SPI mode and $\overline{\text{SDI}}$ in LVDS interface mode
27	54	SDI	Serial data input
28	53	$\overline{\text{SYNC}}$	Frame sync, active low
29	52	CPOL1/ SYNC	Comparator output low in SPI mode and SYNC in LVDS interface mode
31	50	CPOH1/$\overline{\text{SDO}}$	Comparator output high in SPI mode and $\overline{\text{SDO}}$ in LVDS interface mode

32	49	SDO	Serial data out, for readback and diagnostic purposes
35	46	CPOL2/CPO0	Comparator output Low, comparator window in LVDS interface mode
36	45	CPOH2/CPO1	Comparator output Low, comparator window in LVDS interface mode
37	44	CPOL3/CPO2	Comparator output Low, comparator window in LVDS interface mode
38	43	CPOH3/CPO3	Comparator output Low, comparator window in LVDS interface mode
66, 65, 64, 63	15, 16, 17, 18	MEASOUT(0-3)	Multiplexed DUT voltage/Current sense output/temperature sensor voltage per channel, referenced to AGND.
68	13	SYS_FORCE	External FORCE signal input, enables connection of system PMU.
70	11	SYS_SENSE	External SENSE signal output, enables connection of system PMU.
71	10	REFGND	Accurate analog reference input ground.
72	9	VREF	Reference Input for DAC channels, 5V for specified performance.
75	6	$\overline{\text{SPI}}$/LVDS	Interface select pin. Logic low selects SPI interface compatible mode, logic high selects LVDS interface mode. In LVDS mode the CPOH(0-3) pins default to differential interface pins.
76	5	$\overline{\text{CGALM}}$	$\overline{\text{CGALM}}$ is an open drain pin providing shared Alarm information for Guard amplifier and Clamp circuitry. By default, this output pin is disabled. The System Control Register allows user to enable this function and to set the open drain output as a latched output, or to configure either the Guard or Clamp function or both flagging the alarm pin. When this pin flags an alarm, the origins of the alarm may be determined by reading back the Alarm Status Register. Two flags per channel in this word (one latched, one unlatched) indicate which function caused the alarm and if the alarm is still present.
77	4	$\overline{\text{TMPALM}}$	The function of this pin is to flag a Temperature Alarm. It is a latched active low open drain output indicating the junction temperature has exceeded either the programmed or default (130degC) temperature setting. Two flags in the Alarm Status Register (one latched, one unlatched) indicate if the temperature has dropped below 130degC or still above. User action is required to clear this latched alarm flag, by writing to the "CLEAR" bit in any of the PMU registers.
78	3	$\overline{\text{RESET}}$	Active low, level sensitive input used to reset all internal nodes on the device to their power-on reset value.
3, 18, 43, 58	78, 63, 38, 23	C_{COMP}(0-3)	Compensation capacitor Input per channel. See section on compensation capacitors..
2, 19, 42, 59	79, 62, 39, 22	C_{FF} (0-3)	External capacitor optimizing the stability performance of the force amplifier (per channel).. See section on Compensation Capacitors
80, 21, 40, 61	1, 60, 41, 20	EXTFOH(0-3)	Per channel, Force output for high current range. Use external resistor here for current range up to 64mA.
6, 15, 46, 55	75, 66, 35, 26	FOH(0-3)	Per channel force output for all other ranges.
4, 17, 44, 57	77, 64, 37, 24	EXTMEASIH(0-3)	Per channel sense input (high sense) for high current range.
5, 16, 45, 56	76, 65, 36, 25	EXTMEASIL(0-3)	Per channel sense input (Low sense) for high current range.
9, 12, 49, 52	72, 69, 32, 29	MEASVH(0-3)	Per channel DUT voltage sense input (high sense)
73	8	DUTGND	DUT voltage sense input (low sense). By default, DUTGND is shared between all four PMU channels. If user requires a DUTGND input per channel, the GUARDIN (0-3)/DUTGND(0-3) pin may be configured to be a DUTGND input per each PMU channel.
7, 14 , 47, 54	74, 67, 34, 27	GUARD (0-3)	Guard output drive.
8, 13, 48, 53	73, 68, 33, 28	$\overline{\text{GUARDIN(0-3)}}$ /DUTGND(0-3)	This pin has dual functionality; it may be either a Guard input per channel or DUTGND per channel. Its function is determined via the serial interface. The power on default is GUARDIN, where it functions as the input to the Guard Amplifier. Alternatively, it may be configured to be a DUTGND input per channel. If selected as DUTGND via the interface, it now provides a DUTGND per Channel function and the input to the Guard amplifier is internally connected to MEASVH. See section on Guard Amplifier

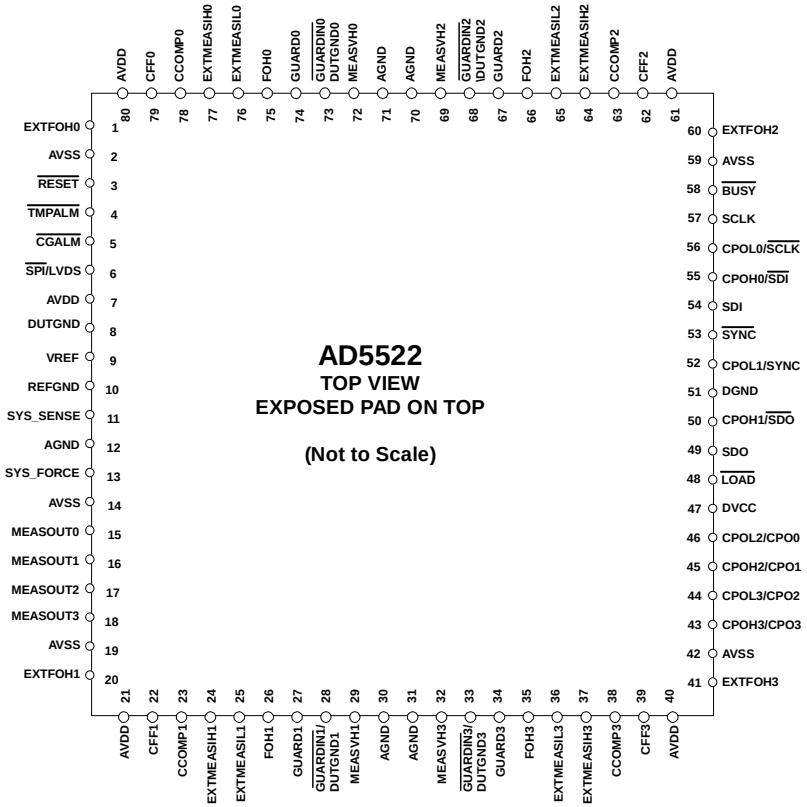


Figure 9. Pin Configuration (Exposed Pad on Top of package)

TERMINOLOGY

Offset Error
Offset error is a measure of the difference between actual and ideal voltage expressed in mV.
Gain Error Gain error is the difference between full-scale error and zero-scale error. It is expressed in %.

Gain Error = Full-Scale Error − Zero-Scale Error

Linearity Error
Relative accuracy, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the full-scale range. It is measured after adjusting for offset error and gain error and is expressed in % FSR.
CM Error
Common Mode Error is the error at the output of the amplifier due to the common mode input voltage. It is expressed in % of FSR/V.
Clamp Accuracy
Clamp accuracy is a measure of where the clamps begin to function fully and limit the clamped voltage or current.
Leakage Current
Current measured at an output pin, when that function is off or high impedance.
Pin Capacitance
Capacitance measured at a pin when that function is off or high impedance.
Slew Rate
The rate of change of output voltage, expressed in V/µs.

DAC SPECIFIC TERMS
Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB maximum ensures monotonicity.
Output Voltage Settling Time
The amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.
Digital-to-Analog Glitch Energy
The amount of energy injected into the analog output at the major code transition. The area of the glitch in is specified in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.
Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.
Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

FUNCTIONAL DESCRIPTION

The AD5522 is a highly integrated quad per pin parametric measurement unit (PPMU) for use in semiconductor automatic test equipment. It contains programmable modes to force a pin voltage and measure the corresponding current (FVMI), force current measure voltage (FIMV), force current measure current (FIMI), force voltage measure voltage (FVMV) and force nothing measure voltage (FNMV) or measure current (FNMI). The PPMU can force or measure a voltage range of 22.5 V. It can force or measure currents ranging up to 64mA per channel using the internal amplifier, while the addition of an external amplifier enables higher current ranges. On Chip are all the DAC levels required for each PMU channel.

FORCE AMPLIFIER

The force amplifier drives the analog output FOH, which drives a programmed current or voltage to the DUT (device under test). Headroom and footroom requirements for this amplifier is 3V on either end. An additional ±1V is dropped across the sense resistor when maximum current is flowing through it.

This amplifier is designed to drive DUT capacitances up to 10nF, with a compensation value of 100pF. Larger DUT capacitive load will require larger compensation capacitances.

Local feedback ensures the amplifiers are stable when disabled. A disabled channel reduces power consumption by 2.5mA/channel.

COMPARATORS

Per channel, the DUT measured value is monitored by two comparators configured as window comparators. Internal DAC levels set the CPL and CPH (low and high) threshold values. There are no restrictions on the voltage settings of the comparator high and lows. CPL going higher than CPH is not a useful operation; however, it will not cause any problems to the device. CPOL and CPOH are continuous time comparator outputs.

Table 7. Comparator Output Function

TEST CONDITION	CPOL	CPOH
V_{DUT} or I_{DUT} > CPH		0
V_{DUT} or I_{DUT} < CPH		1
V_{DUT} or I_{DUT} > CPL	1	
V_{DUT} or I_{DUT} < CPL	0	
CPH > V_{DUT} or I_{DUT} > CPL	1	1

When using SPI interface, full comparator functionality is available. When using the LVDS interface, the comparator function is limited to one output per comparator, due to the large pin count requirement of the LVDS interface. In this case, comparator output available CPO (0-3) provides information on whether the measured voltage or current is inside or outside the set CPH and CPL window. Information of whether the measurement was high or low is available via the serial interfaces (Comparator Status Register).

Table 8. Comparator Output Function using LVDS interface

TEST CONDITION	CPO Output
CPL < V_{DUT} And I_{DUT} < CPH	1
CPL > V_{DUT} or I_{DUT} > CPH	0

CLAMPS

Current and voltage clamps are included on chip per PMU channel. They protect the DUT in the event of an open or a short. Internal DAC levels set the CLL and CLH (low and high) levels and the clamps work to limit the force amplifier in the event of a voltage or current at the DUT exceeding the set levels. The clamps also function to protect the DUT when a transient voltage or current spike occurs when changing to a different operating mode or when programming the device to a different current range.

The voltage clamps are active while forcing current and the current clamps are active while forcing voltage. By default, the current clamps are off. Simply set them up via the status register through the serial interface.

If a clamp level has been hit, this will be flagged via the $\overline{\text{CGALM}}$ open drain output and the resulting alarm information may be read back via the SPI or LVDS interface. CLL should never be greater than CLH.

CURRENT RANGE SELECTION

Integrated thin film resistors minimize external components and allow easy selection of current ranges from 5 µA (200kΩ), 20µA (50kΩ), 200µA (5kΩ) and 2mA (500Ω). Per channel, one current range up to 64mA may be accommodated by connecting an external sense resistor. For current ranges in excess of 64mA, it is recommended an external amplifier be used.

For the suggested current ranges, the maximum voltage drop across the sense resistors is ±1V, however, to allow for correction of errors, there is some over range available in the current ranges. The full-scale voltage range that can be loaded to the DAC is ±11.5V; the forced current may be calculated as follows:

$$FI = \frac{VFIN}{RSENSE \times Gain}$$

Where:
FI = Forced Current
VFIN = Voltage of the FIN DAC, See V_{OUT} for DAC levels.
RSENSE = Selected Sense Resistor
Gain of Current Measure Instrumentation amplifier, it may be set (via the serial interface) to 5 or 10.

Using the 5kΩ sense resistor and ISENSE gain of 10, the maximum current range possible is ±225µA. Similarly for the other current ranges, there is an over range of 12.5% to allow for correction.

Also, the forced current range will only be the quoted full scale range with an applied reference of 5V or 2.5V (with ISENSE AMP gain = 5). The ISENSE amplifier is biased by the Offset DAC output voltage, in such as way as to center the Measure current output irrespective of the voltage span used.

When using the EXTFOHx outputs for current ranges up to 64mA, there is no switch in series with the EXTFOHx line, ensuring minimum capacitance presented at the output of the force amplifier. This is also an important feature if using a Pin electronics driver to provide high current ranges.

HIGH CURRENT RANGES

With the use of an external high current amplifier, one high current range in excess of 64mA is possible. The high current amplifier simply buffers the force output and provides the drive for the required current.

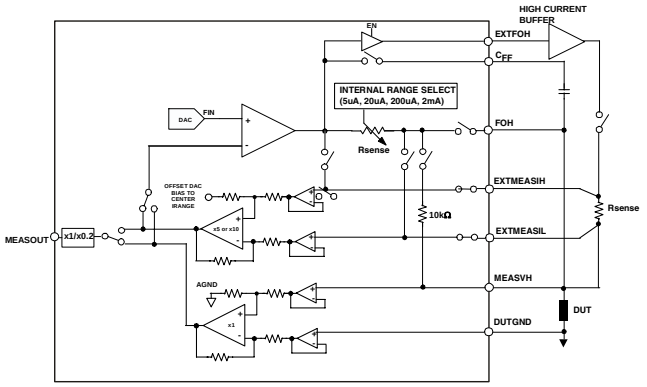


Figure 10. Addition of high current amplifier for wider current range(>64mA)

DEVICE UNDER TEST GROUND (DUTGND)

By default, there is one DUTGND input available for all four PMU channels. In some applications of a PMU, it is necessary that each channel operate from its own DUTGND level. There is a shared pin in the form of the $\overline{\text{GUARDIN}}$(0-3)/DUTGND(0-3) which may be shared as either the input to the GUARD amplifier (GUARDIN), or as a DUTGND per channel function. This should be configured through the serial interface on power on as per required operation. The default connection is SW13b and SW14b. When configured as DUTGND per channel, this multifunction pin is no longer connected to the input of the guard amplifier, it is instead connected to the low end of the instrumentation amplifier (SW14a), and the input of the Guard amplifier is not connected internally to MEASVH (SW13a).

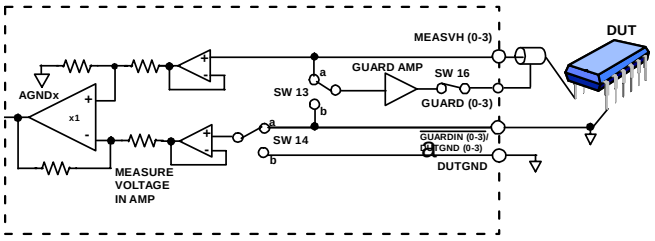


Figure 11. Using the DUTGND per channel Feature

GUARD AMPLIFER

A Guard amplifier allows the user to bootstrap the shield of the cable to the voltage applied to the DUT, ensuring minimal drops across the cable. This is particularly important for measurements requiring a high degree of accuracy and in leakage current testing.

If not required, all four Guard Amplifiers may be disabled via the serial interface (through the System Control Register), this decreases the power consumption by 400uA per channel.

As described in the DUTGND section, the $\overline{\text{GUARDIN(0-3)}}$ /DUTGND(0-3) is a shared pin. It can function either as a guard amplifier input per channel or as a DUTGND input per channel as required by the end application. Refer to Figure 11.

A Guard alarm event occurs when the guard output moves more than 100mV away from the Guard input voltage for more than 200µs. In the event this happens, this will be flagged via the $\overline{\text{CGALM}}$ open drain output. As the guard and clamp alarm functions share the same alarm output$\overline{\text{CGALM}}$, the alarm information (alarm trigger and alarm channel) is available via the serial interface (ALARM STATUS REGISTER).

Alternatively, the serial interfaces allow the user to setup the $\overline{\text{CGALM}}$ output to flag either the clamp status or the guard status. By default, this open drain alarm pin is an unlatched output, but may be set to a latched output via the serial interface, System Control Register.

COMPENSATION CAPACITORS

Each channel requires an external compensation capacitor (C_{COMP}) to ensure stability into the maximum load capacitance while ensuring settling time is optimized. In addition, one C_{FF} pin is provided to further optimize stability and settling time performance when in Force voltage mode. When changing from Force current to force voltage mode, the switch connecting C_{FF} capacitor is automatically closed. While the force amplifier is designed to drive load capacitances up to 10nF, using larger compensation capacitor values, it is possible to drive larger load at the expense of an increase in settling time. If a wide range of load capacitance must be driven, then an external multiplexer connected to the C_{COMP} pin will allow optimization of settling time versus stability. The series resistance of a switch placed on C_{COMP}, should typically be <50Ω.

Similarly, connecting the C_{FF} node to a multiplexer externally, would cater for a wide range of CDUT in Force Voltage mode. The series resistance of the multiplexer used should be such that:

$$\left(\frac{1}{2\Pi RON \times CDUT}\right) > 100kHz$$

Table 9. Suggested Compensation Capacitor Selection

C_{LOAD}	C_{COMP}	C_{FF}
≤1nF	100pF	220pF
≤10nF	100pF	1nF
≤100nF	C_{LOAD}/100	C_{LOAD}/10

SYSTEM FORCE SENSE SWITCHES

Each channel has switches to allow connection of the force (FOHx) and sense (MEASVHx) lines to a central PMU for calibration purposes. There is one set of SYS_FORCE and SYS_SENSE pins per device.

TEMPERATURE SENSOR

An on board temperature sensor monitors temperatures and in the event of the temperature exceeding a factory defined value, (130°C) or a user programmable value, the device will protect itself by shutting down all channels and will flag an alarm through the latched open drain $\overline{\text{TMPALM}}$ pin. Alarm status may be readback from the Alarm Status Register or the PMU registers where latched and unlatched bits tell if an alarm has occurred and whether the temperature has dropped below the set alarm temperature.

MEASURE OUTPUT (MEASOUT)

The measured DUT voltage or current (voltage representation of DUT current) is available on MEASOUT (0-3) with respect to AGND. The default MEASOUT range is the forced voltage range for voltage measure and current measure (nominally ±11.25V, depends on reference voltage and offset DAC) and includes some over range to allow for offset correction. The serial interface allows the user to select another MEASOUT range of V_{REF} to AGND, allowing for a smaller input range ADC to be used. Each PMU channel MEASOUT line may be made high impedance via the serial interface.

When using low supply voltages, ensure that there is sufficient headroom and footroom for the required force voltage range.

The Offset DAC also directly offsets the MEASURE output voltage level, but only when GAIN1 = 0.

Table 10. MEASOUT Output Ranges

MEASOUT Function			**GAIN1 = "0" V_{REF} = 5V**	**GAIN1 = "1"**
			MEASOUT Gain = 1	**MEASOUT Gain = 1/5**
MV			±VDUT (up to 11.25V)	$0 \text{ to } \frac{4.5VREF}{5}$
MI	**GAIN0 = "0"**	CURRENT MEAS GAIN = 10	$\pm V_{RSENSE}$ X 10 = up to ±11.25V	0 to 4.5V
	GAIN0 = "1"	CURRENT MEAS GAIN = 5	$\pm V_{RSENSE}$ X 5 = up to ±5.625	0 to 2.25V

DAC LEVELS

Each channel contains five dedicated DAC levels : one for the force amplifier, one each for the clamp high and low levels and one each for the comparator high and low levels.

The architecture of a single DAC channel consists of a 16-bit resistor-string DAC followed by an output buffer amplifier. This resistor-string architecture guarantees DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier.

The transfer function for DAC outputs is:

$$V_{OUT} = 4.5V_{REF}\left(\frac{DACCODE}{2^{16}}\right) - 3.5V_{REF}\left(\frac{OFFSETDAC\ CODE}{2^{16}}\right) + DUTGND$$

Where the voltage range must be take into account the +/-4V headroom and footroom requirements for the amplifier and sense resistor and must be within the range -16.25V to 22.5V (22V range + 500mV overrange to allow for correction).

OFFSET DAC

The device is capable of forcing a 22.5V ($4.5 \times V_{REF}$) voltage range. Included on chip is one 16 Bit offset DAC (one for all four channels) which allows for adjustment of the voltage range.

The useable range is -16.25V to 22.5V. Zero scale gives a full-scale range of 0V to +22.5V, mid scale gives ±11.25V, while the most negative useful range is in a range of -16.25V to 6.25V. Full scale loaded to the Offset DAC does not give a useful output voltage range as the output amplifiers are limited by available footroom. The following table shows the effect of the Offset DAC on the other DACs in the device.

Table 11. OFFSET DAC Relationship with other DACs with V_{REF} = 5V

Offset DAC Code	DAC Code	DAC Output Voltage Range
0	0	0.00 V
0	32768	11.25 V
0	65535	22.50 V
32768	0	-8.75 V
32768	32768	2.50 V
32768	65535	13.75 V
42130	0	-11.25 V
42130	32768	0.00 V
42130	65535	11.25 V
60855	0	-16.25
60855	32768	-5.00
60855	65535	6.25
65535	-	Footroom Limitations

Therefore, depending on headroom available, the input to the Force Amplifier may be unipolar positive, or bipolar, either symmetrical or asymmetrical about DUTGND but always within a voltage span of 22.5V.

The offset DAC offsets all DAC functions. It also centers the current range, such that zero current always flows at midscale code irrespective of offset DAC setting.

Rearranging the transfer function for the DAC output gives the following equation to determine what Offset DAC code is required for a given reference and output voltage range.

$$OFFSETDAC\ CODE = \left(\frac{2^{16}(V_{OUT} - DUTGND)}{3.5V_{REF}}\right) - \left(\frac{4.5 \times DACCODE}{3.5}\right)$$

OFFSET AND GAIN REGISTERS

Each DAC level contains independent offset and gain control registers that allow the user to digitally trim offset and gain. These registers give the user the ability to calibrate out errors in the complete signal chain, including the DAC, using the internal m and c registers, which hold the correction factors. All registers in the AD5522 are volatile, so need to be loaded on power on during a calibration cycle.

The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 1)/\ 2^n \times x1] + (c - 2^{n-1})$$

where:
x2 = the data-word loaded to the resistor string DAC.
x1 = the 16-bit data-word written to the DAC input register.
m = code in gain register (default code = $2^{16} - 1$.)
c = code in offset register (default code = 2^{15})
n = DAC resolution (*n* = 16).
The calibration engine is only engaged when data is written to the x1 register. This has the advantage of minimizing the setup time of the device.

CACHED X2 REGISTERS

Each DAC has a number of cached x2 values. These registers store the result of an offset and gain calibration in advance of a mode change. This enables the user to preload registers; allow the calibration engine to calculate the appropriate x2 value and store until ready to change modes. As the data is ready and held in the appropriate register, this enables mode changing be as time efficient as possible. If an update occurs to a DAC register set that is currently part of the operating PMU mode, the DAC output will update immediately (depending on $\overline{\text{LOAD}}$ condition).

Offset and Gain registers for the FIN DAC

The FIN (force amplifier input) DAC level contains independent offset and gain control registers that allow the user to digitally trim offset and gain. There are six sets of x1, m and c registers, one set (x1, m and c) for the force voltage range, and one set for each of the force current ranges (4 internal current ranges and 1 external current range). Six x2 registers store calculated DAC values ready to load to the DAC register on a mode change.

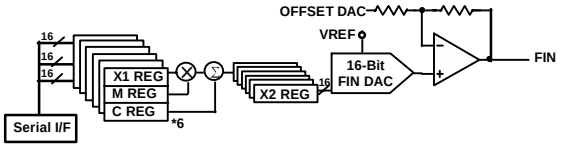


Figure 12. FIN DAC Registers

Offset and Gain registers for the COMPARATOR DACs

The Comparator DAC levels contain independent offset and gain control registers that allow the user to digitally trim offset and gain. There are six sets of (x1, m and c) registers, one set for the voltage mode, and one set for each of the four internal current ranges and one set for the external current range. In this way, x1 may also be preprogrammed, so switching different modes, allows for efficient switching into the required compare mode. Six x2 registers store cached calculated DAC values ready to load to the DAC register on a mode change.

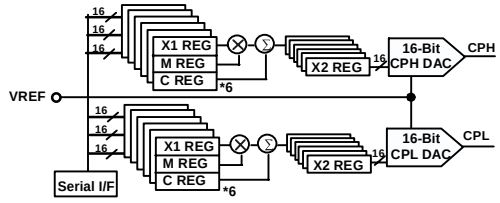


Figure 13. Comparator Registers

Offset and Gain registers for the Clamp DACs

The clamp DAC levels contain independent offset and gain control registers that allow the user to digitally trim offset and gain. There are just two sets of registers, one for the voltage mode and another register set (x1, m and c) for all five current ranges. Two x2 registers store cached calculated DAC values ready to load to the DAC register on a PMU mode change.

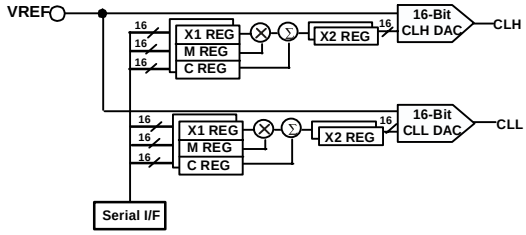


Figure 14. Clamp Registers

V_{REF}

One buffered analog input supplies all 20 DACs with the necessary reference voltage to generate the required DC levels.

REFERENCE SELECTION

The voltage applied to the V_{REF} pin determines the output voltage range and span applied to the force amplifier, clamp and comparator inputs. This device can be used with a reference input ranging from 2V to 5V, however, for most applications, a reference input of 5V or 2.5V will be sufficient to meet all voltage range requirements. The DAC amplifier gain is 4.5, which gives a DAC output span of 22.5V. The DACs have offset and gain registers which can be used to calibrate out system errors.

In addition, the gain register can be used to reduce the DAC output range to the desired force voltage range. The Force DAC will retain 16 bit resolution even with a gain register setting of quarter scale (0x4000). Therefore, from a single 5V reference, it is possible to get a voltage span as high as 22.5V or as low as 5.625V all from one 5V reference.

When using the offset and gain registers, the chosen output range should take into account the system offset and gain errors that need to be trimmed out. Therefore, the chosen output range should be larger than the actual, required range.

When using low supply voltages, ensure that there is sufficient headroom and footroom for the required force voltage range. Also, note that with a supply differential of less than 18V and a full scale current range requirement, it is necessary to reduce the current measure in amp gain to 5 so the feedback path can swing through the full range.

Also, the forced current range will only be the quoted full scale range with an applied reference of 5V or 2.5V (with ISENSE AMP gain = 5).

For other voltage/current ranges, the required reference level can be calculated as follows:

1. Identify the nominal range required
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range including the expected maximum offset and gain errors.
4. Choose the new required $VOUT_{max}$ and $VOUT_{min}$, keeping the VOUT limits centered on the nominal values. Note that AV_{DD} and AV_{SS} must provide sufficient headroom.
5. Calculate the value of V_{REF} as follows:

$$V_{REF} = (VOUT_{MAX} - VOUT_{MIN})/4.5$$

Reference Selection Example

Nominal Output Range = 10V (-2V to +8V)
Offset Error = ±100mV
Gain Error = ±0.5%
REFGND = AGND = 0V

1) *Gain Error* = ±0.5%
   => *Maximum Positive Gain Error* = +0.5%
   => *Output Range incl. Gain Error*
   = 10 + 0.005(10)=10.05V

2) *Offset Error* = ±100mV
   => *Maximum Offset Error Span* = 2(100mV)=0.2V
   => *Output Range including Gain Error and Offset Error* = 10.05V + 0.2V = 10.25V

3) V_{REF} *Calculation*
   Actual Output Range = 10.25V, that is -2.125V to +8.125V *(centered);*
   V_{REF} = (8.125V + 2.125V)/4.5 = 2.28V

If the solution yields an inconvenient reference level, the user can adopt one of the following approaches:

1. Use a resistor divider to divide down a convenient, higher reference level to the required level.
2. Select a convenient reference level above V_{REF} and modify the Gain and Offset registers to digitally downsize the reference. In this way the user can use almost any convenient reference level.
3. Use a combination of these two approaches

In this case, the optimum reference to choose is a 2.5V reference, then use the m and c registers and the OFFSET DAC to achieve the required -2V to +8V range. The ISENSE amplifier gain should be changed to a gain of 5. This ensures a full scale current range of the specified values and also allows optimization of power supplies and minimizes power consumption within the device.

CALIBRATION

The user can perform a system calibration by overwriting the default values in the m and c registers for any individual DAC channels as follows:

Calculate the nominal offset and gain coefficients for the new output range (see previous example)

Calculate the new m and c values for each channel based on the specified offset and gain errors

Calibration Example

Nominal Offset Coefficient = 32768
Nominal Gain Coefficient = 10/10.25x 65535 = 63937
12/12.26× 65535 = 64145

Example 1: Gain Error = +0.5%, Offset Error = +100mV

1) Gain Error (0.5%) Calibration: 63937 × 0.995 = 63617
=> *Load Code* "0b1111 1000 1000 0001" *to m register*

2) Offset Error (100mV) Calibration:
LSB Size = 10.25/65535 = 156 µV;
Offset Coefficient for 100mV Offset = 100/0.156 = 641 LSBs
=> *Load Code* "0b0111 1101 0111 1111" *to c register*

SYSTEM LEVEL CALIBRATION

There are many ways to calibrate the device on power on. The following gives an example of how to calibrate the FIN DAC of the device without a DUT or DUT board connected.
Calibration Procedure for Force and Measure circuitry:

1) Calibrate Force Voltage (2 point)
   Write zero scale to the Force DAC (FIN), connect SYS_FORCE to FOHx and SYS_SENSE to MEASVHx, close the internal Force/Sense Switch (SW 7). Using the System PMU, measure the error between voltage at FOHx, MEASVHx and desired value.
   Similarly, load Full scale to the Force DAC, and measure the error between FOHx , MEASVH and the desired value. Work out m and c values. Load these values to appropriate m and c registers for Force DAC.

2) Calibrate Measure Voltage (2 point)
   Connect SYS_FORCE to FOH, SYS_SENSE to MEASVHx Close Internal Force/Sense switch (SW 7). Force voltage on FOH via SYS_FORCE and measure voltage at MEASOUT. The difference is the error between the actual forced voltage and the voltage at MEASOUT.

3) Calibrate Force current (2 point)
   In Force current mode, write zero and fullscale to the Force DAC. Connect SYS_FORCE to external ammeter and to FOH pin. Measure error on zero and fullscale current and calculate m and c values.

4) Calibrate Measure Current (2 Point)
   Write zero scale to the Force DAC in Force Current mode. Connect SYS_FORCE to an external ammeter and to the FOH pin. Measure the error between ammeter reading and MEASOUT reading. Repeat with Full scale loaded to the Force DAC.

5) Repeat for all four channels.

Similarly, calibrate the comparators and clamp DACs and load the appropriate gain and offset registers. Calibrating these DACs will require some successive approximation to find where the comparator trips or the clamps engage.

CIRCUIT OPERATION

FORCE VOLTAGE, FV

Most PMU measurements are performed while in force voltage and measure current mode, for example, when the device is used as a device power supply, or in continuity or leakage testing. In the force voltage mode, the voltage forced is mapped directly to the DUT. The voltage measure amplifier completes the loop giving negative feedback to the forcing amplifier. See Figure 15.

Forced Voltage at DUT = VFIN

Where:
VFIN = Voltage of the FIN DAC, See V_{OUT} for DAC levels.

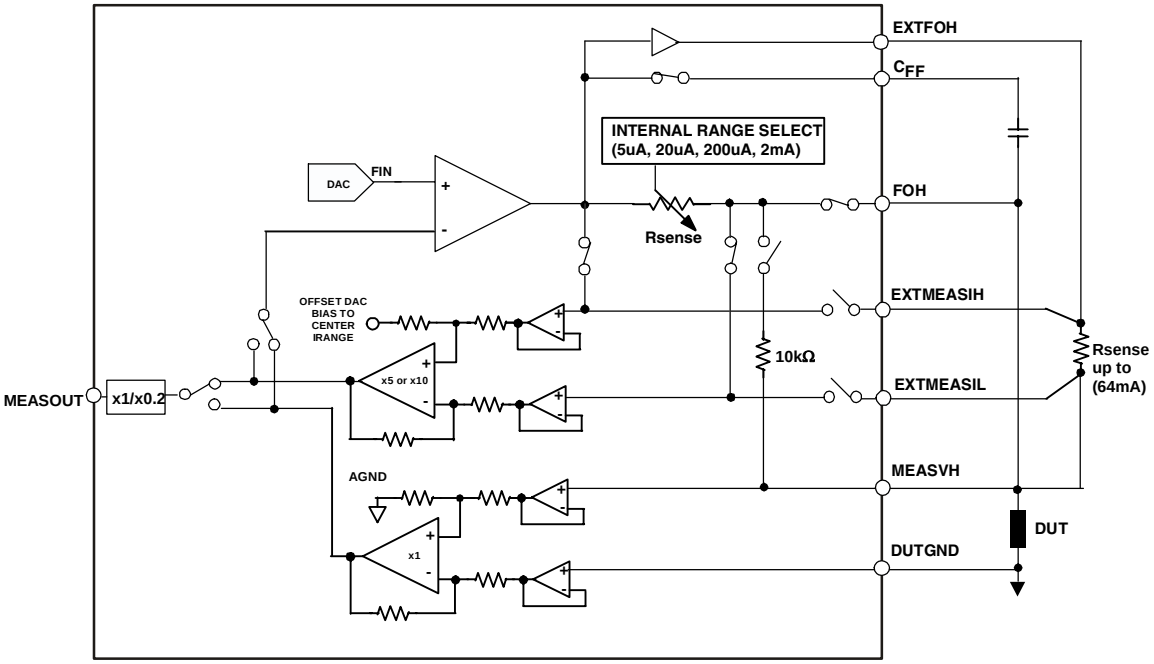


Figure 15. Forcing voltage, measuring current

FORCE CURRENT, FI

In the force current mode, the voltage at FIN is now converted to a current and applied to the DUT. The feedback path is now the current measure amplifier, feeding back the voltage measured across the sense resistor and MEASOUT reflects the voltage measured across the DUT. See Figure 16.

For the suggested current ranges, the maximum voltage drop across the sense resistors is ±1V, however, to allow for correction of errors, there is some over range available in the current ranges. The maximum full-scale voltage range that can be loaded to the FIN DAC is ±11.5V; the forced current may be calculated as follows:

$$FI = \frac{VFIN}{RSENSE \times Gain}$$

Where:
FI = Forced Current
VFIN = Voltage of the FIN DAC, See V_{OUT} for DAC levels.
RSENSE = Selected Sense Resistor
Gain of Current Measure Instrumentation amplifier, it may be set (via the serial interface) to 5 or 10.

The ISENSE amplifier is biased by the Offset DAC output voltage, in such as way as to center the Measure current output irrespective of the voltage span used.

Using the 5kΩ sense resistor and ISENSE gain of 10, the maximum current range possible is ±225μA. Similarly for the other current ranges, there is an over range of 12.5% to allow for correction.

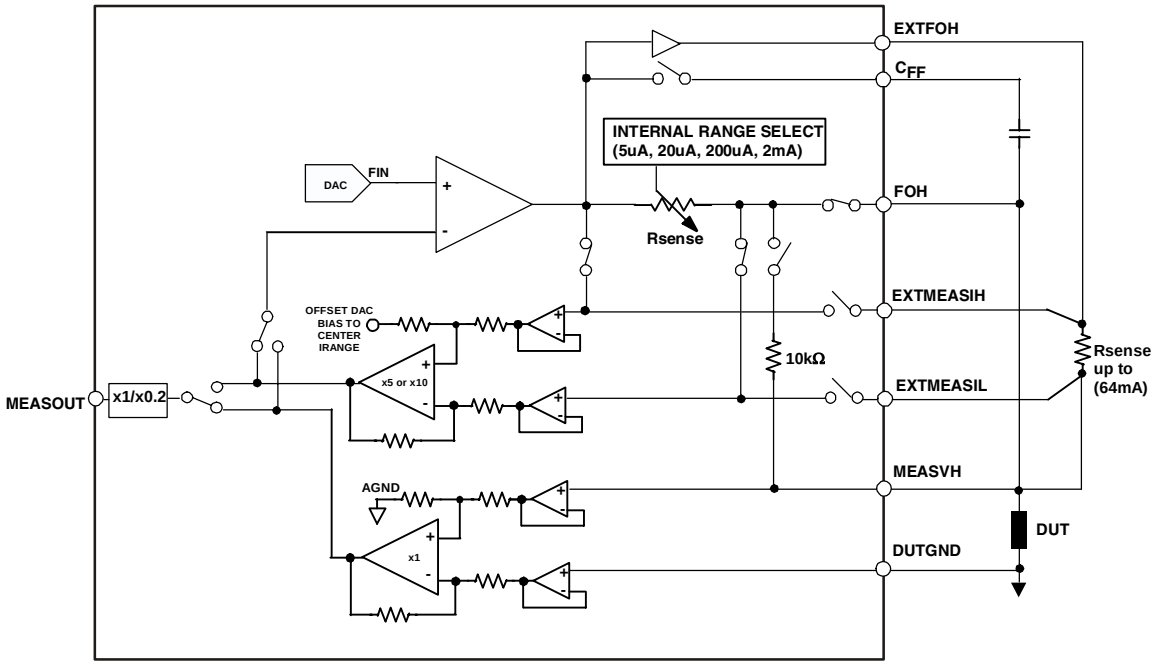


Figure 16. .Forcing current, measuring voltage

SERIAL INTERFACE

The AD5522 contains two high-speed serial interfaces, an SPI compatible, interface operating at clock frequencies up to 50MHz, and an EIA-644-compliant, LVDS interface. To minimize both the power consumption of the device and on-chip digital noise, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$.

SPI INTERFACE

The serial interface operates over a 2.3V to 5.25V DV_{CC} supply range. The serial interface is controlled by four pin, as follows:

$\overline{\text{SYNC}}$ Frame synchronization input.

SDI Serial data input pin.

SCLK Clocks data in and out of the device.

SDO Serial data output pin for data readback purposes.

There is also an $\overline{\text{SPI}}$/LVDS select pin, which must be held low for SPI interface and high for LVDS interface.

LVDS INTERFACE

The LVDS interface uses the same input pins as the SPI interface with the same designations. In addition, three other pins are provided for the complementary signals needed for differential operation, thus:

SYNC/$\overline{\text{SYNC}}$ Differential frame synchronization signal.

SDI/$\overline{\text{SDI}}$ Differential serial data input.

SCLK/$\overline{\text{SCLK}}$ Differential clock input.

SDO/$\overline{\text{SDO}}$ Serial data output pin for data readback

SERIAL INTERFACE WRITE MODE

The AD5522 allows writing of data via the serial interface to every register directly accessible to the serial interface, which is all registers except the DAC registers.

The serial word is 29 bits long. The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5522 by clock pulses applied to SCLK. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. At least 29 falling clock edges must be applied to SCLK to clock in 29 bits of data, before $\overline{\text{SYNC}}$ is taken high again.

The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. In order for another serial transfer to take place, $\overline{\text{SYNC}}$ must be taken low again.

$\overline{\text{RESET}}$ FUNCTION

Bringing the level sensitive $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state (detailed in the section Power On Default). This sequence takes approx 300µs. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled. When $\overline{\text{BUSY}}$ returns high, normal operation resumes and the status of the $\overline{\text{RESET}}$ pin is ignored until it goes low again. The SDO output will be high impedance during a power on reset or a $\overline{\text{RESET}}$.

Power on reset follows the same function as $\overline{\text{RESET}}$.

$\overline{\text{BUSY}}$ AND $\overline{\text{LOAD}}$ FUNCTION

$\overline{\text{BUSY}}$ is an open drain output that indicates the status of the AD5522 interface. When writing to any of the registers $\overline{\text{BUSY}}$ goes low and stays low until the command completes.

Writing to a DAC register drives the $\overline{\text{BUSY}}$ signal low for longer than a simple PMU or System Control Register write. For the DACs, the value of the internal cached (x2) data is calculated and stored each time the user writes new data to the corresponding x1 register. During this write and calculation, the $\overline{\text{BUSY}}$ output is driven low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no output updates can take place.

X2 values are stored and held until a PMU word is written that calls the appropriate cached x2 register. Only then does a DAC output update.

The DAC outputs and PMU modes are updated by taking the $\overline{\text{LOAD}}$ input low. If $\overline{\text{LOAD}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LOAD}}$ event is stored and the DAC outputs or PMU modes update immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LOAD}}$ input permanently low. In this case, the change in DAC outputs or PMU modes update immediately after $\overline{\text{BUSY}}$ goes high.

The $\overline{\text{BUSY}}$ pin is bidirectional and has a 50 kΩ internal pullup resistor. Where multiple AD5522 devices may be used in one system, the $\overline{\text{BUSY}}$ pins can be tied together. This is useful where it is required that no DAC or PMU in any device is updated until all others are ready. When each device has finished updating the x2 registers, it will release the $\overline{\text{BUSY}}$ pin. If another device has not finished updating its x2 registers, it will hold $\overline{\text{BUSY}}$ low, thus delaying the effect of $\overline{\text{LOAD}}$ going low. As there is only one multiplier shared between four channels, this task must be done sequentially, so the length of the $\overline{\text{BUSY}}$ pulse will vary according to the number of channels being updated.

Table 12. $\overline{\text{BUSY}}$ Pulse Width

Action	$\overline{\text{BUSY}}$ Pulse Width (μs max)
Loading data to PMU, System Control Register or Readback	0.15
Loading x1 to any 1 PMU DAC Channel	1.25
Loading x1 to any 2 PMU DAC Channels	1.75
Loading x1 to any 3 PMU DAC Channels	2.25
Loading x1 to any 4 PMU DAC Channels	2.75

$\overline{\text{BUSY}}$ Pulse Width = ((Number of channels +1) × 500ns) + 250ns

$\overline{\text{BUSY}}$ also goes low during power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin.

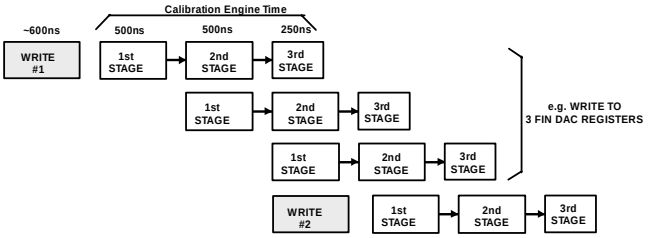


Figure 17. Multiple writes to DAC x1 registers

Writing data to the System control register, PMU control register, m or c registers do not involve the digital calibration engine, thus speeding up configuration of the device on power on.

REGISTER UPDATE RATES

As mentioned previously the value of the X2 register is calculated each time the user writes new data to the corresponding X1 register. The calculation is performed by a three stage process. The first two stages take 500ns each and the third stage takes 250ns. When the writes to one of the X1 registers is complete the calculation process begins. If the write operation involves the update of a single DAC channel the user is free to write to another register provided that the write operation doesn't finish until the first stage calculation is complete, i.e. 500ns after the completion of the first write operation.

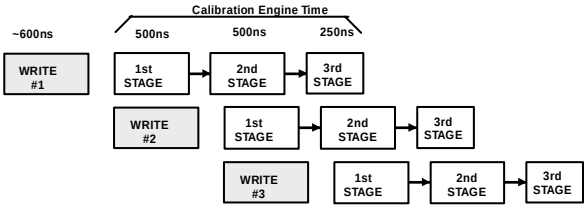


Figure 18. Multiple Single Channel writes engaging calibration engine

REGISTER SELECTION

The serial word assignment consists of 29 bits. Bits 28 through to 22 are common to all registers, whether writing to or reading from the device. PMU3 to PMU0 data bits address each PMU channel (or associated DAC register). When PMU3 to PMU0 are all zeros, the System Control Register is addressed. Mode Bits MODE0 and MODE1 address the different sets of DAC registers and the PMU register.

Readback Control, RD/$\overline{WR}$

The R/$\overline{W}$ bit set high initiates a readback sequence of PMU, Alarm, Comparator, System Control Register or DAC information as determined by address bits.

PMU Address Bits, PMU3, PMU2, PMU1, PMU0

Bits PMU3 through PMU0 address each of the PMU channels on chip. This allows individual control of each PMU channel or any manner of combined addressing in addition to multi channel programming. PMU bits also allow access to write registers such as the System Control Register and the many DAC registers, in addition to reading from all the registers.

Table 13. Mode Bits

B23	B22	WRITE FUNCTION
MODE1	MODE0	Action
0	0	System Control Register or PMU Register
0	1	DAC Gain (m) Register
1	0	DAC Offset (c) Register
1	1	DAC Input Data Register, (x1)

Table 14. Read and Write Functions of the AD5522

B28	B27	B26	B25	B24	B23	B22	B21 to B0	SELECTED REGISTER			
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	DATA BITS	CH3	CH2	CH1	CH0
WRITE FUNCTIONS											
0	0	0	0	0	0	0	DATA BITS	Write to System Control Register (Table 16)			
0	0	0	0	0	0	1	DATA BITS	RESERVED			
0	0	0	0	0	1	0	DATA BITS	RESERVED			
0	0	0	0	0	1	1	11 1111 1111 1111 1111 1111b	NOP (No Operation)			
0	0	0	0	0	1	1	DATA BITS other than all 1's	RESERVED			
WRITE ADDRESSED DAC OR PMU REGISTER											
0	0	0	0	1	Select DAC or PMU Registers. See Table 13		DATA BITS	×	×	×	CHO
0	0	0	1	0				×	×	CH1	×
0	0	0	1	1				×	×	CH1	CH0
0	0	1	0	0				×	CH2	×	×
0	-	-	-	-				-	-	-	-
0	1	0	0	0				CH3	×	×	×
0	-	-	-	-				-	-	-	-
0	1	1	1	0				CH3	CH2	CH1	×
0	1	1	1	1				CH3	CH2	CH1	CH0
READ FUNCTIONS											
1	0	0	0	0	0	0	All zeros	Read from System Control Register			
1	0	0	0	0	0	1	All zeros	Read from Comparator Status Registers			
1	0	0	0	0	1	0	X	Reserved			
1	0	0	0	0	1	1	All zeros	Read from Alarm Status Register			
READ ADDRESSED DAC or PMU REGISTER – Can only read one PMU or DAC register at one time.											
1	0	0	0	1	PMU/.DAC REGISTER ADDRESS		DAC ADDRESS SEE	×	×	×	CH0
1	0	0	1	0	SEE Table 13		Table 21	×	×	CH1	×
1	0	1	0	0				×	CH2	×	×
1	1	0	0	0				CH3	×	×	×

NOP (No Operation)

If a NOP (No Operation) command is loaded, no change is made to DAC or PMU registers. This code is useful when performing a read back of a register within the device (via the SDO pin) where a change of DAC code or PMU function may not be required

Reserved Commands

Any bit combination that is not described in the Register address tables for the PMU, DAC and System Control Registers are Reserved commands. These commands are unassigned commands; they are reserved for factory use. To ensure correct operation of the device, do not used reserved commands.

WRITE SYSTEM CONTROL REGISTER

The System Control Register is accessed when the PMU channel address PMU3-PMU0 and Mode Bits, MODE1 and MODE0 are all zeros. It allows quick setup of different functions within the device. The System Control Register operates on a per device basis.

Table 15. System Control Register Bits

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1/0
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CL3	CL2	CL1	CL0	CPOLH3	CPOLH2	CPOLH1	CPOLH0	CPBIASEN	DUTGND/CH	GUARD ALM	CLAMP ALM	INT10K	GUARD EN	GAIN1	GAIN0	TMP ENABLE	TMP1	TMP0	LATCHED	0

Table 16. System Control Register Functions

Bit	Bit name	Description
28 (MSB)	RD/$\overline{WR}$	When low, a write function takes place to the selected register, while if the RD/$\overline{WR}$ bit is set high, this initiates a readback sequence of PMU, Alarm, Comparator, System Control or DAC register as determined by address bits.
27	PMU3	Bits PMU3 through PMU0 address each of the PMU channels in the device. If all four of this bits are set to zero, the System Control Register is addressed.
26	PMU2	
25	PMU1	
24	PMU0	

B27	B26	B25	B24	B23	B22	SELECTED REGISTER			
PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CH3	CH2	CH1	CH0
0	**0**	**0**	**0**	**0**	**0**	**Write to System Control Register**			
0	0	0	1	Select DAC or PMU Registers. See below		×	×	×	CHO
0	0	1	0			×	×	CH1	×
0	0	1	1			×	×	CH1	CH0
0	1	0	0			×	CH2	×	×
-	-	-	-			-	-	-	-
1	0	0	0			CH3	×	×	×
-	-	-	-			-	-	-	-
1	1	1	0			CH3	CH2	CH1	×
1	1	1	1			CH3	CH2	CH1	CH0

23	MODE1	Mode Bits, MODE0 and MODE1 allow addressing of the PMU register or the DAC gain (m), offset (c) or input register (x1). Set to Zero to access the System Control Register.
22	MODE0	

MODE1	MODE0	Action
0	**0**	**System Control Register or PMU Register**
0	1	DAC Gain (m) Register
1	0	DAC Offset (c) Register
1	1	DAC Input Data Register, (x1)

SYSTEM CONTROL REGISTER SPECIFIC BITS		
21	CL3	Clamp Enable. Bits CL3 through CL0 enable and disable the clamp function per channel. A "0" disables, while a "1" enables. The clamp enable function is also available in the PMU register on a per channel basis. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the clamp enable function, what was most recently written to the clamp register is available in the readback word from either PMU or System Control Registers.
20	CL2	
19	CL1	
18	CL0	
17	CPOLH3	Comparator Output Enable. By default the comparator outputs are hi-Z on power on. A "1" in each bit position enables the comparator output for the selected channel. The CPBIASEN (Bit 13) must be enabled to power on the comparator functions. The comparator enable function is also available in the PMU register on a per channel basis. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the comparator enable function, what was most recently written to the comparator register is available in the readback word from either PMU or System Control Registers.
16	CPOLH2	
15	CPOLH1	
14	CPOLH0	
13	CPBIASEN	Comparator Enable. By default the comparators are powered down on power on. To enable the comparator function for all channels, write a "1" to the CPBIASEN bit. A "0" disabled the comparators and shuts them down. Comparator Output Enables bits (CPOLHx) allow the user to switch on each comparator output individually, enabling bussing of comparator outputs.
12	DUTGND/CH	DUTGND per channel enable. The $\overline{GUARDIN(0-3)}$/DUTGND(0-3) pins are shared pin functions and may be configured to enable a DUTGND per PMU channel or GUARD input per PMU channel. Setting this bit to "1" enables DUTGND per channel. In this mode, this pin now functions as a DUTGND pin on a per channel basis. The guard inputs are disconnected from this pin and instead connected directly to the MEASVH line by an internal connection. Default power on condition is GUARDIN(0-3).
11	GUARD ALM	Clamp and Guard Alarm Function share one open drain $\overline{CGALM}$ alarm pin. By default, the $\overline{CGALM}$ pin is disabled. Bits GUARD ALM and CLAMP ALM allow the user to choose if they only wish to have both or either information flagged to the $\overline{CGALM}$ pin. Set high to enable either alarm function.
10	CLAMP ALM	
9	INT10K	Internal Sense Short, INT10K. Setting this bit high allows the user to connect in an internal sense short resistor of 10kΩ between the FOH and the MEASVH lines, (closes SW 7), it also closes SW 15, connecting another 10 kΩ resistor between DUTGND and AGND.

<table>
<tr><td>8</td><td>GUARD EN</td><td>Guard enable. The Guard Amplifier is disabled on power on; write a “1” to enable it. Disabling the guard function if not in use saves power (typically 400µA per Channel).</td></tr>
<tr><td>7</td><td>GAIN1</td><td rowspan="3">MEASOUT Output Range. The MEASOUT range defaults to the voltage force span for voltage and current measurements, this is ±11.25V, which includes some over range to allow for offset correction. The MEASOUT range may be reduced by using the GAIN0 and GAIN1 data bits. This allows for use of asymmetrical supplies and also for use of a smaller input range ADC.
<table>
<tr><td colspan="3">MEASOUT Function</td><td>GAIN1 = “0” V_{REF} = 5V</td><td>GAIN1 = “1”</td></tr>
<tr><td colspan="3"></td><td>MEASOUT Gain = 1</td><td>MEASOUT Gain = 1/5</td></tr>
<tr><td colspan="3">MV</td><td>±VDUT (up to 11.25V)</td><td>$0 \text{ to } \frac{4.5VREF}{5}$</td></tr>
<tr><td rowspan="2">MI</td><td>GAIN0 = “0”</td><td>CURRENT MEAS GAIN = 10</td><td>±V_{RSENSE} X 10 = up to ±11.25V</td><td>0 to 4.5V</td></tr>
<tr><td>GAIN0 = “1”</td><td>CURRENT MEAS GAIN = 5</td><td>± V_{RSENSE} X 5 = up to ±5.625</td><td>0 to 2.25V</td></tr>
</table></td></tr>
<tr><td>6</td><td>GAIN0</td></tr>
<tr><td>5</td><td>TMP ENABLE</td><td rowspan="3">Thermal Shutdown Function, TMP ENABLE, TMP1, TMP0
To disable the Thermal Shutdown feature, write a “0” to the TMP ENABLE bit (enabled by default). Bits TMP1 and TMP0 allow the user to program the thermal shutdown temperature of operation.
<table>
<tr><th>TMP ENABLE</th><th>TMP1</th><th>TMP0</th><th>Action</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>Thermal Shutdown Disabled</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Thermal Shutdown Enabled</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Shutdown at Junction Temp of 130°C (Power On Default)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Shutdown at Junction Temp of 120°C</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Shutdown at Junction Temp of 110°C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Shutdown at Junction Temp of 100°C</td></tr>
</table></td></tr>
<tr><td>4</td><td>TMP1</td></tr>
<tr><td>3</td><td>TMP0</td></tr>
<tr><td>2</td><td>LATCHED</td><td>Configure open drain $\overline{\text{CGALM}}$ as a latched or unlatched output pin. When high, this bit sets the $\overline{\text{CGALM}}$ alarm output as latched outputs allowing it to drive a controller I/O without having to poll the line constantly. Default condition on power on is unlatched.</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Unused bits. Set to 0.</td></tr>
<tr><td>0 (LSB)</td><td>0</td></tr>
</table>

WRITE PMU REGISTER

To address PMU functions, set Mode bits MODE1, MODE0 low, this selects the PMU register as outlined in Table 13 and Table 14. The AD5522 has very flexible addressing, in that it allows writing of data to a single PMU channel, any combination of them or all PMU channels. This enables multi pin broadcasting to similar pins on a DUT. Bits 27 to 24 select which PMU or group of PMUs is addressed.

Table 17. PMU Register Bits

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5 to B0
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CH EN	FORCE1	FORCE0	X	C2	C1	C0	MEAS1	MEAS0	FIN	SF0	SF0	CL	CPOLH	COMPARE V/I	CLEAR	UNUSED DATA BITS

Table 18. PMU Register Functions

Bit	Bit name	Description
28 (MSB)	RD/$\overline{WR}$	When low, a write function takes place to the selected register, while if the RD/$\overline{WR}$ bit is set high, this initiates a readback sequence of PMU, Alarm, Comparator, System Control or DAC register as determined by address bits.
27	PMU3	Bits PMU3 through PMU0 address each of the PMU channels in the device. This allows individual control of each PMU channel or any manner of combined addressing in addition to multi-channel programming.
26	PMU2	
25	PMU1	
24	PMU0	

B27	B26	B25	B24	B23	B22	SELECTED REGISTER			
PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CH3	CH2	CH1	CH0
0	0	0	0	0	0	Write to System Control Register			
0	**0**	**0**	**1**	**Select DAC or PMU Registers.**		×	×	×	**CHO**
0	**0**	**1**	**0**	**See below**		×	×	**CH1**	×
0	**0**	**1**	**1**			×	×	**CH1**	**CH0**
0	**1**	**0**	**0**			×	**CH2**	×	×
-	-	-	-			-	-	-	-
1	**0**	**0**	**0**			**CH3**	×	×	×
-	-	-	-			-	-	-	-
1	**1**	**1**	**0**			**CH3**	**CH2**	**CH1**	×
1	**1**	**1**	**1**			**CH3**	**CH2**	**CH1**	**CH0**

23	MODE1	Mode Bits, MODE0 and MODE1 allow addressing of the PMU register or the DAC gain (m), offset (c) or input register (x1). Set to zero to access the PMU Register.
22	MODE0	

MODE1	MODE0	Action
0	**0**	**System Control Register or PMU Register**
0	1	DAC Gain (m) Register
1	0	DAC Offset (c) Register
1	1	DAC Input Data Register, (x1)

PMU REGISTER SPECIFIC BITS

21	CH EN	Channel Enable, Set high to enable the selected channel, similarly, set low to disable a selected channel or group of channels. When disabled, SW 2 is closed, SW 5 open.
20	FORCE1	Bits FORCE1 and FORCE0 address the force function for each of the PMU channels (in association with P3-P0). All combinations of forcing and measuring (using MEAS0 and MEAS1) are available. The Hi-Z (voltage and current) modes allows user to optimize glitch response during mode changes. While in these modes, with PMU Hi-Z, new x1 codes loaded to the FIN DAC register and the Clamp DAC register will be calibrated, stored in x2 register and loaded directly to the DAC outputs.
19	FORCE0	

FORCE1	FORCE0	Action
0	0	FV & Current Clamp (if clamp enabled)
0	1	FI & Voltage Clamp (if clamp enabled)
1	0	Hi-Z FOH Voltage (pre load FIN DAC & Clamp DAC)
1	1	Hi-Z FOH Current (pre load FIN DAC & Clamp DAC)

18	RESERVED	0
17	C2	Bits C2 through C0 address allow selection of the required current range.
16	C1	
15	C0	

C2	C1	C0	Action
0	0	0	±5µA current range
0	0	1	±20µA current range
0	1	0	±200µA current range
0	1	1	±2mA current range
1	0	0	±external current range
1	0	1	NOP
1	1	0	NOP
1	1	1	NOP

<table>
<tr><td>14</td><td>MEAS1</td><td rowspan="2">Bits MEAS1 and MEAS0 allow selection of the required measure mode, allowing the measout line to be disabled, connected to the temperature sensor or enabled for measurement or current or voltage.
<table>
<tr><th>MEAS1</th><th>MEAS0</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>MEASOUT connected to I SENSE</td></tr>
<tr><td>0</td><td>1</td><td>MEASOUT connected to V SENSE</td></tr>
<tr><td>1</td><td>0</td><td>MEASOUT connected to Temperature Sensor</td></tr>
<tr><td>1</td><td>1</td><td>MEASOUT Hi-Z (SW 12 Open)</td></tr>
</table></td></tr>
<tr><td>13</td><td>MEAS0</td></tr>
<tr><td>12</td><td>FIN</td><td>Bit FIN = 0 switches the input of the force amplifier to GND, while FIN = 1 connects it to FIN DAC output.</td></tr>
<tr><td>11</td><td>SFO</td><td rowspan="2">Bits SF0 through SS0 address each of the different combinations of switching the system force and sense lines to the force and sense at the DUT. Selection of which channel the system force and sense lines are connected to as per P3 to P0 addressing.
<table>
<tr><th>SF0</th><th>SS0</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>SYS_FORCE and SYS_SENSE Hi-Z</td></tr>
<tr><td>0</td><td>1</td><td>SYS_FORCE Hi-Z, SYS_SENSE connected to MEASVHx</td></tr>
<tr><td>1</td><td>0</td><td>SYS_FORCE connected to FOHx, SYS_SENSE Hi-Z</td></tr>
<tr><td>1</td><td>1</td><td>SYS_FORCE connected to FOHx, SYS_SENSE connected to MEASVHx</td></tr>
</table></td></tr>
<tr><td>10</td><td>SSO</td></tr>
<tr><td>9</td><td>CL</td><td>Per PMU clamp enable bit. A logic high enables the clamp function for the selected PMU. The clamp enable function is also available in the System control register. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the clamp enable function on a per channel basis, what was most recently written to the clamp register is available in the readback word from either PMU or System Control Registers.</td></tr>
<tr><td>8</td><td>CPOLH</td><td>Comparator output enable bit. A logic high enables the comparator output for the selected PMU, the comparator function CPBIASEN must be enabled in the SYSTEM CONTROL REGISTER. The comparator output enable function is also available in the System control register. This dual functionality allows flexible enable or disabling of this function.</td></tr>
<tr><td>7</td><td>COMPARE V/I</td><td>A logic high selects compare voltage function, while logic low, current function.</td></tr>
<tr><td>6</td><td>CLEAR</td><td>To clear or reset a latched alarm bit and pin (temperature, guard or clamp), load a “1” to the Clear bit position. This bit applies to latched alarm (clamp and guard) conditions on all four PMU channels.</td></tr>
<tr><td>5</td><td>0</td><td rowspan="6">Unused bits. Set to 0.</td></tr>
<tr><td>4</td><td></td></tr>
<tr><td>3</td><td></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>1</td><td></td></tr>
<tr><td>0 (LSB)</td><td></td></tr>
</table>

WRITE DAC REGISTER

The DAC input, gain and offset registers are addressed through a combination of PMU bits (Bits 27 through 24) and MODE bits (Bits 23 and 22). Bits A5 through A0 address each of the DAC levels on chip. D15 through D0 are the DAC data Bits when writing to these registers. PMU address bits allow addressing to DAC across any combination of PMU channels.

Table 19. DAC Register Bits

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15 to B0
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	A5	A4	A3	A2	A1	A0	DATA BITS D15 (MSB to D0 (LSB)

Table 20. DAC Register Functions

Bit	Bit name	Description
28 (MSB)	RD/$\overline{WR}$	When low, a write function takes place to the selected register, while if the RD/$\overline{WR}$ bit is set high, this initiates a readback sequence of PMU, Alarm, Comparator, System Control or DAC register as determined by address bits.
27	PMU3	Bits PMU3 through PMU0 address each of the PMU and DAC channels in the device. This allows individual control of each DAC channel or any manner of combined addressing in addition to multi-channel programming.
26	PMU2	
25	PMU1	
24	PMU0	
23	MODE1	Mode Bits, MODE0 and MODE1 allow addressing of the DAC gain (m), offset (c) or input register (x1)
22	MODE0	
DAC REGISTER SPECIFIC BITS		
21,20,19	A5,A4,A3	DAC Address Bits. A5 to A3 select which register set is addressed. See Table 21
18,17,16	A2,A1,A0	DAC Address Bits, A2 to A0 select which DAC is addressed. See Table 21
15 to 0(LSB)	D15 (MSB) to D0(LSB)	16 DAC Data bits. D15 MSB.

B27	B26	B25	B24	B23	B22	SELECTED REGISTER			
PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CH3	CH2	CH1	CH0
0	0	0	0	0	0	Write to System Control Register			
0	**0**	**0**	**1**	**Select DAC or PMU Registers.**		×	×	×	**CHO**
0	**0**	**1**	**0**	**See below**		×	×	**CH1**	×
0	**0**	**1**	**1**			×	×	**CH1**	**CH0**
0	**1**	**0**	**0**			×	**CH2**	×	×
-	-	-	-			-	-	-	-
1	**0**	**0**	**0**			**CH3**	×	×	×
-	-	-	-			-	-	-	-
1	**1**	**1**	**0**			**CH3**	**CH2**	**CH1**	×
1	**1**	**1**	**1**			**CH3**	**CH2**	**CH1**	**CH0**

MODE1	MODE0	Action
0	0	System Control Register or PMU Register
0	**1**	**DAC Gain (m) Register**
1	**0**	**DAC Offset (c) Register**
1	**1**	**DAC Input Data Register, (x1)**

DAC Addressing

For the FIN and Comparator (CPH & CPL) DACs, there are sets of x1, m and c registers for each current range and for the voltage range, but only two sets for the Clamp function (CLL and CLH).

When calibrating the device, m and c registers allow volatile storage of offset and gain coefficients. Calculation of the corresponding DAC x2 register only occurs when x1 data is loaded (no internal calculation occurs on m or c updates).

There is one Offset DAC per all four channels in the device, it is addressed through any PMU0-3 address. The Offset DAC only has an input register associated with it; there are no m or c registers for this DAC. When writing to this DAC, set both Mode bits high to address the DAC input register (x1).

This address table is also used for readback of a particular DAC address.

Table 21. DAC Register Addressing

			Address bits A5 to A3 (DAC ADDRESS Register)								
		Register Set	**000**			**001**	**010**	**011**	**100**	**101**	**110**	**111**
A2 to A0 (REGISTER ADDRESS)			**MODE1**	**MODE0**								
			0	1	*RESERVED*							
			1	0	*RESERVED*							
	000	±5µA I range	1	1	**OFFSET DAC**	**FIN**	*RESERVED*	*RESERVED*	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	001	±20µA I range	*RESERVED*			**FIN**	*RESERVED*	*RESERVED*	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	010	±200µA I range	*RESERVED*			**FIN**	*RESERVED*	*RESERVED*	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	011	±2mA I range	*RESERVED*			**FIN**	*RESERVED*	*RESERVED*	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	100	±external I range	*RESERVED*			**FIN**	**CLL I[1]**	**CLH I[1]**	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	101	Voltage range	*RESERVED*			**FIN**	**CLL V[2]**	**CLH V[2]**	**CPL**	**CPH**	*RESERVED*	*RESERVED*
	110	*RESERVED*	*RESERVED*			*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*
	111	*RESERVED*	*RESERVED*			*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*	*RESERVED*

[1] CLL I = Clamp Level Low Current register. CLH I = Clamp Level High Current Register. When forcing a voltage, current clamps are engaged, so this register set will be loaded to the Clamp DAC.
[2] CLL V = Clamp Level Low Voltage register. CLH V = Clamp Level High Voltage Register. When forcing a current, voltage clamps are engaged, so this register set will be loaded to the Clamp DAC.

READ REGISTERS

Readback of all the registers in the device is possible via the both SPI and LVDS interfaces. In order to readback data from a register, it is first necessary to write a "readback" command to tell the device which register is required to readback. See Table 22 to address the appropriate channel.

Table 22. Read Functions of the AD5522

B28	B27	B26	B25	B24	B23	B22	B21 to B0	SELECTED REGISTER			
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	DATA BITS	CH3	CH2	CH1	CH0
READ FUNCTIONS											
1	0	0	0	0	0	0	All zeros	Read from System Control Register			
1	0	0	0	0	0	1	All zeros	Read from Comparator Status Registers			
1	0	0	0	0	1	0	X	Reserved			
1	0	0	0	0	1	1	All zeros	Read from Alarm Status Register			
READ ADDRESSED PMU REGISTER – ONLY ONE PMU REGISTER CAN BE READ AT ONE TIME											
1	0	0	0	1	0	0	All zeros	×	×	×	CH0
1	0	0	1	0	0	0		×	×	CH1	×
1	0	1	0	0	0	0		×	CH2	×	×
1	1	0	0	0	0	0		CH3	×	×	×
READ ADDRESSED DAC "m" Register – ONLY ONE DAC REGISTER CAN BE READ AT ONE TIME											
1	0	0	0	1	0	1	DAC ADDRESS	×	×	×	CH0
1	0	0	1	0	0	1	SEE Table 21	×	×	CH1	×
1	0	1	0	0	0	1		×	CH2	×	×
1	1	0	0	0	0	1		CH3	×	×	×
READ ADDRESSED DAC "c" Register – ONLY ONE DAC REGISTER CAN BE READ AT ONE TIME											
1	0	0	0	1	1	0	DAC ADDRESS	×	×	×	CH0
1	0	0	1	0	1	0	SEE Table 21	×	×	CH1	×
1	0	1	0	0	1	0		×	CH2	×	×
1	1	0	0	0	1	0		CH3	×	×	×
READ ADDRESSED DAC "x1" Register – ONLY ONE DAC REGISTER CAN BE READ AT ONE TIME											
1	0	0	0	1	1	1	DAC ADDRESS	×	×	×	CH0
1	0	0	1	0	1	1	SEE Table 21	×	×	CH1	×
1	0	1	0	0	1	1		×	CH2	×	×
1	1	0	0	0	1	1		CH3	×	×	×

Once the required channel has been addressed, the device will load the 24 bit Readback data into the MSB positions of the 29 Bit serial shift register, the five LSB bits will be filled with zeros. SCLK rising edges clock this readback data out on SDO(framed by the $\overline{SYNC}$ signal).

A minimum of 24 clock rising edges are required to shift the readback data out of the shift register. If writing a 24-bit word to shift data out of the device, user must ensure that the 24 bit write is effectively a NOP (No Operation) command. The last 5 bits in the shift register will always be 00000b, these five bits will become the MSBs of the shift register when the 24 bit write is loaded. To ensure the device receives a NOP command as outlined in Table 14, the recommended flush command is 0xFFFFFF and no change will be made to any register within the device.

Readback data may also be shifted out by writing another 29 bit write or read command. If writing a 29-bit command, the readback data will be MSB data available on SDO, followed by 00000b.

READBACK OF SYSTEM CONTROL REGISTER

The readback function is a 24 bit word, mode, address and System Control Register data bits as shown in the following table.

Table 23. Readback System Control Register Data

Bit	Bit name	Description
23 (MSB)	MODE1	0
22	MODE0	0
SYSTEM CONTROL REGISTER SPECIFIC READBACK BITS		
21	CL3	Readback the status of the individual Clamp Enable bits. A "0" means the clamp is disabled, while a "1" enabled. The clamp enable function is also available in the System Control Register. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the clamp enable function, what was most recently written to the clamp register from either System Control register or PMU register will be available in the readback word.
20	CL2	
19	CL1	
18	CL0	
17	CPOLH3	Readback information on the Comparator Output Enable status. A "1" signifies the function is enabled, while a "0" disabled. A logic high indicates that the PMU comparator output is enabled, while if low, it's disabled. The comparator output enable function is also available in the PMU Register. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the comparator output enable function, what was most recently written to the comparator register from either System Control register or PMU register will be available in the readback word.
16	CPOLH2	
15	CPOLH1	
14	CPOLH0	
13	CPBIASEN	This readback bit tells the status of the Comparator Enable function. A "1" in this bit position means the Comparator functions are enabled, while a "0" disabled.
12	DUTGND/CH	DUTGND per channel enable. If this bit is set at "1", DUTGND per channel is enabled, while if "0", individual guard inputs are available per channel.
11	GUARD ALM	These bits give status on which of these alarm bits trigger the $\overline{\text{CGALM}}$ pin.
10	CLAMP ALM	
9	INT10K	If this bit is set high, the internal 10k resistor is connected between FOH and MEASVH, and between DUTGND and AGND. If low, they are disconnected.
8	GUARD EN	Readback status of the Guard amplifies. If high, Amplifiers are enabled.
7	GAIN1	Status of the selected MEASOUT Output Range.
6	GAIN0	
5	TMP ENABLE	Information is available on the status of the setting for Thermal shutdown function. Refer to System control write register.
4	TMP1	
3	TMP0	
2	LATCHED	This bit tells of the status of the open drain outputs. When high, the open drain alarm outputs are latched outputs, while if low, they are unlatched.
1	Unused Readback bits	Will be loaded with zeros.
0 (LSB)		

READBACK OF PMU REGISTER

The PMU readback function is a 24 bit word, mode, address and PMU data bits.

Table 24. Readback PMU Register (Only one PMU register may be read back at any one time).

Bit	Bit name	Description
23 (MSB)	MODE1	0
22	MODE0	0
PMU REGISTER SPECIFIC BITS		
21	CH EN	Channel Enable, If high selected channel is enabled, otherwise disabled.
20	FORCE1	These bits tell what force and measure mode the selected channel is in.
19	FORCE0	
18	RESERVED	0
17	C2	These three bits tell what forced or measured current range is set for the selected channel.
16	C1	
15	C0	
14	MEAS1	Bits MEAS1 and MEAS0 tell which measure mode is selected, voltage, current, temperature sensor or Hi-Z.
13	MEAS0	
12	FIN	This bit shows the status of the Force input amplifier.
11	SFO	The system force and sense lines may be connected to any of the four PMU channels. Reading back these bits tell if they are switched in or not.
10	SSO	
9	CL	A logic high in this readback position tells if the Per PMU clamp is enabled, while if low, the clamp is disabled. The clamp enable function is also available in the System Control Register. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the clamp enable function, what was most recently written to the clamp register from either System Control register or PMU register will be available in the readback word.
8	CPOLH	A logic high indicates that the PMU comparator output is enabled, while if low, it's disabled. The comparator output enable function is also available in the System Control Register. This dual functionality allows flexible enable or disabling of this function. When reading back information on the status of the comparator output enable function, what was most recently written to the comparator register from either System Control register or PMU register will be available in the readback word.
7	COMPARE V/I	A logic high selects indicates the selected channel is comparing voltage function, while logic low, current function.
6	$\overline{\text{LTMPALM}}$	$\overline{\text{TMPALM}}$ corresponds to the open drain $\overline{\text{TMPALM}}$ output pin which flags the user of a temperature event exceeding the default or user programmed level. The temperature alarm is a per device alarm, and latched ($\overline{\text{LTMPALM}}$) and unlatched ($\overline{\text{TMPALM}}$) bits tell a temperature event occurred and if the alarm still exists (if the junction temperature still exceeds the programmed alarm level). To reset an alarm event, the user must write to the CLEAR bit in the PMU register.
5	$\overline{\text{TMPALM}}$	
4, 3, 2, 1, 0 (LSB)	Unused Readback bits	Will be loaded with zeros.

READBACK OF COMPARATOR STATUS REGISTER

The Comparator output status Register is a read only register giving access to the output status of each of the comparators on the chip. Table 25 shows the format of the comparator readback word.

Table 25. Comparator Status Readback Register

Bit	Bit name	Description
23 (MSB)	MODE1	0
22	MODE0	1
COMPARATOR STATUS REGISTER SPECIFIC BITS		
21	CP0L0	Comparator output conditions per channel corresponding to the comparator output pins.
20	CP0H0	
19	CP0L1	
18	CP0H1	
17	CP0L2	
16	CP0H2	
15	CP0L3	
14	CP0H3	
13 to 0 (LSB)	Unused Readback bits	Will be loaded with zeros.

READBACK OF ALARM STATUS REGISTER

The Alarm Status register is a READ only register that gives information on temperature, clamp and guard alarm events. In the event the Guard and Clamp alarm functions are not used, (the alarm function may be switched off in the System Control Register). In this case, the Temperature alarm status is also available in the contents of any of the four PMU readback registers.

Table 26. Alarm Status Readback Register

Bit	Bit name	Description
23 (MSB)	MODE1	1
22	MODE0	1
ALARM STATUS READBACK REGISTER SPECIFIC BITS		
21	$\overline{\text{LTMPALM}}$	$\overline{\text{TMPALM}}$ corresponds to the open drain $\overline{\text{TMPALM}}$ output pin which flags the user of a temperature event exceeding the default or user programmed level. The temperature alarm is a per device alarm, and latched ($\overline{\text{LTMPALM}}$) and unlatched ($\overline{\text{TMPALM}}$) bits tell a temperature event occurred and if the alarm still exists (if the junction temperature still exceeds the programmed alarm level). To reset an alarm event, the user must write to the CLEAR bit in the PMU register.
20	$\overline{\text{TMPALM}}$	
19	$\overline{\text{LG0}}$	$\overline{\text{LGx}}$ is the per channel latched Guard Alarm bit and $\overline{\text{Gx}}$ is an unlatched alarm bit. These bits give information on which channel flagged an alarm on the open drain alarm $\overline{\text{CGALM}}$ pin and if the alarm condition still exists.
18	$\overline{\text{G0}}$	
17	$\overline{\text{LG1}}$	
16	$\overline{\text{G1}}$	
15	$\overline{\text{LG2}}$	
14	$\overline{\text{G2}}$	
13	$\overline{\text{LG3}}$	
12	$\overline{\text{G3}}$	
11	$\overline{\text{LC0}}$	$\overline{\text{LCx}}$ is a per channel latched Clamp alarm bit and $\overline{\text{Cx}}$ is the unlatched alarm bit. These bits give information on which channel flagged an alarm on the open drain alarm $\overline{\text{CGALM}}$ pin and if the alarm condition still exists.
10	$\overline{\text{C0}}$	
9	$\overline{\text{LC1}}$	
8	$\overline{\text{C1}}$	
7	$\overline{\text{LC2}}$	
6	$\overline{\text{C2}}$	
5	$\overline{\text{LC3}}$	
4	$\overline{\text{C3}}$	
3 to 0 (LSB)	Unused Readback bits	Will be loaded with zeros.

READBACK OF DAC REGISTER

The DAC readback function is a 24 bit word, mode, address and DAC data bits.

Table 27. DAC Register Readback

Bit	Bit name	Description
23 (MSB)	MODE1	0
22	MODE0	0
DAC READBACK REGISTER SPECIFIC BITS		
21 to 16	A5, A4, A3, A2, A1	Address Bits indicating the DAC register that is read.
15 to 0 (LSB)	D15 to D0	Contents of the addressed DAC register (x1, m or c).

POWER ON DEFAULT

The power on default for all DAC channels is that the contents of each m register is set to full-scale (0xFFFF) and c register to midscale(0x8000). The contents of the DAC registers are :

Offset DAC: 0xA492, FIN DACs: 0x8000, CLL DACs: 0x0000, CLH DACs: 0xFFFF, CPL DACs: 0x0000, CPH DACs: 0xFFFF

The power on defaults of the PMU register and the System Control Register are shown below.

Table 28. Power on Default for System Control Register and PMU Register

	SYSTEM CONTROL REGISTER POWER ON DEFAULT			PMU REGISTER POWER ON DEFAULT	
Bit	**Bit name**	**Description**		**Bit name**	**Description**
21 (MSB)	CL3	0		CH EN	0
20	CL2	0		FORCE1	0
19	CL1	0		FORCE0	0
18	CL0	0		RESERVED	0
17	CPOLH3	0		C2	0
16	CPOLH2	0		C1	1
15	CPOLH1	0		C0	1
14	CPOLH0	0		MEAS1	1
13	CPBIASEN	0		MEAS0	1
12	DUTGND/CH	0		FIN	0
11	GUARD ALM	0		SFO	0
10	CLAMP ALM	0		SSO	0
9	INT10K	0		CL	0
8	GUARD EN	0		CPOLH	0
7	GAIN1	0		COMPARE V/I	0
6	GAIN0	0		$\overline{\text{LTMPALM}}$	1
5	TMP ENABLE	1		$\overline{\text{TMPALM}}$	1
4	TMP1	0		Unused Data Bits	0
3	TMP0	0			0
2	LATCHED	0			0
1	Unused Data Bits	0			0
0 (LSB)		0			0

SETTING UP THE DEVICE ON POWER ON

On power on, default conditions are recalled from the power on reset register ensuring each PMU and DAC channel is powered up to a known condition. To operate the device, the user must:

1) Configure the device by writing to the System Control register to set up different functions as required.

2) Calibrate out errors and load required calibration values to (Gain) m and (Offset) c registers, and load codes to each DAC input register (x1). Once x1 values are loaded to the individual DACs, the calibration engine calculates the appropriate x2 value and stores it ready for the PMU address to call it.

3) Load the required PMU channel with the required force mode, current range etc. Loading the PMU channel configures the switches around the Force Amplifier, Measure function, clamps and comparators and also acts as a load signal for the DACs, loading the DAC register with the appropriate stored x2 value.

4) As the voltage and current ranges have individual DAC registers associated with them, each PMU register mode of operation calls a particular x2 register. Hence, only updates (changes to x1 register) to DACs associated with the selected mode of operation are reflected to the output of the PMU. If there is a change to the x1 value associated with a different PMU mode of operation, then this x1 value and it's m and c coefficients are used to calculate a corresponding x2 value which is stored in the correct x2 register, but it does not get loaded to the DAC.

CHANGING MODES

There are different ways of handling a mode change:

1) Load any DAC x1 values that are required to change. Remember that x1 registers are available per voltage and current range (for Force Amplifier and Comparator DACs), so you can preload these and may not need to make changes. The calibration engine will calculate the x2 values and store them.

2) Now change into the new PMU mode. This will load the new switch conditions in the PMU circuitry and load the DAC register with the stored x2 data.

or

1) Use the Hi-Z V or Hi-Z I mode in the PMU register, this makes the amplifier high impedance.

2) Now load any DAC x1 values that need to be loaded. Remember that x1 registers are available per voltage and current range, so you can preload these and may not need to make changes.

3) When the Hi-Z (V or I) modes are used, the relevant DAC outputs are automatically updated (FIN, CLL, CLH DACs). For example, when selecting Hi-Z V (Voltage), the FIN Voltage x2 result is loaded, offset and gain corrected, cached and loaded to the FIN DAC. When forcing a voltage, current clamps are engaged, so the CLL I (Current) register can be loaded, gain and offset corrected and loaded to the DAC register. Similarly, for the CLH I register.

4) Now change into the new PMU mode (FI/FV). This will load the new switch conditions in the PMU circuitry. As the DAC outputs are already loaded, transients when changing current or voltage mode will be minimized.

REQUIRED EXTERNAL COMPONENTS

The minimum required external components are shown in the block diagram below. Decoupling will be very dependent on the type of supplies used, other decoupling on the board and the noise in the system. It is possible more or less decoupling may be required as a result.

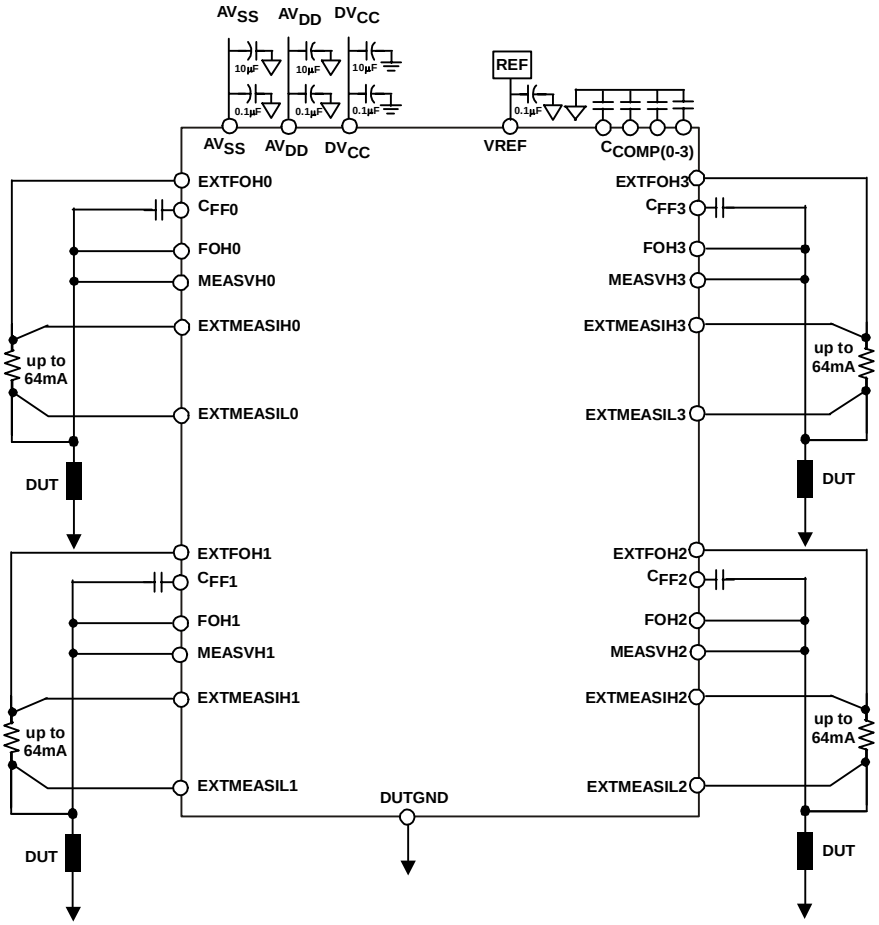


Figure 19. External components required for use with this PMU device.

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5522 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5522 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (AV_{SS}, AV_{DD}, V_{CC}), it is recommended to tie these pins together and to decouple each supply once.

The AD5522 should have ample supply decoupling of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided, because these couple noise onto the device. The analog ground plane should be allowed to run under the AD5522 to avoid noise coupling (only with the package with paddle up).. The power supply lines of the AD5522 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. It is essential to minimize noise on all V_{REF} lines. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

Also note that the exposed paddle of the AD5522 is connected to the negative supply AV_{SS}.

TYPICAL APPLICATION FOR THE AD5522

Figure 20 shows the AD5522 as used in an ATE system. This device can used as a per pin parametric unit in order to speed up the rate at which testing can be done.

The central PMU shown in the block diagram is usually a highly accurate PMU, and is shared among a number of pins in the tester. In general, many discrete levels are required in an ATE system for the pin drivers, comparators, clamps, and active loads. DAC devices, such as the AD5379, offer a highly integrated solution for a number of these levels. The AD5379 is a dense 40-channel DAC designed with high channel requirements, such as ATE

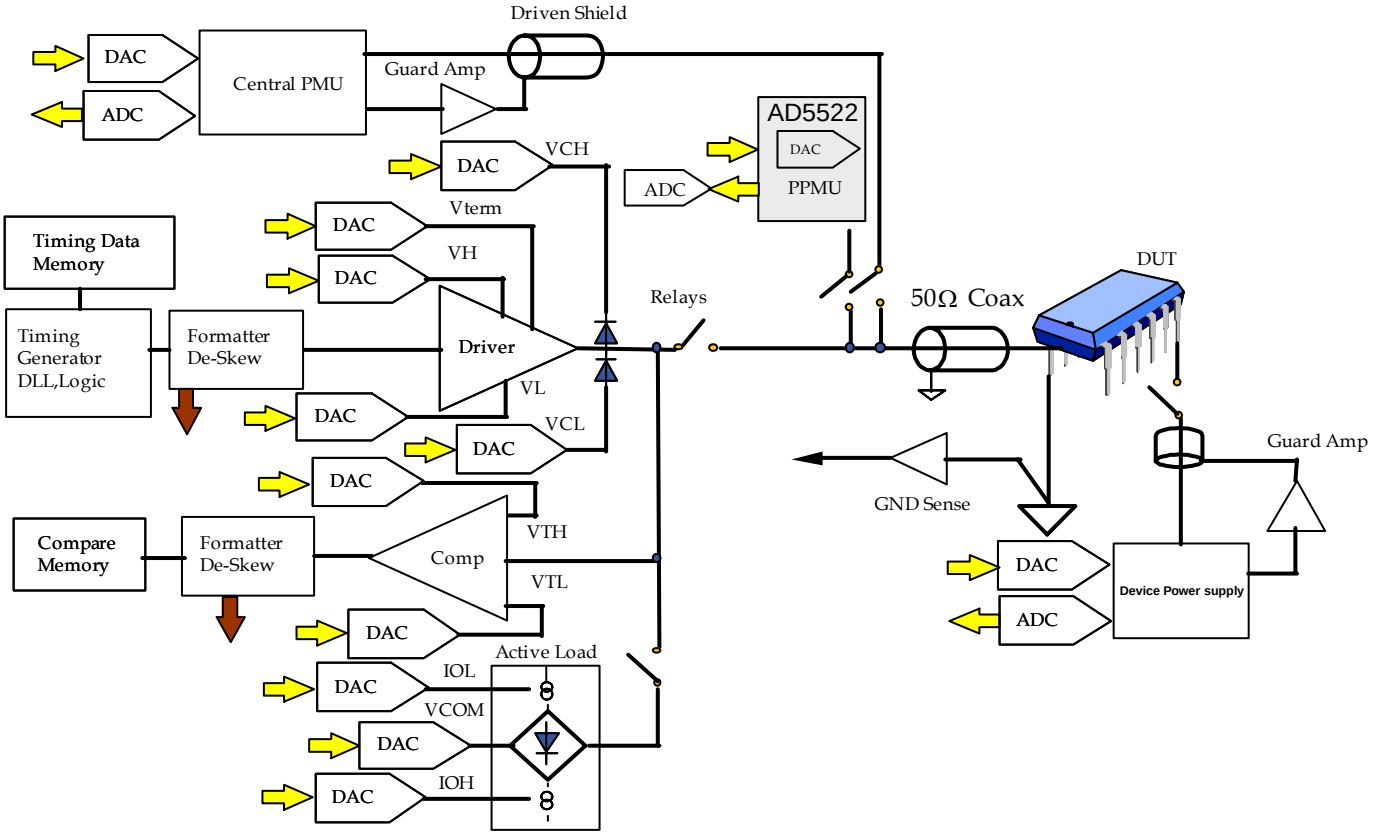
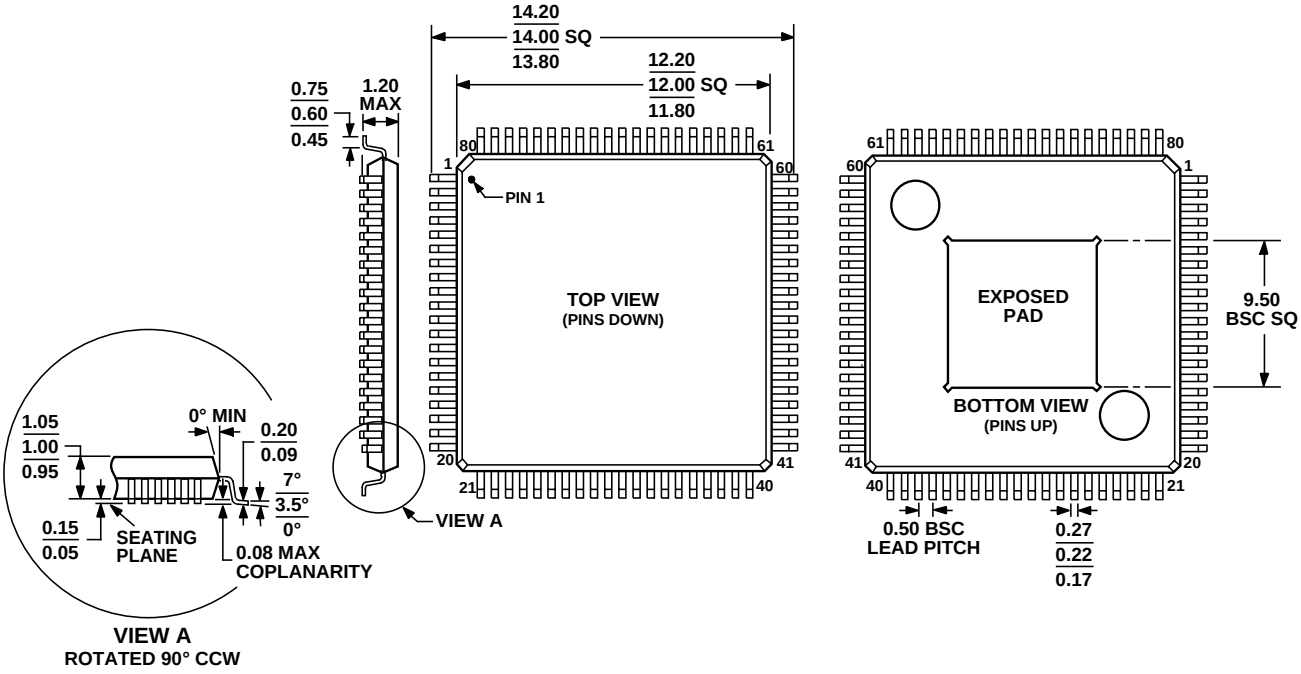


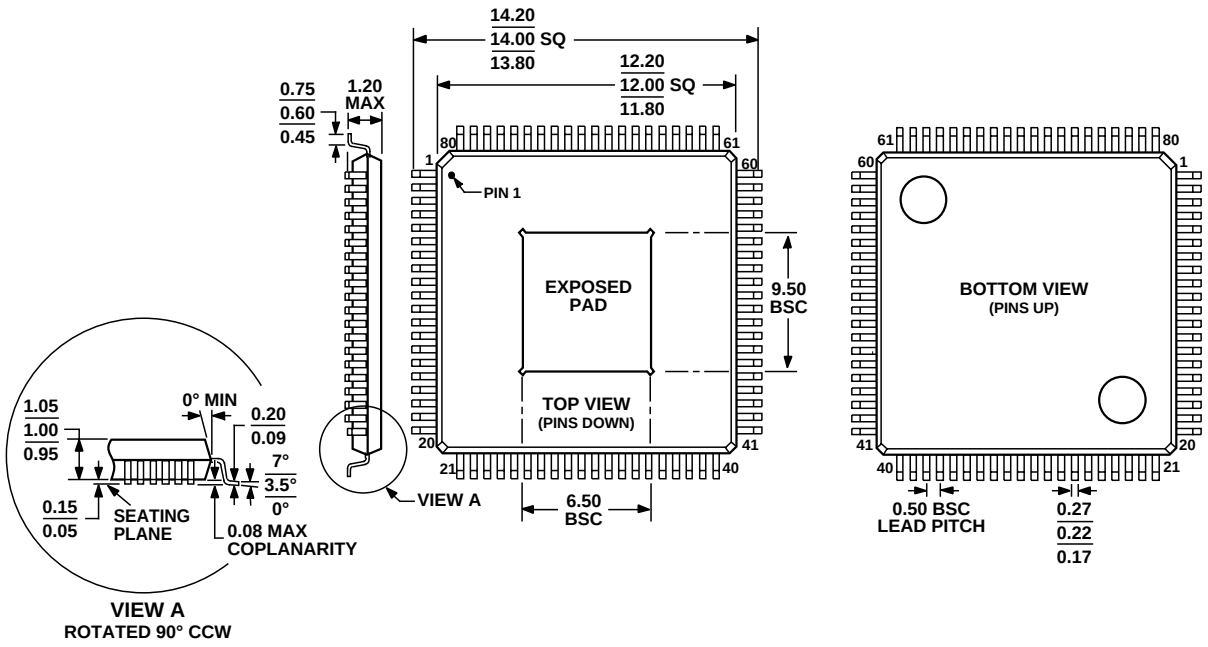
Figure 20. Typical Applications Circuit using the AD5522 as a per pin parametric unit.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HD

Figure 21. 80 lead TQFP/EP with exposed pad on bottom



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HU

Figure 22. 80 lead TQFP/EP with exposed pad on top

ORDERING GUIDE

Model	Function	Package Description[1]	Package Options
AD5522JSVDZ[2]	Quad PMU with 4 internal current ranges, full comparator function, 1 external current range, SPI and LVDS serial interfaces.	80 Lead TQFP with exposed pad on bottom	SV-80
AD5522JSVUZ[Error! Bookmark not defined.]	Quad PMU with 4 internal current ranges, full comparator function, 1 external current range, SPI and LVDS serial interfaces.	80 Lead TQFP with exposed pad on top	SV-80
AD5523JCPZ[Error! Bookmark not defined.],[3]	Quad PMU, 4 internal current ranges, window comparator function, SPI interface.	64 Lead LFCSP with exposed pad on bottom 9mm x 9mm	CP-64

[1] Exposed pad is tied to AV_{SS}.
[2] Lead Free.
[3] Reduced functionality. Contact factory for AD5523 datasheet and more details..

NOTES

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