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AD8568/AD8569/AD8570—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_S ≤ 16 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}			2	10	mV
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C ≤ T _A ≤ +85°C		5		μV/°C
Input Bias Current	I _B	−40°C ≤ T _A ≤ +85°C		80	600	nA
					800	nA
Input Voltage Range			−0.5		V _S + 0.5	V
Input Impedance	Z _{IN}			400		kΩ
Input Capacitance	C _{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	I _L = 100 μA V _S = 16 V, I _L = 5 mA −40°C ≤ T _A ≤ +85°C	15.85 15.75	V _S − 0.005 15.95		V V V
		V _S = 4.5 V, I _L = 5 mA −40°C ≤ T _A ≤ +85°C	4.2 4.1	4.38		V V
Output Voltage Low	V _{OL}	I _L = 100 μA V _S = 16 V, I _L = 5 mA −40°C ≤ T _A ≤ +85°C		5 42		mV mV
		V _S = 4.5 V, I _L = 5 mA −40°C ≤ T _A ≤ +85°C			150 250	mV mV
				95	300	mV
Continuous Output Current	I _{OUT}	−40°C ≤ T _A ≤ +85°C			400	mV
Peak Output Current	I _{PK}	V _S = 16 V		35 250		mA mA
TRANSFER CHARACTERISTICS						
Gain	A _{VCL}	R _L = 2 kΩ −40°C ≤ T _A ≤ +85°C	0.995 0.995	0.9985 0.9980	1.005 1.005	V/V V/V
Gain Linearity	NL	R _L = 2 kΩ, V _O = 0.5 to (V _S − 0.5 V)		0.01		%
POWER SUPPLY						
Supply Voltage	V _S		4.5		16	V
Power Supply Rejection Ratio	PSRR	V _S = 4 V to 17 V −40°C ≤ T _A ≤ +85°C	70	90		dB
Supply Current/Amplifier	I _{SY}	V _O = V _S /2, No Load −40°C ≤ T _A ≤ +85°C		700	850 1	μA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 10 kΩ, C _L = 200 pF	4	6		V/μs
Bandwidth	BW	−3 dB, R _L = 10 kΩ, C _L = 10 pF		6		MHz
Phase Margin	Ø _o	R _L = 10 kΩ, C _L = 10 pF		65		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e _n	f = 1 kHz		26		nV/√Hz
	e _n	f = 10 kHz		25		nV/√Hz
Current Noise Density	i _n	f = 10 kHz		0.8		pA/√Hz

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S)	18 V
Input Voltage	-0.5 V to $V_S + 0.5$ V
Differential Input Voltage	V_S
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA} ¹	θ_{JC}	Ψ_{JB} ²	Unit
6-Lead SOT-23 (RT)	250	140		°C/W
10-Lead MSOP (RM)	200	44		°C/W
32-Lead LFCSP (CP)	35		13	°C/W

NOTES

¹ θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered onto a circuit board for surface mount packages.

² Ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

ORDERING GUIDE

Model*	Temperature Range	Package Description	Package Option	Branding Information
AD8568ART	-40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8569ARM	-40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8570ACP	-40°C to +85°C	32-Lead LFCSP	CP-32	

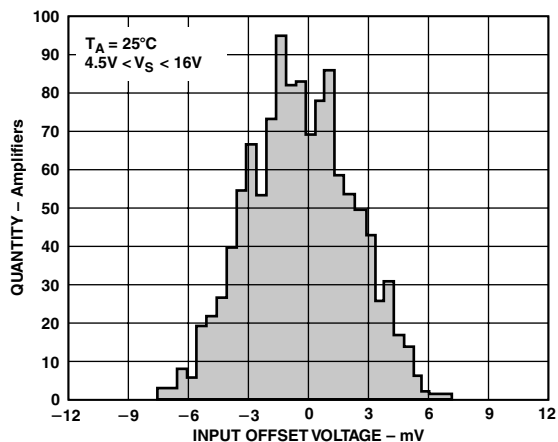
*Available in reels only.

CAUTION

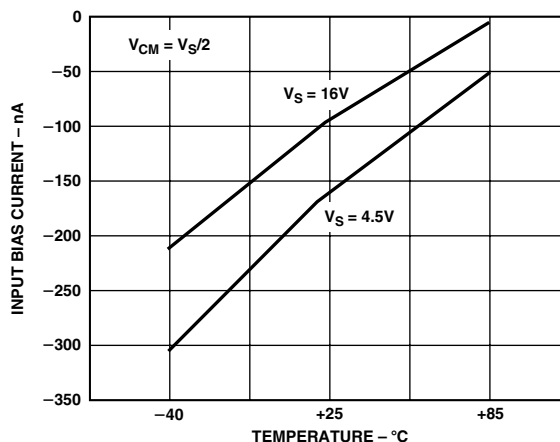
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8568/AD8569/AD8570 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



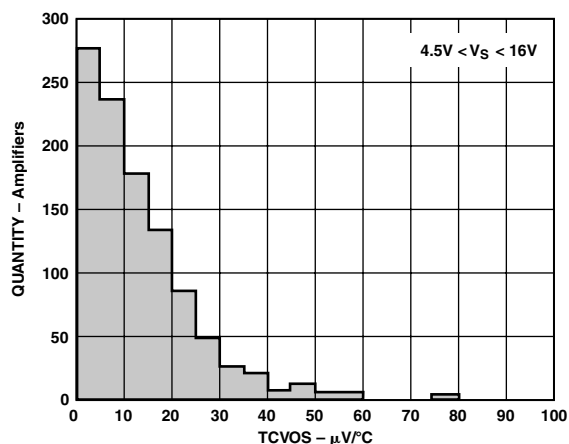
AD8568/AD8569/AD8570—Typical Performance Characteristics



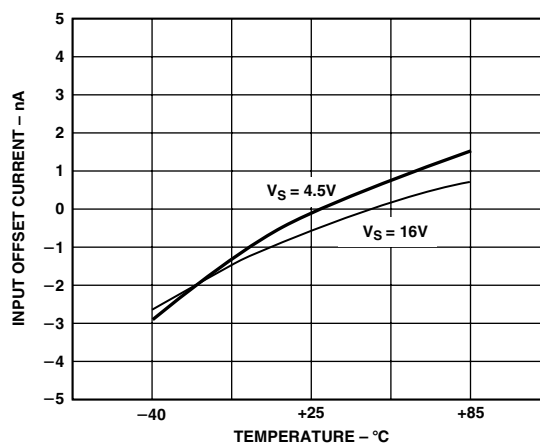
TPC 1. Input Offset Voltage Distribution



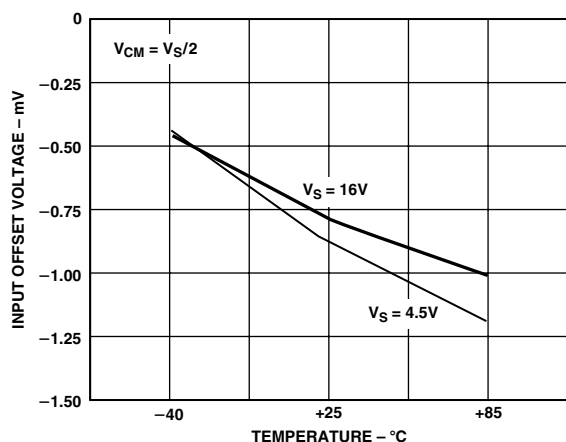
TPC 4. Input Bias Current vs. Temperature



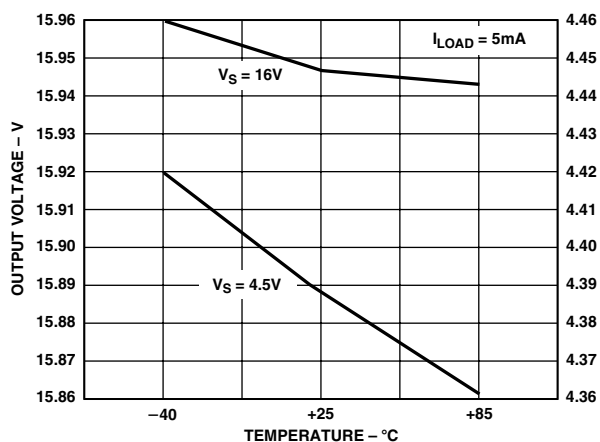
TPC 2. Input Offset Voltage Drift Distribution



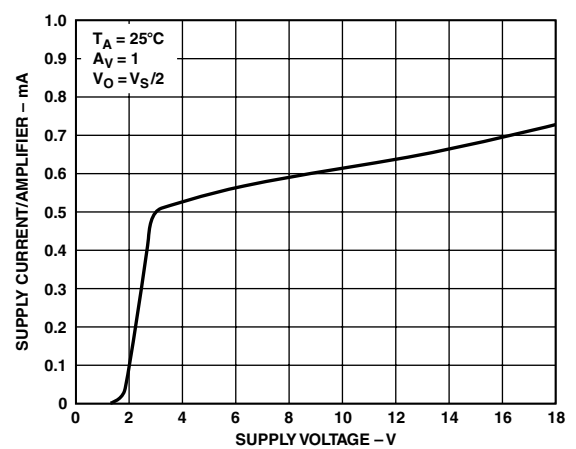
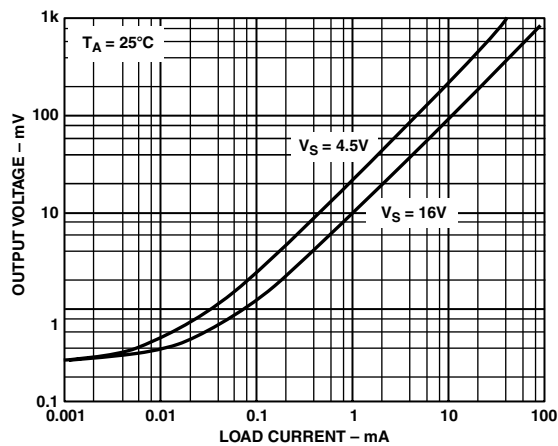
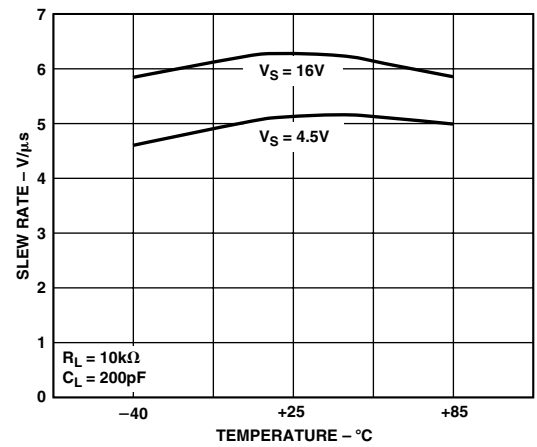
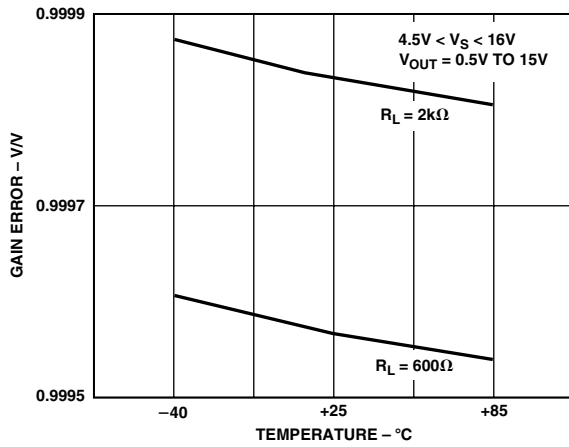
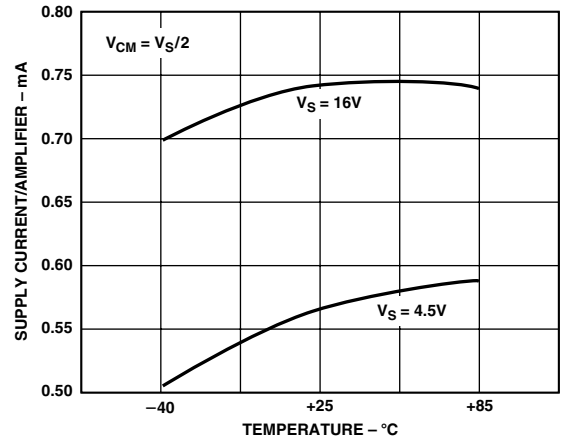
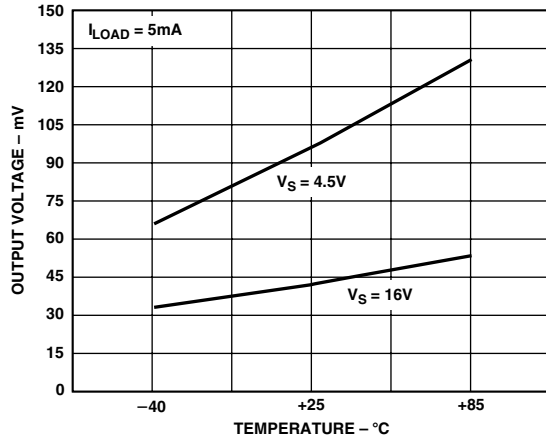
TPC 5. Input Offset Current vs. Temperature



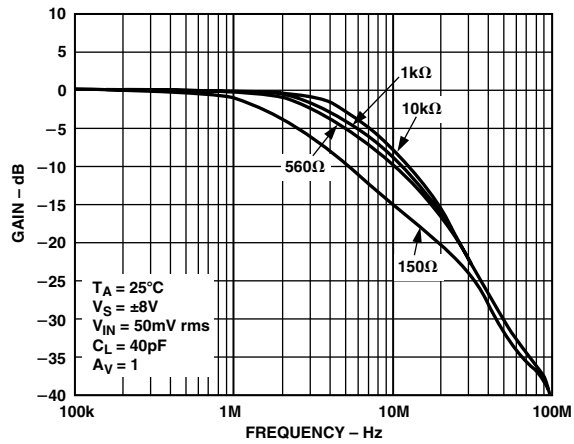
TPC 3. Input Offset Voltage vs. Temperature



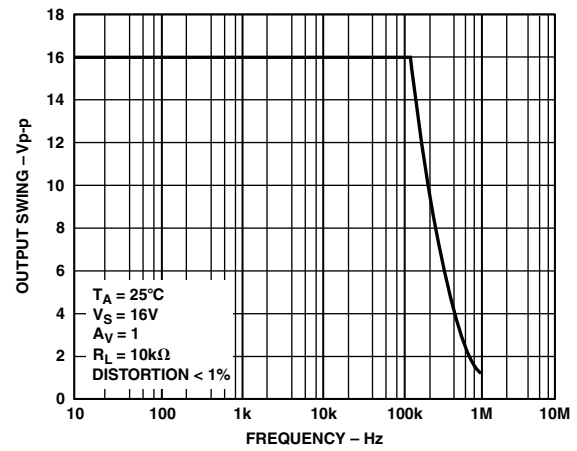
TPC 6. Output Voltage Swing vs. Temperature



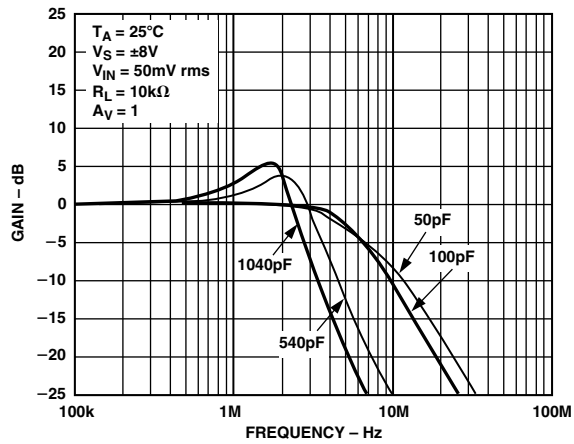
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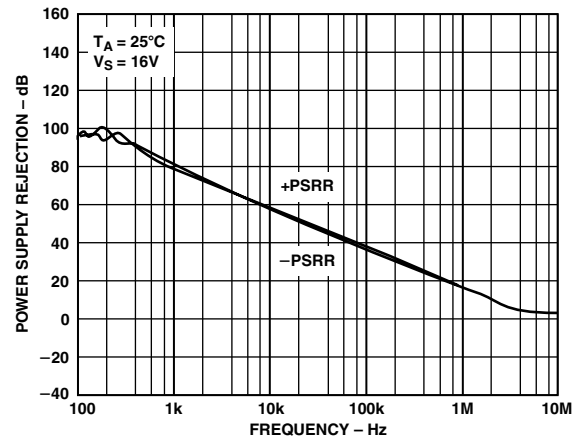
TPC 13. Frequency Response vs. Resistive Loading



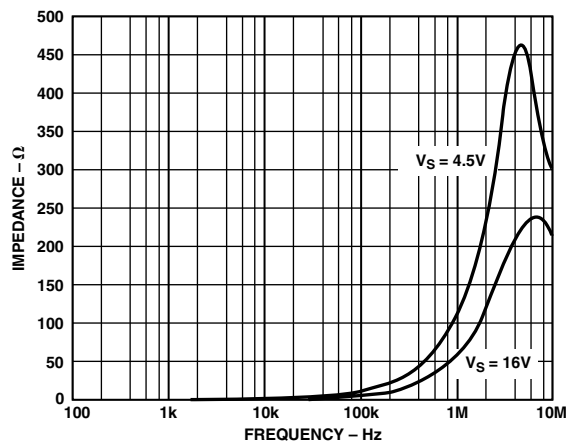
TPC 16. Closed-Loop Output Swing vs. Frequency



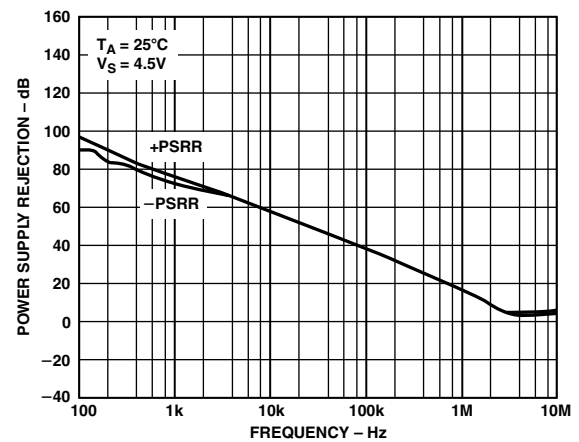
TPC 14. Frequency Response vs. Capacitive Loading



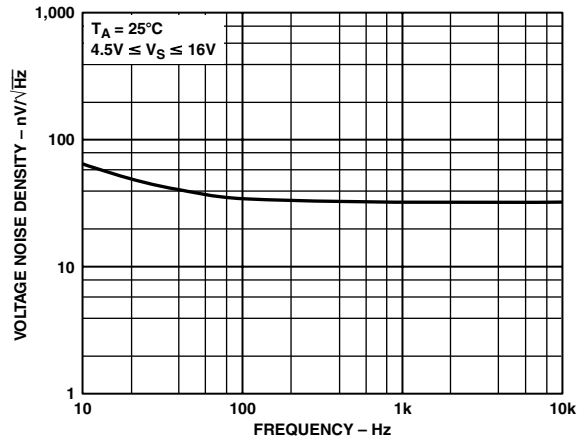
TPC 17. Power Supply Rejection Ratio vs. Frequency



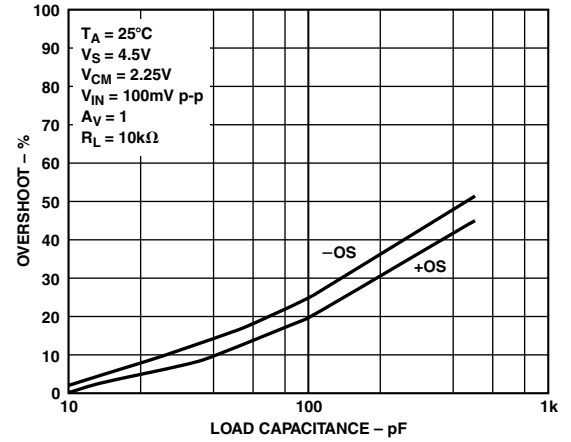
TPC 15. Closed-Loop Output Impedance vs. Frequency



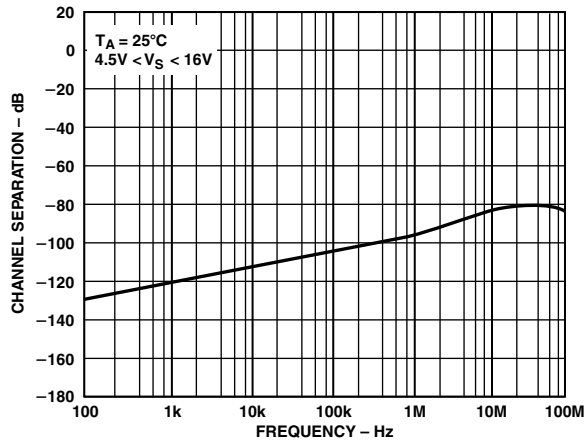
TPC 18. Power Supply Rejection Ratio vs. Frequency



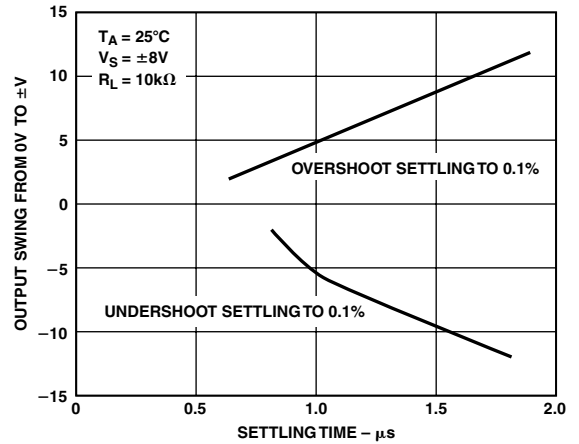
TPC 19. Voltage Noise Density vs. Frequency



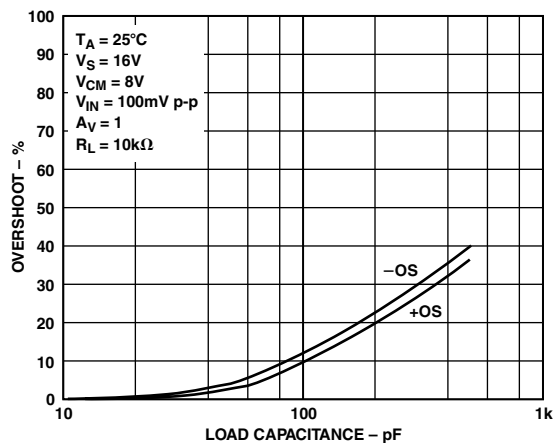
TPC 22. Small Signal Overshoot vs. Load Capacitance



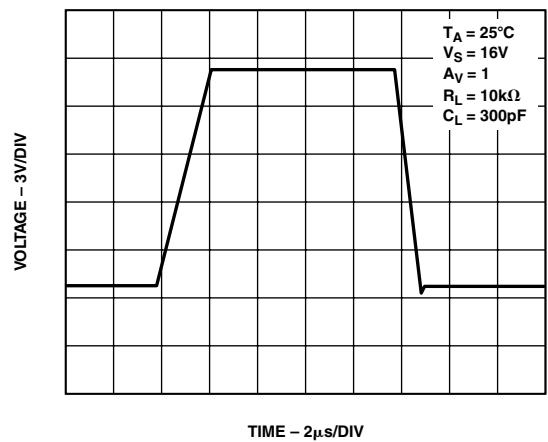
TPC 20. Channel Separation vs. Frequency



TPC 23. Settling Time vs. Step Size

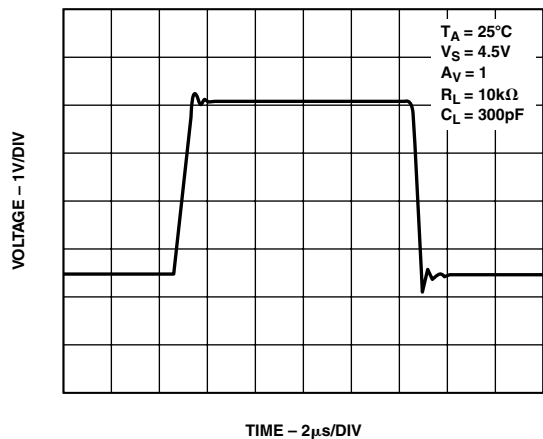


TPC 21. Small Signal Overshoot vs. Load Capacitance

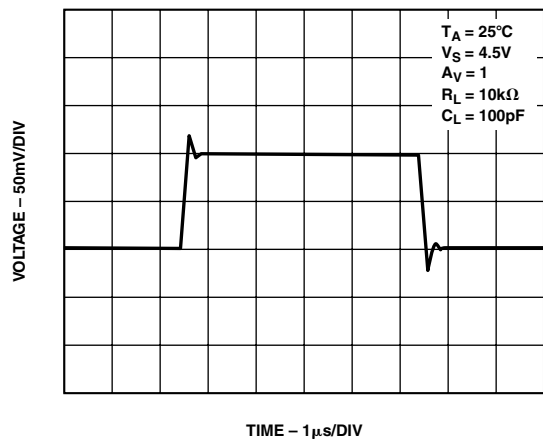


TPC 24. Large Signal Transient Response

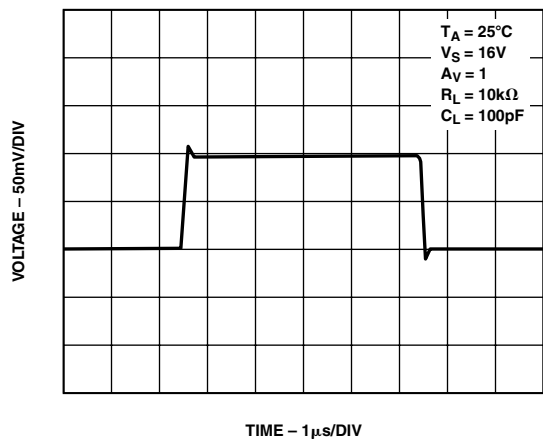
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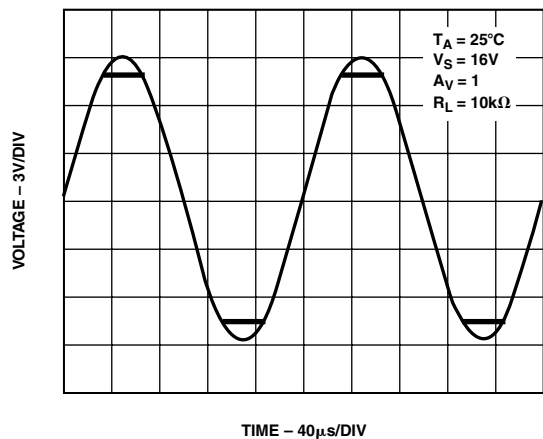
TPC 25. Large Signal Transient Response



TPC 27. Small Signal Transient Response



TPC 26. Small Signal Transient Response



TPC 28. No Phase Reversal

APPLICATIONS

Theory of Operation

This family of buffers is designed to drive large capacitive loads in LCD applications. Each has high output current drive, rail-to-rail input/output operation and can be powered from a single 16 V supply. They are also intended for other applications where low distortion and high output current drive are needed.

Input Overvoltage Protection

As with any semiconductor device, whenever the input exceeds either supply voltage, attention needs to be paid to the input overvoltage characteristics. As an overvoltage occurs, the amplifier could be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, internal pin junctions will allow current to flow from the input to the supplies.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If a condition exists using the buffers where the input exceeds the supply by more than 0.6 V, a series external resistor should be added. The size of the resistor can be calculated by using the maximum overvoltage divided by 5 mA. This resistance should be placed in series with the input exposed to an overvoltage.

Output Phase Reversal

The buffer family is immune to phase reversal. Although the device's output will not change phase, large currents due to input overvoltage could damage the device. In applications where the possibility exists of an input voltage exceeding the supply voltage, overvoltage protection should be used as described in the previous section.

Power Dissipation

The maximum allowable internal junction temperature of 150°C limits the buffer family Maximum Power Dissipation. As the ambient temperature increases, the maximum power dissipated by the buffer family must decrease linearly to maintain the maximum junction temperature. If this maximum junction temperature is exceeded momentarily, the part will still operate properly once the junction temperature is reduced below 150°C. If the maximum junction temperature is exceeded for an extended period of time, overheating could lead to permanent damage of the device.

The maximum safe junction temperature, T_{JMAX} , is 150°C. Using the following formula, we can obtain the maximum power that the buffer family can safely dissipate as a function of temperature.

$$P_{DISS} = (T_{JMAX} - T_A)/\theta_{JA}$$

where:

P_{DISS} = Power dissipation

T_{JMAX} = Maximum allowable junction temp (150°C)

T_A = Ambient temperature of the circuit

θ_{JA} = AD856x package thermal resistance, junction-to-ambient

The power dissipated by the device can be calculated as

$$P_{DISS} = (V_S - V_{OUT}) \times I_{LOAD}$$

where:

V_S = supply voltage

V_{OUT} = output voltage

I_{LOAD} = output load current

Figure 1 shows the maximum power dissipation versus temperature. To achieve proper operation, use the previous equation to calculate P_{DISS} for a specific package at any given temperature, or see Figure 1.

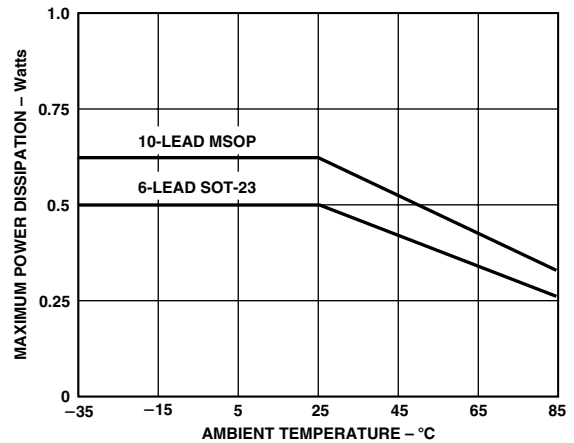


Figure 1. Maximum Power Dissipation vs. Temperature for 6- and 10-Lead Packages

THD + N

The buffer family features low total harmonic distortion. Figure 2 shows a graph of THD + N versus frequency. The Total Harmonic Distortion plus Noise for the buffer over the entire supply range is below 0.08%. When the device is powered from a 16 V supply, the THD + N stays below 0.03%. Figure 2 shows the AD8568 THD + N versus frequency performance.

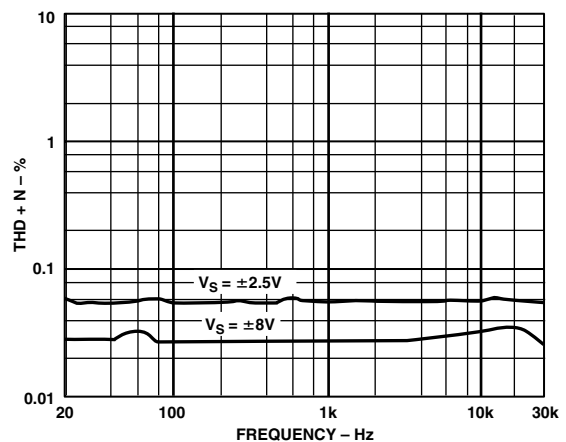


Figure 2. AD8568 THD + N vs. Frequency

Short Circuit Output Conditions

The buffer family does not have internal short circuit protection circuitry. As a precautionary measure, do not short the output directly to the positive power supply or to ground.

It is not recommended to operate the AD856x with more than 35 mA of continuous output current. The output current can be limited by placing a series resistor at the output of the amplifier whose value can be derived using the following equation:

$$R_X \geq \frac{V_S}{35mA}$$

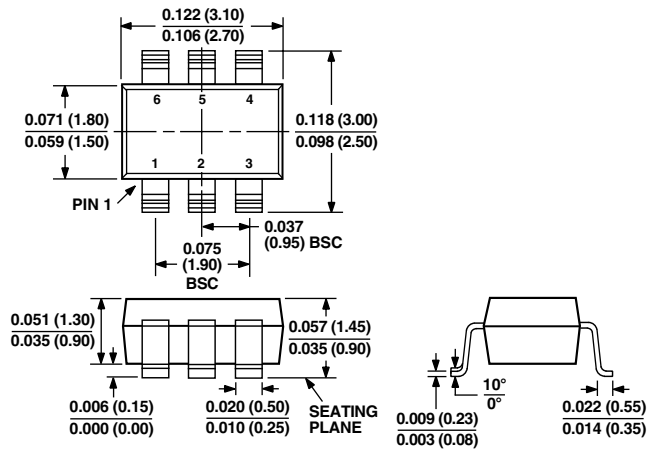
For a 5 V single supply operation, R_X should have a minimum value of 143 Ω .

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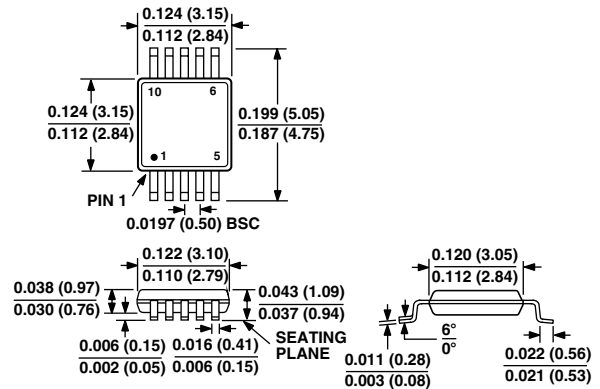
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

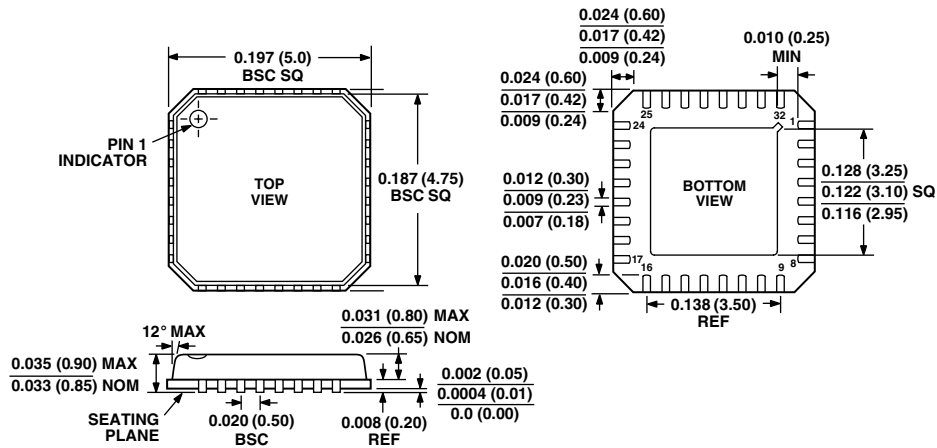
6-Lead SOT-23
(RT Suffix)



10-Lead MSOP
(RM Suffix)



32-Lead LFCSP
(CP Suffix)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
DIMENSIONS MEET JEDEC MO-220-VHHD-2.

Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Finalization of LFCSP Package	Universal

