

### FEATURES

- High isolation voltage: 5000 V rms
- Enhanced system-level ESD performance per IEC 61000-4-x
- Low power operation
  - 5 V operation
    - 1.6 mA per channel maximum at 0 Mbps to 2 Mbps
    - 3.7 mA per channel maximum at 10 Mbps
  - 3 V operation
    - 1.4 mA per channel maximum at 0 Mbps to 2 Mbps
    - 2.4 mA per channel maximum at 10 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High temperature operation: 125°C
- Default low output
- High data rate: dc to 10 Mbps (NRZ)
- Precise timing characteristics
  - 3 ns maximum pulse width distortion
  - 3 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/μs
- 16-lead SOIC wide body package version (RW-16)
- 16-lead SOIC wide body enhanced creepage version (RI-16)
- Safety and regulatory approvals (RI-16 package)
  - UL recognition: 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
    - IEC 60601-1: 250 V rms (reinforced)
    - IEC 60950-1: 400 V rms (reinforced)
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V<sub>IORM</sub> = 846 V peak

### APPLICATIONS

- General-purpose, high voltage, multichannel isolation
- Medical equipment
- Power supplies
- RS-232/RS-422/RS-485 transceiver isolation

### GENERAL DESCRIPTION

The ADuM221x<sup>1</sup> are 2-channel digital isolators based on Analog Devices, Inc., iCoupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics that are superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, iCoupler devices remove the design difficulties commonly associated with optocouplers. Typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents pending.

#### Rev. B

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### FUNCTIONAL BLOCK DIAGRAMS

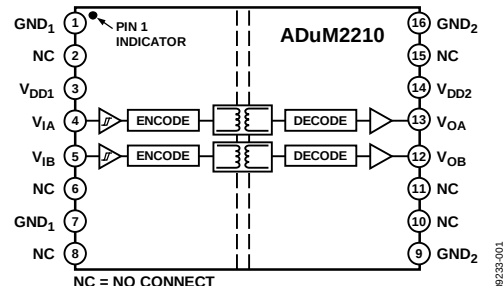


Figure 1. ADuM2210

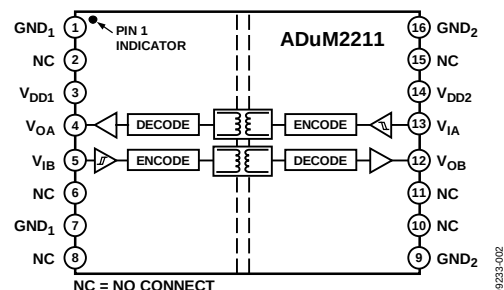


Figure 2. ADuM2211

and lifetime effects are eliminated with the simple iCoupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these iCoupler products. Furthermore, iCoupler devices run at one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM221x isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). The ADuM221x models operate with the supply voltage of either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The ADuM221x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

Similar to the ADuM320x isolators, the ADuM221x isolators contain various circuit and layout enhancements to provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM320x or ADuM221x products is strongly determined by the design and layout of the user's board or module. For more information, see the [AN-793 Application Note](#), ESD/Latch-Up Considerations with iCoupler Isolation Products.

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## REVISION HISTORY

### 2/12—Rev. A to Rev. B

|                                                       |    |
|-------------------------------------------------------|----|
| Created Hyperlink for Safety and Regulatory Approvals |    |
| Entry in Features Section.....                        | 1  |
| Change to PCB Layout Section.....                     | 16 |
| Updated Outline Dimensions .....                      | 19 |

### 8/11—Rev. 0 to Rev. A

|                                     |           |
|-------------------------------------|-----------|
| Added 16-Lead SOIC_IC Package ..... | Universal |
| Changes to Features Section.....    | 1         |
| Changes to Table 5 and Table 6..... | 10        |
| Changes to Endnote 1, Table 8.....  | 11        |
| Updated Outline Dimensions .....    | 19        |
| Changes to Ordering Guide .....     | 20        |

### 9/10—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground.  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ .

Table 1.

| Parameter                                                  | Symbol                | Min                              | Typ   | Max                            | Unit | Test Conditions                                                   |
|------------------------------------------------------------|-----------------------|----------------------------------|-------|--------------------------------|------|-------------------------------------------------------------------|
| DC SPECIFICATIONS                                          |                       |                                  |       |                                |      |                                                                   |
| Input Supply Current, per Channel, Quiescent               | $I_{DD1(Q)}$          |                                  | 0.4   | 0.8                            | mA   |                                                                   |
| Output Supply Current, per Channel, Quiescent              | $I_{DDO(Q)}$          |                                  | 0.5   | 0.6                            | mA   |                                                                   |
| ADuM2210, Total Supply Current, Two Channels <sup>1</sup>  |                       |                                  |       |                                |      |                                                                   |
| DC to 2 Mbps                                               |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(Q)}$          |                                  | 1.3   | 1.7                            | mA   | DC to 1 MHz logic signal frequency                                |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(Q)}$          |                                  | 1.0   | 1.6                            | mA   | DC to 1 MHz logic signal frequency                                |
| 10 Mbps (TR Grade Only)                                    |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(10)}$         |                                  | 3.5   | 4.6                            | mA   | 5 MHz logic signal frequency                                      |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(10)}$         |                                  | 1.7   | 2.8                            | mA   | 5 MHz logic signal frequency                                      |
| ADuM2211, Total Supply Current, Two Channels <sup>1</sup>  |                       |                                  |       |                                |      |                                                                   |
| DC to 2 Mbps                                               |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(Q)}$          |                                  | 1.1   | 1.5                            | mA   | DC to 1 MHz logic signal frequency                                |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(Q)}$          |                                  | 1.3   | 1.8                            | mA   | DC to 1 MHz logic signal frequency                                |
| 10 Mbps (TR Grade Only)                                    |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(10)}$         |                                  | 2.6   | 3.4                            | mA   | 5 MHz logic signal frequency                                      |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(10)}$         |                                  | 3.1   | 4.0                            | mA   | 5 MHz logic signal frequency                                      |
| For All Models                                             |                       |                                  |       |                                |      |                                                                   |
| Input Currents                                             | $I_{IA}, I_{IB}$      | −10                              | +0.01 | +10                            | μA   | $0\text{ V} \leq V_{IA}, V_{IB} \leq V_{DD1} \text{ or } V_{DD2}$ |
| Logic High Input Threshold                                 | $V_{IH}$              | 0.7 ( $V_{DD1}$ or $V_{DD2}$ )   |       |                                | V    |                                                                   |
| Logic Low Input Threshold                                  | $V_{IL}$              |                                  |       | 0.3 ( $V_{DD1}$ or $V_{DD2}$ ) | V    |                                                                   |
| Logic High Output Voltages                                 | $V_{OAH}$             | ( $V_{DD1}$ or $V_{DD2}$ ) − 0.1 | 5.0   |                                | V    | $I_{OX} = -20\text{ }\mu\text{A}$ , $V_{IX} = V_{IXH}$            |
|                                                            | $V_{OBH}$             | ( $V_{DD1}$ or $V_{DD2}$ ) − 0.5 | 4.8   |                                | V    | $I_{OX} = -4\text{ mA}$ , $V_{IX} = V_{IXH}$                      |
|                                                            | $V_{OAL}$             |                                  | 0.0   | 0.1                            | V    | $I_{OX} = 20\text{ }\mu\text{A}$ , $V_{IX} = V_{IXL}$             |
| Logic Low Output Voltages                                  | $V_{OBL}$             |                                  | 0.04  | 0.1                            | V    | $I_{OX} = 400\text{ }\mu\text{A}$ , $V_{IX} = V_{IXL}$            |
|                                                            |                       |                                  | 0.2   | 0.4                            | V    | $I_{OX} = 4\text{ mA}$ , $V_{IX} = V_{IXL}$                       |
| SWITCHING SPECIFICATIONS                                   |                       |                                  |       |                                |      |                                                                   |
| ADuM221xSR                                                 |                       |                                  |       |                                |      |                                                                   |
| Minimum Pulse Width <sup>2</sup>                           | PW                    |                                  |       | 1000                           | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Maximum Data Rate <sup>3</sup>                             |                       | 1                                |       |                                | Mbps | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Propagation Delay <sup>4</sup>                             | $t_{PHL}, t_{PLH}$    | 20                               |       | 150                            | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>4</sup> | PWD                   |                                  |       | 40                             | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Propagation Delay Skew <sup>5</sup>                        | $t_{PSK}$             |                                  |       | 100                            | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Channel-to-Channel Matching <sup>6</sup>                   | $t_{PSKCD}/t_{PSKOD}$ |                                  |       | 50                             | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Output Rise/Fall Time (10% to 90%)                         | $t_R/t_F$             |                                  | 10    |                                | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |

| Parameter                                                                   | Symbol                              | Min | Typ  | Max | Unit    | Test Conditions                                                                                                |
|-----------------------------------------------------------------------------|-------------------------------------|-----|------|-----|---------|----------------------------------------------------------------------------------------------------------------|
| ADuM221xTR                                                                  |                                     |     |      |     |         |                                                                                                                |
| Minimum Pulse Width <sup>2</sup>                                            | PW                                  |     |      | 100 | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Maximum Data Rate <sup>3</sup>                                              |                                     | 10  |      |     | Mbps    | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Propagation Delay <sup>4</sup>                                              | t <sub>PHL</sub> , t <sub>PLH</sub> | 20  |      | 50  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup> | PWD                                 |     |      | 3   | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Change vs. Temperature                                                      |                                     |     | 5    |     | ps/°C   | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Propagation Delay Skew <sup>5</sup>                                         | t <sub>PSK</sub>                    |     |      | 15  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>            | t <sub>PSKCD</sub>                  |     |      | 3   | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Channel-to-Channel Matching, Opposing Directional Channels <sup>6</sup>     | t <sub>PSKOD</sub>                  |     |      | 17  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Output Rise/Fall Time (10% to 90%)                                          | t <sub>R</sub> /t <sub>F</sub>      |     | 2.5  |     | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| For All Models                                                              |                                     |     |      |     |         |                                                                                                                |
| Common-Mode Transient Immunity at Logic High Output <sup>7</sup>            | CM <sub>H</sub>                     | 25  | 35   |     | kV/μs   | V <sub>ix</sub> = V <sub>DD1</sub> or V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>             | CM <sub>L</sub>                     | 25  | 35   |     | kV/μs   | V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V                                   |
| Refresh Rate                                                                | f <sub>r</sub>                      |     | 1.2  |     | Mbps    |                                                                                                                |
| Input Dynamic Supply Current, per Channel <sup>8</sup>                      | I <sub>DDI</sub> (D)                |     | 0.19 |     | mA/Mbps |                                                                                                                |
| Output Dynamic Supply Current, per Channel <sup>8</sup>                     | I <sub>DDO</sub> (D)                |     | 0.05 |     | mA/Mbps |                                                                                                                |

<sup>1</sup> The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I<sub>DD1</sub> and I<sub>DD2</sub> supply currents as a function of data rate for ADuM2210 and ADuM2211 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>5</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—3 V OPERATION**

All voltages are relative to their respective ground.  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.0\text{ V}$ .

**Table 2.**

| Parameter                                                  | Symbol                | Min                              | Typ   | Max                            | Unit | Test Conditions                                                   |
|------------------------------------------------------------|-----------------------|----------------------------------|-------|--------------------------------|------|-------------------------------------------------------------------|
| <b>DC SPECIFICATIONS</b>                                   |                       |                                  |       |                                |      |                                                                   |
| Input Supply Current, per Channel, Quiescent               | $I_{DDI(Q)}$          |                                  | 0.3   | 0.5                            | mA   |                                                                   |
| Output Supply Current, per Channel, Quiescent              | $I_{DDO(Q)}$          |                                  | 0.3   | 0.5                            | mA   |                                                                   |
| ADuM2210, Total Supply Current, Two Channels <sup>1</sup>  |                       |                                  |       |                                |      |                                                                   |
| DC to 2 Mbps                                               |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(Q)}$          |                                  | 0.8   | 1.3                            | mA   | DC to 1 MHz logic signal frequency                                |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(Q)}$          |                                  | 0.7   | 1.0                            | mA   | DC to 1 MHz logic signal frequency                                |
| 10 Mbps (TR Grade Only)                                    |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(10)}$         |                                  | 2.0   | 3.2                            | mA   | 5 MHz logic signal frequency                                      |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(10)}$         |                                  | 1.1   | 1.7                            | mA   | 5 MHz logic signal frequency                                      |
| ADuM2211, Total Supply Current, Two Channels <sup>1</sup>  |                       |                                  |       |                                |      |                                                                   |
| DC to 2 Mbps                                               |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(Q)}$          |                                  | 0.7   | 1.3                            | mA   | DC to 1 MHz logic signal frequency                                |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(Q)}$          |                                  | 0.8   | 1.6                            | mA   | DC to 1 MHz logic signal frequency                                |
| 10 Mbps (TR Grade Only)                                    |                       |                                  |       |                                |      |                                                                   |
| $V_{DD1}$ Supply Current                                   | $I_{DD1(10)}$         |                                  | 1.5   | 2.1                            | mA   | 5 MHz logic signal frequency                                      |
| $V_{DD2}$ Supply Current                                   | $I_{DD2(10)}$         |                                  | 1.9   | 2.4                            | mA   | 5 MHz logic signal frequency                                      |
| <b>For All Models</b>                                      |                       |                                  |       |                                |      |                                                                   |
| Input Currents                                             | $I_{IA}, I_{IB}$      | −10                              | +0.01 | +10                            | μA   | $0\text{ V} \leq V_{IA}, V_{IB} \leq V_{DD1} \text{ or } V_{DD2}$ |
| Logic High Input Threshold                                 | $V_{IH}$              | 0.7 ( $V_{DD1}$ or $V_{DD2}$ )   |       |                                | V    |                                                                   |
| Logic Low Input Threshold                                  | $V_{IL}$              |                                  |       | 0.3 ( $V_{DD1}$ or $V_{DD2}$ ) | V    |                                                                   |
| Logic High Output Voltages                                 | $V_{OAH}$             | ( $V_{DD1}$ or $V_{DD2}$ ) − 0.1 | 3.0   |                                | V    | $I_{OX} = -20\text{ μA}, V_{IX} = V_{IXH}$                        |
|                                                            | $V_{OBH}$             | ( $V_{DD1}$ or $V_{DD2}$ ) − 0.5 | 2.8   |                                | V    | $I_{OX} = -4\text{ mA}, V_{IX} = V_{IXH}$                         |
| Logic Low Output Voltages                                  | $V_{OAL}$             |                                  | 0.0   | 0.1                            | V    | $I_{OX} = 20\text{ μA}, V_{IX} = V_{IXL}$                         |
|                                                            | $V_{OBL}$             |                                  | 0.04  | 0.1                            | V    | $I_{OX} = 400\text{ μA}, V_{IX} = V_{IXL}$                        |
|                                                            |                       |                                  | 0.2   | 0.42                           | V    | $I_{OX} = 4\text{ mA}, V_{IX} = V_{IXL}$                          |
| <b>SWITCHING SPECIFICATIONS</b>                            |                       |                                  |       |                                |      |                                                                   |
| <b>ADuM221xSR</b>                                          |                       |                                  |       |                                |      |                                                                   |
| Minimum Pulse Width <sup>2</sup>                           | PW                    |                                  |       | 1000                           | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Maximum Data Rate <sup>3</sup>                             |                       | 1                                |       |                                | Mbps | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Propagation Delay <sup>4</sup>                             | $t_{PHL}, t_{PLH}$    | 20                               |       | 150                            | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ <sup>4</sup> | PWD                   |                                  |       | 40                             | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Propagation Delay Skew <sup>5</sup>                        | $t_{PSK}$             |                                  |       | 100                            | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Channel-to-Channel Matching <sup>6</sup>                   | $t_{PSKCD}/t_{PSKOD}$ |                                  |       | 50                             | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |
| Output Rise/Fall Time (10% to 90%)                         | $t_R/t_F$             |                                  | 10    |                                | ns   | $C_L = 15\text{ pF}$ , CMOS signal levels                         |

| Parameter                                                                   | Symbol                              | Min | Typ  | Max | Unit    | Test Conditions                                                                                                |
|-----------------------------------------------------------------------------|-------------------------------------|-----|------|-----|---------|----------------------------------------------------------------------------------------------------------------|
| ADuM221xTR                                                                  |                                     |     |      |     |         |                                                                                                                |
| Minimum Pulse Width <sup>2</sup>                                            | PW                                  |     |      | 100 | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Maximum Data Rate <sup>3</sup>                                              |                                     | 10  |      |     | Mbps    | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Propagation Delay <sup>4</sup>                                              | t <sub>PHL</sub> , t <sub>PLH</sub> | 20  |      | 60  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Pulse Width Distortion,  t <sub>PLH</sub> – t <sub>PHL</sub>   <sup>4</sup> | PWD                                 |     |      | 3   | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Change vs. Temperature                                                      |                                     |     | 5    |     | ps/°C   | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Propagation Delay Skew <sup>5</sup>                                         | t <sub>PSK</sub>                    |     |      | 22  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>            | t <sub>PSKCD</sub>                  |     |      | 3   | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Channel-to-Channel Matching, Opposing Directional Channels <sup>6</sup>     | t <sub>PSKOD</sub>                  |     |      | 22  | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| Output Rise/Fall Time (10% to 90%)                                          | t <sub>r</sub> /t <sub>f</sub>      |     | 3.0  |     | ns      | C <sub>L</sub> = 15 pF, CMOS signal levels                                                                     |
| For All Models                                                              |                                     |     |      |     |         |                                                                                                                |
| Common-Mode Transient Immunity at Logic High Output <sup>7</sup>            | CM <sub>H</sub>                     | 25  | 35   |     | kV/μs   | V <sub>ix</sub> = V <sub>DD1</sub> or V <sub>DD2</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>             | CM <sub>L</sub>                     | 25  | 35   |     | kV/μs   | V <sub>ix</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V                                   |
| Refresh Rate                                                                | f <sub>r</sub>                      |     | 1.1  |     | Mbps    |                                                                                                                |
| Input Dynamic Supply Current, per Channel <sup>8</sup>                      | I <sub>DDI</sub> (D)                |     | 0.10 |     | mA/Mbps |                                                                                                                |
| Output Dynamic Supply Current, per Channel <sup>8</sup>                     | I <sub>DDO</sub> (D)                |     | 0.03 |     | mA/Mbps |                                                                                                                |

<sup>1</sup> The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I<sub>DD1</sub> and I<sub>DD2</sub> supply currents as a function of data rate for ADuM2210 and ADuM2211 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>5</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION**

All voltages are relative to their respective ground. 5 V/3 V operation:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ . 3 V/5 V operation:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD1} = 3.0\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ ; or  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$ .

**Table 3.**

| Parameter                                                 | Symbol        | Min | Typ | Max | Unit | Test Conditions                    |
|-----------------------------------------------------------|---------------|-----|-----|-----|------|------------------------------------|
| <b>DC SPECIFICATIONS</b>                                  |               |     |     |     |      |                                    |
| Input Supply Current, per Channel, Quiescent              | $I_{DD1(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 0.4 | 0.8 | mA   |                                    |
| 3 V/5 V Operation                                         |               |     | 0.3 | 0.5 | mA   |                                    |
| Output Supply Current, per Channel, Quiescent             | $I_{DDO(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 0.3 | 0.5 | mA   |                                    |
| 3 V/5 V Operation                                         |               |     | 0.5 | 0.6 | mA   |                                    |
| ADuM2210, Total Supply Current, Two Channels <sup>1</sup> |               |     |     |     |      |                                    |
| DC to 2 Mbps                                              |               |     |     |     |      |                                    |
| $V_{DD1}$ Supply Current                                  | $I_{DD1(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 1.3 | 1.7 | mA   | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation                                         |               |     | 0.8 | 1.3 | mA   | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current                                  | $I_{DD2(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 0.7 | 1.0 | mA   | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation                                         |               |     | 1.0 | 1.6 | mA   | DC to 1 MHz logic signal frequency |
| 10 Mbps (TR Grade Only)                                   |               |     |     |     |      |                                    |
| $V_{DD1}$ Supply Current                                  | $I_{DD1(10)}$ |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 3.5 | 4.6 | mA   | 5 MHz logic signal frequency       |
| 3 V/5 V Operation                                         |               |     | 2.0 | 3.2 | mA   | 5 MHz logic signal frequency       |
| $V_{DD2}$ Supply Current                                  | $I_{DD2(10)}$ |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 1.1 | 1.7 | mA   | 5 MHz logic signal frequency       |
| 3 V/5 V Operation                                         |               |     | 1.7 | 2.8 | mA   | 5 MHz logic signal frequency       |
| ADuM2211, Total Supply Current, Two Channels <sup>1</sup> |               |     |     |     |      |                                    |
| DC to 2 Mbps                                              |               |     |     |     |      |                                    |
| $V_{DD1}$ Supply Current                                  | $I_{DD1(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 1.1 | 1.5 | mA   | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation                                         |               |     | 0.7 | 1.3 | mA   | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current                                  | $I_{DD2(Q)}$  |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 0.8 | 1.6 | mA   | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation                                         |               |     | 1.3 | 1.8 | mA   | DC to 1 MHz logic signal frequency |
| 10 Mbps (TR Grade Only)                                   |               |     |     |     |      |                                    |
| $V_{DD1}$ Supply Current                                  | $I_{DD1(10)}$ |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 2.6 | 3.4 | mA   | 5 MHz logic signal frequency       |
| 3 V/5 V Operation                                         |               |     | 1.5 | 2.1 | mA   | 5 MHz logic signal frequency       |
| $V_{DD2}$ Supply Current                                  | $I_{DD2(10)}$ |     |     |     |      |                                    |
| 5 V/3 V Operation                                         |               |     | 1.9 | 2.4 | mA   | 5 MHz logic signal frequency       |
| 3 V/5 V Operation                                         |               |     | 3.1 | 4.0 | mA   | 5 MHz logic signal frequency       |

| Parameter                                                               | Symbol                | Min                              | Typ                              | Max                            | Unit            | Test Conditions                                                                               |
|-------------------------------------------------------------------------|-----------------------|----------------------------------|----------------------------------|--------------------------------|-----------------|-----------------------------------------------------------------------------------------------|
| For All Models                                                          |                       |                                  |                                  |                                |                 |                                                                                               |
| Input Currents                                                          | $I_{IA}, I_{IB}$      | -10                              | +0.01                            | +10                            | $\mu A$         | $0V \leq V_{IA}, V_{IB} \leq V_{DD1} \text{ or } V_{DD2}$                                     |
| Logic High Input Threshold                                              | $V_{IH}$              | 0.7 ( $V_{DD1}$ or $V_{DD2}$ )   |                                  |                                | V               |                                                                                               |
| Logic Low Input Threshold                                               | $V_{IL}$              |                                  |                                  | 0.3 ( $V_{DD1}$ or $V_{DD2}$ ) | V               |                                                                                               |
| Logic High Output Voltages                                              | $V_{OAH}, V_{OBH}$    | ( $V_{DD1}$ or $V_{DD2}$ ) - 0.1 | ( $V_{DD1}$ or $V_{DD2}$ )       |                                | V               | $I_{OX} = -20 \mu A, V_{IX} = V_{IXH}$                                                        |
|                                                                         |                       | ( $V_{DD1}$ or $V_{DD2}$ ) - 0.5 | ( $V_{DD1}$ or $V_{DD2}$ ) - 0.2 |                                | V               | $I_{OX} = -4 \text{ mA}, V_{IX} = V_{IXH}$                                                    |
| Logic Low Output Voltages                                               | $V_{OAL}, V_{OBL}$    |                                  | 0.0                              | 0.1                            | V               | $I_{OX} = 20 \mu A, V_{IX} = V_{IXL}$                                                         |
|                                                                         |                       |                                  | 0.04                             | 0.1                            | V               | $I_{OX} = 400 \mu A, V_{IX} = V_{IXL}$                                                        |
|                                                                         |                       |                                  | 0.2                              | 0.42                           | V               | $I_{OX} = 4 \text{ mA}, V_{IX} = V_{IXL}$                                                     |
| SWITCHING SPECIFICATIONS                                                |                       |                                  |                                  |                                |                 |                                                                                               |
| ADuM221xSR                                                              |                       |                                  |                                  |                                |                 |                                                                                               |
| Minimum Pulse Width <sup>2</sup>                                        | PW                    |                                  |                                  | 1000                           | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Maximum Data Rate <sup>3</sup>                                          |                       | 1                                |                                  |                                | Mbps            | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Propagation Delay <sup>4</sup>                                          | $t_{PHL}, t_{PLH}$    | 15                               |                                  | 150                            | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$                         | PWD                   |                                  |                                  | 40                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Propagation Delay Skew <sup>5</sup>                                     | $t_{PSK}$             |                                  |                                  | 50                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Channel-to-Channel Matching <sup>6</sup>                                | $t_{PSKCD}/t_{PSKOD}$ |                                  |                                  | 50                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Output Rise/Fall Time (10% to 90%)                                      | $t_R/t_F$             |                                  | 10                               |                                | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| ADuM221xTR                                                              |                       |                                  |                                  |                                |                 |                                                                                               |
| Minimum Pulse Width <sup>2</sup>                                        | PW                    |                                  |                                  | 100                            | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Maximum Data Rate <sup>3</sup>                                          |                       | 10                               |                                  |                                | Mbps            | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Propagation Delay <sup>4</sup>                                          | $t_{PHL}, t_{PLH}$    | 15                               |                                  | 55                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$                         | PWD                   |                                  |                                  | 3                              | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Change vs. Temperature                                                  |                       |                                  | 5                                |                                | ps/ $^{\circ}C$ | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Propagation Delay Skew <sup>5</sup>                                     | $t_{PSK}$             |                                  |                                  | 22                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Channel-to-Channel Matching, Codirectional Channels <sup>6</sup>        | $t_{PSKCD}$           |                                  |                                  | 3                              | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Channel-to-Channel Matching, Opposing Directional Channels <sup>6</sup> | $t_{PSKOD}$           |                                  |                                  | 22                             | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| Output Rise/Fall Time (10% to 90%)                                      | $t_R/t_F$             |                                  |                                  |                                |                 |                                                                                               |
| 5 V/3 V Operation                                                       |                       |                                  | 3.0                              |                                | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| 3 V/5 V Operation                                                       |                       |                                  | 2.5                              |                                | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| 5 V/3 V Operation                                                       |                       |                                  | 3.0                              |                                | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| 3 V/5 V Operation                                                       |                       |                                  | 2.5                              |                                | ns              | $C_L = 15 \text{ pF}$ , CMOS signal levels                                                    |
| For All Models                                                          |                       |                                  |                                  |                                |                 |                                                                                               |
| Common-Mode Transient Immunity at Logic High Output <sup>7</sup>        | $ CM_H $              | 25                               | 35                               |                                | kV/ $\mu s$     | $V_{IX} = V_{DD1} \text{ or } V_{DD2}, V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output <sup>7</sup>         | $ CM_L $              | 25                               | 35                               |                                | kV/ $\mu s$     | $V_{IX} = 0 \text{ V}, V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V                 |
| Refresh Rate                                                            | $f_r$                 |                                  |                                  |                                |                 |                                                                                               |
| 5 V/3 V Operation                                                       |                       |                                  | 1.2                              |                                | Mbps            |                                                                                               |
| 3 V/5 V Operation                                                       |                       |                                  | 1.1                              |                                | Mbps            |                                                                                               |
| Input Dynamic Supply Current, per Channel <sup>8</sup>                  | $I_{DDI(D)}$          |                                  |                                  |                                |                 |                                                                                               |
| 5 V/3 V Operation                                                       |                       |                                  | 0.19                             |                                | mA/Mbps         |                                                                                               |
| 3 V/5 V Operation                                                       |                       |                                  | 0.10                             |                                | mA/Mbps         |                                                                                               |

| Parameter                                                  | Symbol       | Min | Typ  | Max | Unit    | Test Conditions |
|------------------------------------------------------------|--------------|-----|------|-----|---------|-----------------|
| Output Dynamic Supply Current,<br>per Channel <sup>8</sup> | $I_{DDO(D)}$ |     |      |     |         |                 |
| 5 V/3 V Operation                                          |              |     | 0.03 |     | mA/Mbps |                 |
| 3 V/5 V Operation                                          |              |     | 0.05 |     | mA/Mbps |                 |

<sup>1</sup> The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total  $I_{DD1}$  and  $I_{DD2}$  supply currents as a function of data rate for ADuM2210 and ADuM2211 channel configurations.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>3</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>4</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{IX}$  signal to the 50% level of the falling edge of the  $V_{OX}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{IX}$  signal to the 50% level of the rising edge of the  $V_{OX}$  signal.

<sup>5</sup>  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>6</sup> Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>7</sup>  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8 V$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>8</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

## PACKAGE CHARACTERISTICS

Table 4.

| Parameter                                      | Symbol           | Min | Typ              | Max | Unit | Test Conditions                                     |
|------------------------------------------------|------------------|-----|------------------|-----|------|-----------------------------------------------------|
| Resistance (Input-to-Output) <sup>1</sup>      | R <sub>I-O</sub> |     | 10 <sup>12</sup> |     | Ω    | f = 1 MHz                                           |
| Capacitance (Input-to-Output) <sup>1</sup>     | C <sub>I-O</sub> |     | 2.2              |     | pF   |                                                     |
| Input Capacitance <sup>2</sup>                 | C <sub>I</sub>   |     | 4.0              |     | pF   |                                                     |
| IC Junction-to-Case Thermal Resistance, Side 1 | θ <sub>JCI</sub> | 33  |                  |     | °C/W | Thermocouple located at center of package underside |
| IC Junction-to-Case Thermal Resistance, Side 2 | θ <sub>JCO</sub> | 28  |                  |     | °C/W |                                                     |

<sup>1</sup> Device considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM221x are approved by the organizations listed in Table 5. Refer to Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

| UL                                                               | CSA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDE                                                                              |
|------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| Recognized under 1577 Component Recognition Program <sup>1</sup> | Approved under CSA Component Acceptance Notice #5A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 <sup>2</sup> |
| Single Protection<br>5000 V rms Isolation Voltage                | Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage<br>RW-16 package:<br>Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage; reinforced insulation per IEC 60601-1 125 V rms (176 V peak) maximum working voltage<br>RI-16 package:<br>Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage; reinforced insulation per IEC 60601-1 250 V rms (353 V peak) maximum working voltage | Reinforced insulation, 846 V peak                                                |
| File E214100                                                     | File 205078                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | File 2471900-4880-0001                                                           |

<sup>1</sup> In accordance with UL1577, each ADuM221x is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each ADuM221x is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

| Parameter                                          | Symbol | Value     | Unit  | Conditions                                                                                                                                           |
|----------------------------------------------------|--------|-----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rated Dielectric Insulation Voltage                |        | 5000      | V rms | 1-minute duration                                                                                                                                    |
| Minimum External Air Gap                           | L(I01) | 8.0 min   | mm    | Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout |
| Minimum External Tracking (Creepage) RW-16 Package | L(I02) | 7.7 min   | mm    | Measured from input terminals to output terminals, shortest distance path along body                                                                 |
| Minimum External Tracking (Creepage) RI-16 Package | L(I02) | 8.3 min   | mm    | Measured from input terminals to output terminals, shortest distance path along body                                                                 |
| Minimum Internal Gap (Internal Clearance)          |        | 0.017 min | mm    | Insulation distance through insulation                                                                                                               |
| Tracking Resistance (Comparative Tracking Index)   | CTI    | >175      | V     | DIN IEC 112/VDE 0303 Part 1                                                                                                                          |
| Isolation Group                                    |        | IIIa      |       | Material Group (DIN VDE 0110, 1/89, Table 1)                                                                                                         |

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. Note that the asterisk (\*) branded on packages denotes DIN V VDE V 0884-10 approval for 846 V peak working voltage.

**Table 7.**

| Description                                                                                                                                                       | Conditions                                                                                       | Symbol     | Characteristic                | Unit   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|------------|-------------------------------|--------|
| Installation Classification per DIN VDE 0110<br>For Rated Mains Voltage ≤ 300 V rms<br>For Rated Mains Voltage ≤ 450 V rms<br>For Rated Mains Voltage ≤ 600 V rms |                                                                                                  |            | I to IV<br>I to II<br>I to II |        |
| Climatic Classification                                                                                                                                           |                                                                                                  |            | 40/125/21                     |        |
| Pollution Degree (DIN VDE 0110, Table 1)                                                                                                                          |                                                                                                  |            | 2                             |        |
| Maximum Working Insulation Voltage                                                                                                                                |                                                                                                  | $V_{IORM}$ | 846                           | V peak |
| Input-to-Output Test Voltage, Method B1                                                                                                                           | $V_{IORM} \times 1.875 = V_{PR}$ , 100% production test, $t_m = 1$ sec, partial discharge < 5 pC | $V_{PR}$   | 1590                          | V peak |
| Input-to-Output Test Voltage, Method A                                                                                                                            |                                                                                                  | $V_{PR}$   |                               |        |
| After Environmental Tests Subgroup 1                                                                                                                              | $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC                        |            | 1375                          | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3                                                                                                          | $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC                        |            | 1018                          | V peak |
| Highest Allowable Overvoltage                                                                                                                                     | Transient overvoltage, $t_{TR} = 10$ seconds                                                     | $V_{TR}$   | 6000                          | V peak |
| Safety-Limiting Values                                                                                                                                            | Maximum value allowed in the event of a failure; see Figure 3                                    |            |                               |        |
| Case Temperature                                                                                                                                                  |                                                                                                  | $T_S$      | 150                           | °C     |
| Side 1 Current                                                                                                                                                    |                                                                                                  | $I_{S1}$   | 265                           | mA     |
| Side 2 Current                                                                                                                                                    |                                                                                                  | $I_{S2}$   | 335                           | mA     |
| Insulation Resistance at $T_S$                                                                                                                                    | $V_{IO} = 500$ V                                                                                 | $R_S$      | >10 <sup>9</sup>              | Ω      |

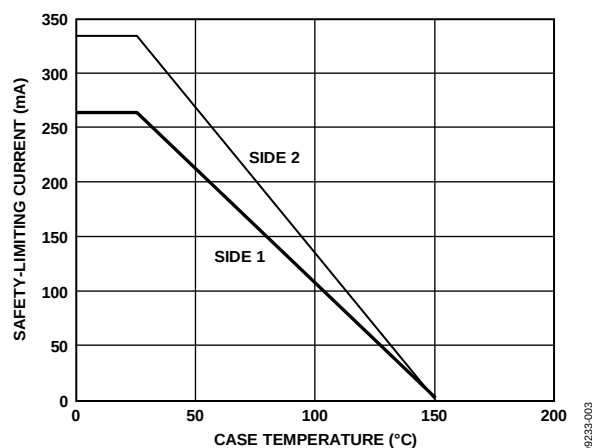


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

**RECOMMENDED OPERATING CONDITIONS****Table 8.**

| Parameter                        | Symbol             | Min | Max  | Unit |
|----------------------------------|--------------------|-----|------|------|
| Operating Temperature            | $T_A$              | -40 | +125 | °C   |
| Supply Voltages <sup>1</sup>     | $V_{DD1}, V_{DD2}$ | 3.0 | 5.5  | V    |
| Input Signal Rise and Fall Times |                    |     | 1.0  | ms   |

<sup>1</sup> All voltages are relative to their respective ground.

## ABSOLUTE MAXIMUM RATINGS

Table 9.

| Parameter                                              | Rating                      |
|--------------------------------------------------------|-----------------------------|
| Storage Temperature ( $T_{ST}$ )                       | –65°C to +150°C             |
| Ambient Operating Temperature ( $T_A$ )                | –40°C to +125°C             |
| Supply Voltage ( $V_{DD1}$ , $V_{DD2}$ ) <sup>1</sup>  | –0.5 V to +7.0 V            |
| Input Voltage ( $V_{IA}$ , $V_{IB}$ ) <sup>1, 2</sup>  | –0.5 V to $V_{DD1}$ + 0.5 V |
| Output Voltage ( $V_{OA}$ , $V_{OB}$ ) <sup>1, 2</sup> | –0.5 V to $V_{DD0}$ + 0.5 V |
| Average Output Current per Pin <sup>3</sup>            |                             |
| Side 1 ( $I_{O1}$ )                                    | –18 mA to +18 mA            |
| Side 2 ( $I_{O2}$ )                                    | –22 mA to +22 mA            |
| Common-Mode Transients <sup>4</sup>                    | –100 kV/μs to +100 kV/μs    |

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup>  $V_{DD1}$  and  $V_{DD0}$  refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

<sup>3</sup> See Figure 3 for maximum rated current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage<sup>1</sup>

| Parameter                                              | Max | Unit   | Constraint                                                         |
|--------------------------------------------------------|-----|--------|--------------------------------------------------------------------|
| AC Voltage, Bipolar Waveform                           | 565 | V peak | 50-year minimum lifetime                                           |
| AC Voltage, Unipolar Waveform<br>Reinforced Insulation | 846 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage<br>Reinforced Insulation                    | 846 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

<sup>1</sup> Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

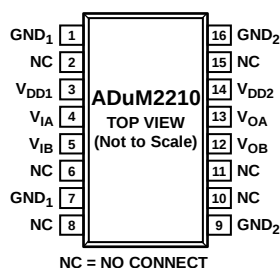
Table 11. ADuM2210 Truth Table (Positive Logic)

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes                                                                         |
|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-------------------------------------------------------------------------------|
| H              | H              | Powered         | Powered         | H               | H               | Outputs return to the input state within 1 μs of $V_{DD1}$ power restoration. |
| L              | L              | Powered         | Powered         | L               | L               |                                                                               |
| H              | L              | Powered         | Powered         | H               | L               |                                                                               |
| L              | H              | Powered         | Powered         | L               | H               |                                                                               |
| X              | X              | Unpowered       | Powered         | L               | L               |                                                                               |
| X              | X              | Powered         | Unpowered       | Indeterminate   | Indeterminate   | Outputs return to the input state within 1 μs of $V_{DD0}$ power restoration. |

Table 12. ADuM2211 Truth Table (Positive Logic)

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes                                                                         |
|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-------------------------------------------------------------------------------|
| H              | H              | Powered         | Powered         | H               | H               | Outputs return to the input state within 1 μs of $V_{DD1}$ power restoration. |
| L              | L              | Powered         | Powered         | L               | L               |                                                                               |
| H              | L              | Powered         | Powered         | H               | L               |                                                                               |
| L              | H              | Powered         | Powered         | L               | H               |                                                                               |
| X              | X              | Unpowered       | Powered         | Indeterminate   | L               |                                                                               |
| X              | X              | Powered         | Unpowered       | L               | Indeterminate   | Outputs return to the input state within 1 μs of $V_{DD0}$ power restoration. |

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



## NOTES:

1. PIN 1 AND PIN 7 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND<sub>1</sub> IS RECOMMENDED.
2. PIN 9 AND PIN 16 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND<sub>2</sub> IS RECOMMENDED.

09233-004

Figure 4. ADuM2210 Pin Configuration

Table 13. ADuM2210 Pin Function Descriptions

| Pin No. | Mnemonic         | Description                                         |
|---------|------------------|-----------------------------------------------------|
| 1       | GND <sub>1</sub> | Ground 1. Ground reference for Isolator Side 1.     |
| 2       | NC               | No internal connection.                             |
| 3       | V <sub>DD1</sub> | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 4       | V <sub>1A</sub>  | Logic Input A.                                      |
| 5       | V <sub>1B</sub>  | Logic Input B.                                      |
| 6       | NC               | No internal connection.                             |
| 7       | GND <sub>1</sub> | Ground 1. Ground reference for Isolator Side 1.     |
| 8       | NC               | No internal connection.                             |
| 9       | GND <sub>2</sub> | Ground 2. Ground reference for Isolator Side 2.     |
| 10      | NC               | No internal connection.                             |
| 11      | NC               | No internal connection.                             |
| 12      | V <sub>OB</sub>  | Logic Output B.                                     |
| 13      | V <sub>OA</sub>  | Logic Output A.                                     |
| 14      | V <sub>DD2</sub> | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |
| 15      | NC               | No internal connection.                             |
| 16      | GND <sub>2</sub> | Ground 2. Ground reference for Isolator Side 2.     |

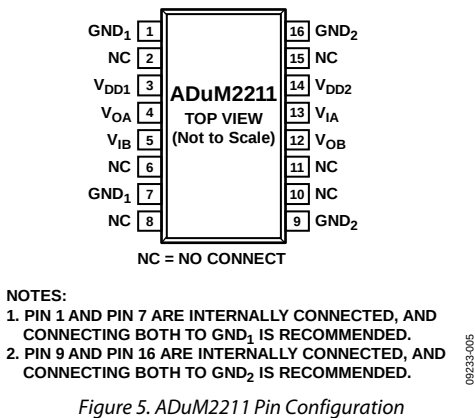


Table 14. ADuM2211 Pin Function Descriptions

| Pin No. | Mnemonic         | Description                                         |
|---------|------------------|-----------------------------------------------------|
| 1       | GND <sub>1</sub> | Ground 1. Ground reference for Isolator Side 1.     |
| 2       | NC               | No internal connection.                             |
| 3       | V <sub>DD1</sub> | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 4       | V <sub>OA</sub>  | Logic Output A.                                     |
| 5       | V <sub>IB</sub>  | Logic Input B.                                      |
| 6       | NC               | No internal connection.                             |
| 7       | GND <sub>1</sub> | Ground 1. Ground reference for Isolator Side 1.     |
| 8       | NC               | No internal connection.                             |
| 9       | GND <sub>2</sub> | Ground 2. Ground reference for Isolator Side 2.     |
| 10      | NC               | No internal connection.                             |
| 11      | NC               | No internal connection.                             |
| 12      | V <sub>OB</sub>  | Logic Output B.                                     |
| 13      | V <sub>IA</sub>  | Logic Input A.                                      |
| 14      | V <sub>DD2</sub> | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |
| 15      | NC               | No internal connection.                             |
| 16      | GND <sub>2</sub> | Ground 2. Ground reference for Isolator Side 2.     |

## TYPICAL PERFORMANCE CHARACTERISTICS

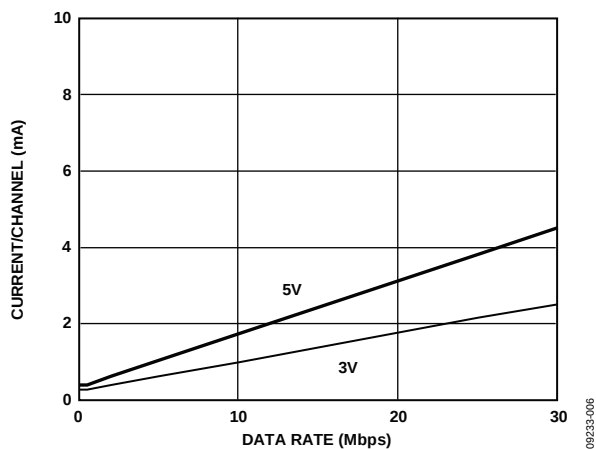


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

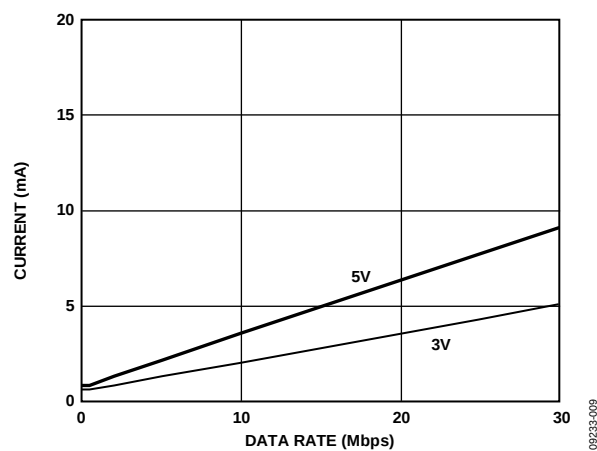


Figure 9. Typical ADuM2210 V<sub>DD1</sub> Supply Current vs. Data Rate for 5 V and 3 V Operation

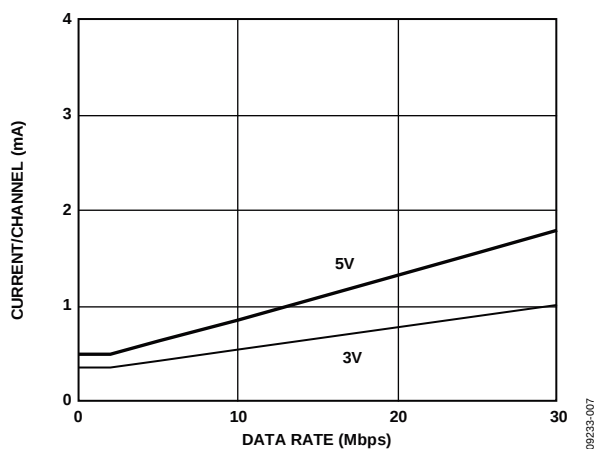


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

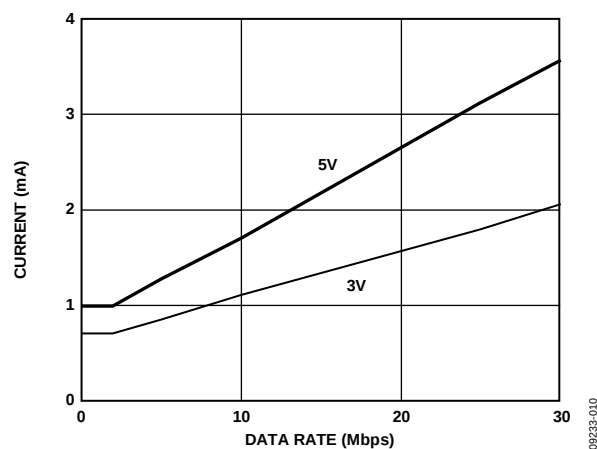


Figure 10. Typical ADuM2210 V<sub>DD2</sub> Supply Current vs. Data Rate for 5 V and 3 V Operation

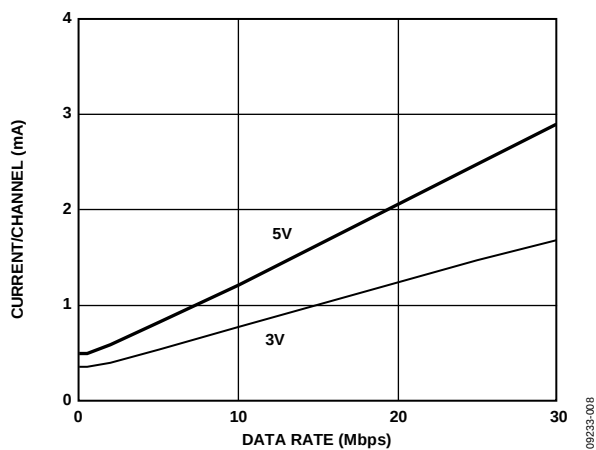


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

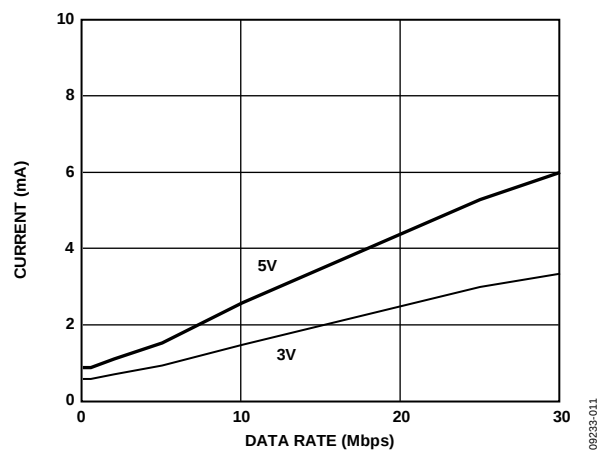


Figure 11. Typical ADuM2211 V<sub>DD1</sub> or V<sub>DD2</sub> Supply Current vs. Data Rate for 5 V and 3 V Operation

## APPLICATIONS INFORMATION

### PCB LAYOUT

The ADuM221x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 12). Bypass capacitors are most conveniently connected between Pin 1 and Pin 3 for  $V_{DD1}$  and between Pin 14 and Pin 16 for  $V_{DD2}$ . The capacitor value should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 3 and Pin 7 and between Pin 9 and Pin 14 should be considered unless the ground pair on each package side is connected close to the package.

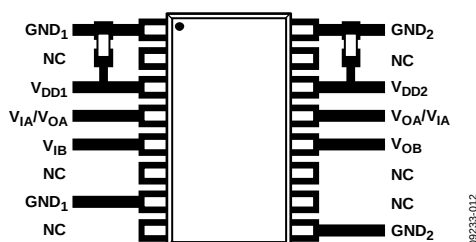


Figure 12. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to logic high.

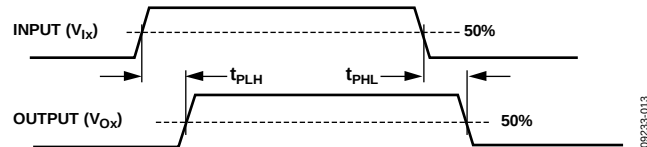


Figure 13. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs among channels within a single ADuM221x component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM221x components operated under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow ( $\sim 1$  ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than  $\sim 1$   $\mu\text{s}$ , a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5  $\mu\text{s}$ , the input side is assumed to be without power or nonfunctional, in which case, the isolator output is forced to a default state (see Table 11 and Table 12) by the watchdog timer circuit.

The limitation on the ADuM221x magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM221x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is the magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM221x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 14.

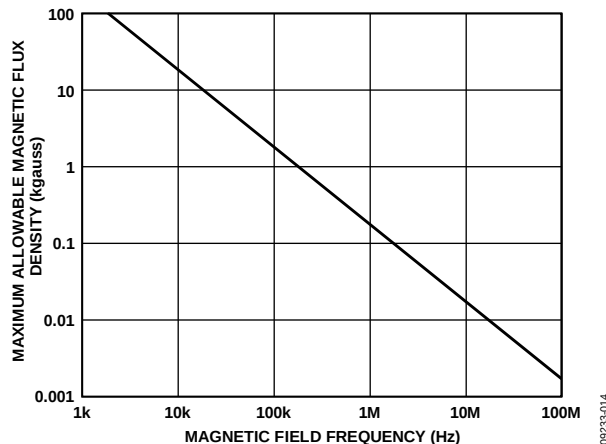


Figure 14. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM221x transformers. Figure 15 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM221x is immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted previously, one would have to place a 0.5 kA current 5 mm away from the ADuM221x to affect operation of the component.

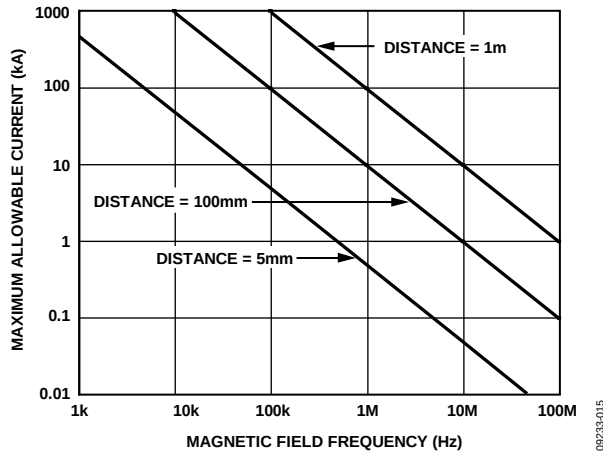


Figure 15. Maximum Allowable Current for Various Current-to-ADuM221x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM221x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

$f_r$  is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$ , the supply currents for each input and output channel corresponding to  $I_{DD1}$  and  $I_{DD2}$  are calculated and totaled. Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 provide total  $I_{DD1}$  and  $I_{DD2}$  as a function of data rate for ADuM2210/ADuM2211 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM221x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than a 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM221x depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 16, Figure 17, and Figure 18 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 17 or Figure 18 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

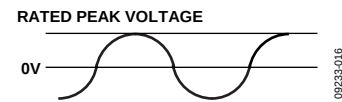


Figure 16. Bipolar AC Waveform

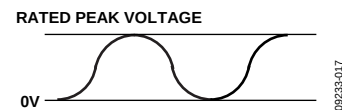


Figure 17. Unipolar AC Waveform

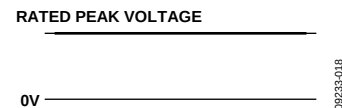
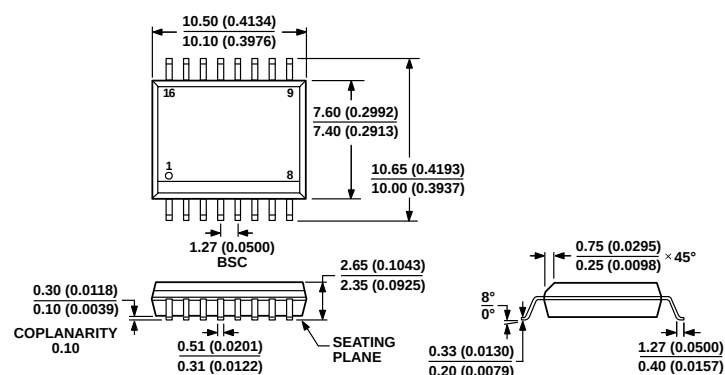


Figure 18. DC Waveform

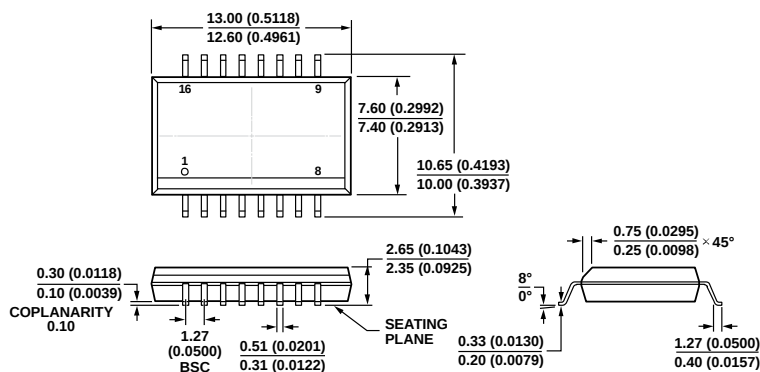
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 16-Lead Standard Small Outline Package [SOIC\_W]  
Wide Body (RW-16)  
Dimensions shown in millimeters and (inches)

03-27-2007-B



COMPLIANT TO JEDEC STANDARDS MS-013-AC  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 20. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC\_IC]  
Wide Body (RI-16-1)  
Dimensions shown in millimeters and (inches)

10-12-2010-A

## ORDERING GUIDE

| Model <sup>1, 2</sup> | Number of Inputs, V <sub>DD1</sub> Side | Number of Inputs, V <sub>DD2</sub> Side | Maximum Data Rate (Mbps) | Maximum Propagation Delay, 5 V (ns) | Maximum Pulse Width Distortion (ns) | Temperature Range | Package Description | Package Option |
|-----------------------|-----------------------------------------|-----------------------------------------|--------------------------|-------------------------------------|-------------------------------------|-------------------|---------------------|----------------|
| ADuM2210SRWZ          | 2                                       | 0                                       | 1                        | 150                                 | 40                                  | −40°C to +125°C   | 16-Lead SOIC_W      | RW-16          |
| ADuM2210TRWZ          | 2                                       | 0                                       | 10                       | 50                                  | 3                                   | −40°C to +125°C   | 16-Lead SOIC_W      | RW-16          |
| ADuM2210SRIZ          | 2                                       | 0                                       | 1                        | 150                                 | 40                                  | −40°C to +125°C   | 16-Lead SOIC_IC     | RI-16-1        |
| ADuM2210TRIZ          | 2                                       | 0                                       | 10                       | 50                                  | 3                                   | −40°C to +125°C   | 16-Lead SOIC_IC     | RI-16-1        |
| ADuM2211SRWZ          | 1                                       | 1                                       | 1                        | 150                                 | 40                                  | −40°C to +125°C   | 16-Lead SOIC_W      | RW-16          |
| ADuM2211TRWZ          | 1                                       | 1                                       | 10                       | 50                                  | 3                                   | −40°C to +125°C   | 16-Lead SOIC_W      | RW-16          |
| ADuM2211SRIZ          | 1                                       | 1                                       | 1                        | 150                                 | 40                                  | −40°C to +125°C   | 16-Lead SOIC_IC     | RI-16-1        |
| ADuM2211TRIZ          | 1                                       | 1                                       | 10                       | 50                                  | 3                                   | −40°C to +125°C   | 16-Lead SOIC_IC     | RI-16-1        |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> Tape and reel is available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.