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ELECTRONICS

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Jameco Part Number 1743324

500mA Power Op Amp with Adjustable Precision Current Limit

FEATURES

- $\pm 500\text{mA}$ Minimum Output Current
- Independent Adjustment of Source and Sink Current Limits
- 2% Current Limit Accuracy
- Operates with Single or Split Supplies
- Shutdown/Enable Control Input
- Open Collector Status Flags:
 - Sink Current Limit
 - Source Current Limit
 - Thermal Shutdown
- Fail Safe Current Limit and Thermal Shutdown
- $1.6\text{V}/\mu\text{s}$ Slew Rate
- 3.6MHz Gain Bandwidth Product
- Fast Current Limit Response: 2MHz Bandwidth
- Specified Temperature Range: -40°C to 85°C
- Available in a 20-Lead TSSOP Package

APPLICATIONS

- Automatic Test Equipment
- Laboratory Power Supplies
- Motor Drivers
- Thermoelectric Cooler Driver

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DESCRIPTION

The LT[®]1970 is a $\pm 500\text{mA}$ power op amp with precise externally controlled current limiting. Separate control voltages program the sourcing and sinking current limit sense thresholds with 2% accuracy. Output current may be boosted by adding external power transistors.

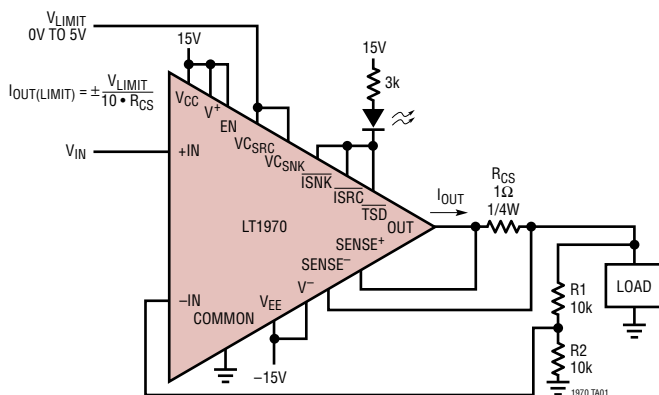
The circuit operates with single or split power supplies from 5V to 36V total supply voltage. In normal operation, the input stage supplies and the output stage supplies are connected (V_{CC} to V^+ and V_{EE} to V^-). To reduce power dissipation it is possible to power the output stage (V^+ , V^-) from independent, lower voltage rails. The amplifier is unity-gain stable with a 3.6MHz gain bandwidth product and slews at $1.6\text{V}/\mu\text{s}$. The current limit circuits operate with a 2MHz response between the VC_{SRC} or VC_{SNK} control inputs and the amplifier output.

Open collector status flags signal current limit circuit activation, as well as thermal shutdown of the amplifier. An enable logic input puts the amplifier into a low power, high impedance output state when pulled low. Thermal shutdown and a $\pm 800\text{mA}$ fixed current limit protect the chip under fault conditions.

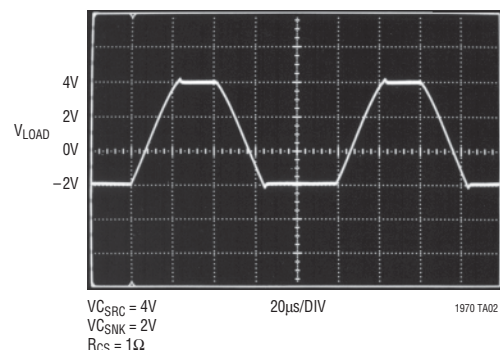
The LT1970 is packaged in a 20-lead TSSOP package with a thermally conductive copper bottom plate to facilitate heat sinking.

TYPICAL APPLICATION

$A_v = 2$ Amplifier with Adjustable $\pm 500\text{mA}$ Full-Scale Current Limit and Fault Indication



Current Limited Sinewave Into 10Ω Load



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC} to V_{EE})	36V
Positive High Current Supply (V^+)	V^- to V_{CC}
Negative High Current Supply (V^-)	V_{EE} to V^+
Amplifier Output (OUT)	V^- to V^+
Current Sense Pins (SENSE ⁺ , SENSE ⁻ , FILTER)	V^- to V^+
Logic Outputs (ISRC, ISNK, TSD)	COMMON to V_{CC}
Input Voltage (-IN, +IN)	$V_{EE} - 0.3V$ to $V_{EE} + 36V$
Input Current	10mA
Current Control Inputs (V_{CSRC} , V_{CSNK})	COMMON to COMMON + 7V
Enable Logic Input	COMMON to V_{CC}
COMMON	V_{EE} to V_{CC}
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (Note 2) ..	-40°C to 85°C
Specified Temperature Range (Note 3) ...	-40°C to 85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>FE PACKAGE 20-LEAD PLASTIC TSSOP</p> <p>$T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 40^{\circ}C/W$ (NOTE 8) EXPOSED PAD (PIN 21) IS CONNECTED TO V_{EE}</p>	ORDER PART NUMBER
	<p>LT1970CFE LT1970IFE</p>
<p>Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/</p>	

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}C$. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Op Amp Characteristics							
V_{OS}	Input Offset Voltage	$0^{\circ}C < T_A < 70^{\circ}C$	●	200	600	μV	
		$-40^{\circ}C < T_A < 85^{\circ}C$	●		1000	μV	
					1300	μV	
	Input Offset Voltage Drift (Note 4)		●	-10	-4	10	$\mu V/^{\circ}C$
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●	-100	100	nA	
I_B	Input Bias Current	$V_{CM} = 0V$	●	-600	-160	nA	
	Input Noise Voltage	0.1Hz to 10Hz		3		μV_{P-P}	
e_n	Input Noise Voltage Density	1kHz		15		nV/\sqrt{Hz}	
i_n	Input Noise Current Density	1kHz		3		pA/\sqrt{Hz}	
R_{IN}	Input Resistance	Common Mode		500		k Ω	
		Differential Mode		100		k Ω	
C_{IN}	Input Capacitance	Pin 8 and Pin 9 to Ground		6		pF	
V_{CM}	Input Voltage Range	Typical	●	-14.5	13.6	V	
		Guaranteed by CMRR Test	●	-12.0	12.0	V	
CMRR	Common Mode Rejection Ratio	$-12V < V_{CM} < 12V$	●	92	105	dB	
PSRR	Power Supply Rejection Ratio	$V_{EE} = V^- = -5V$, $V_{CC} = V^+ = 3V$ to 30V	●	90	100	dB	
		$V_{EE} = V^- = -5V$, $V_{CC} = 30V$, $V^+ = 2.5V$ to 30V	●	110	130	dB	
		$V_{EE} = V^- = -3V$ to -30V, $V_{CC} = V^+ = 5V$	●	90	100	dB	
		$V_{EE} = -30V$, $V^- = -2.5V$ to -30V, $V_{CC} = V^+ = 5V$	●	110	130	dB	

ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$R_L = 1\text{k}, -12.5\text{V} < V_{OUT} < 12.5\text{V}$	100	150		V/mV
			75			V/mV
		$R_L = 100\Omega, -12.5\text{V} < V_{OUT} < 12.5\text{V}$	80	120		V/mV
			40			V/mV
		$R_L = 10\Omega, -5\text{V} < V_{OUT} < 5\text{V}, V^+ = -V^- = 8\text{V}$	20	45		V/mV
			5			V/mV
V_{OL}	Output Sat Voltage Low	$V_{OL} = V_{OUT} - V^-$ $R_L = 100, V_{CC} = V^+ = 15\text{V}, V_{EE} = V^- = -15\text{V}$ $R_L = 10, V_{CC} = -V_{EE} = 15\text{V}, V^+ = -V^- = 5\text{V}$		1.9 0.8	2.5	V V
V_{OH}	Output Sat Voltage High	$V_{OH} = V^+ - V_{OUT}$ $R_L = 100, V_{CC} = V^+ = 15\text{V}, V_{EE} = V^- = -15\text{V}$ $R_L = 10, V_{CC} = -V_{EE} = 15\text{V}, V^+ = -V^- = 5\text{V}$		1.7 1.0	2.3	V V
I_{SC}	Output Short-Circuit Current	Output Low, $R_{SENSE} = 0\Omega$ Output High, $R_{SENSE} = 0\Omega$	500 -1000	800 -800	1200 -500	mA mA
SR	Slew Rate	$-10\text{V} < V_{OUT} < 10\text{V}, R_L = 1\text{k}$	0.7	1.6		V/ μs
FPBW	Full Power Bandwidth	$V_{OUT} = 10V_{PEAK}$ (Note 5)	11			kHz
GBW	Gain Bandwidth Product	$f = 10\text{kHz}$		3.6		MHz
t_s	Settling Time	0.01%, $V_{OUT} = 0\text{V}$ to $10\text{V}, A_V = -1, R_L = 1\text{k}$		8		μs

Current Sense Characteristics

$V_{SENSE(MIN)}$	Minimum Current Sense Voltage	$V_{CSRC} = V_{CSNK} = 0\text{V}$	0.1	4	7	mV
			0.1		10	mV
$V_{SENSE(4\%)}$	Current Sense Voltage 4% of Full Scale	$V_{CSRC} = V_{CSNK} = 0.2\text{V}$	15	20	25	mV
$V_{SENSE(10\%)}$	Current Sense Voltage 10% of Full Scale	$V_{CSRC} = V_{CSNK} = 0.5\text{V}$	45	50	55	mV
$V_{SENSE(FS)}$	Current Sense Voltage 100% of Full Scale	$V_{CSRC} = V_{CSNK} = 5\text{V}$	490	500	510	mV
			480	500	520	mV
I_{BI}	Current Limit Control Input Bias Current	V_{CSRC}, V_{CSNK} Pins	-1	-0.2	0.1	μA
I_{SENSE^-}	SENSE ⁻ Input Current	$0\text{V} < (V_{CSRC}, V_{CSNK}) < 5\text{V}$	-500		500	nA
I_{FILTER}	FILTER Input Current	$0\text{V} < (V_{CSRC}, V_{CSNK}) < 5\text{V}$	-500		500	nA
I_{SENSE^+}	SENSE ⁺ Input Current	$V_{CSRC} = V_{CSNK} = 0\text{V}$	-500		500	nA
		$V_{CSRC} = 5\text{V}, V_{CSNK} = 0\text{V}$	200	250	300	μA
		$V_{CSRC} = 0\text{V}, V_{CSNK} = 5\text{V}$	-300	-250	-200	μA
		$V_{CSRC} = V_{CSNK} = 5\text{V}$	-25		25	μA
	Current Sense Change with Output Voltage	$V_{CSRC} = V_{CSNK} = 5\text{V}, -12.5\text{V} < V_{OUT} < 12.5\text{V}$		± 0.1		%
	Current Sense Change with Supply Voltage	$V_{CSRC} = V_{CSNK} = 5\text{V}, 6\text{V} < (V_{CC}, V^+) < 18\text{V}$ $2.5\text{V} < V^+ < 18\text{V}, V_{CC} = 18\text{V}$ $-18\text{V} < (V_{EE}, V^-) < -2.5\text{V}$ $-18\text{V} < V^- < -2.5\text{V}, V_{EE} = -18\text{V}$		± 0.05		%
				± 0.01		%
				± 0.05		%
				± 0.01		%
	Current Sense Bandwidth			2		MHz
R_{CSF}	Resistance FILTER to SENSE ⁻		750	1000	1250	Ω

Logic I/O Characteristics

	Logic Output Leakage $\overline{ISRC}, \overline{ISNK}, \overline{TSD}$	$V = 15\text{V}$			1	μA
	Logic Low Output Level	$I = 5\text{mA}$ (Note 6)		0.2	0.4	V
	Logic Output Current Limit			25		mA
V_{ENABLE}	Enable Logic Threshold		0.8	1.9	2.5	V
I_{ENABLE}	Enable Pin Bias Current		-1		1	μA

ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SUPPLY}	Total Supply Current	V_{CC} , V^+ and V^- , V_{EE} Connected ●		7	13	mA
I_{CC}	V_{CC} Supply Current	V_{CC} , V^+ and V^- , V_{EE} Separate ●		3	7	mA
$I_{\text{CC}}(\text{STBY})$	Supply Current Disabled	V_{CC} , V^+ and V^- , V_{EE} Connected, $V_{\text{ENABLE}} \leq 0.8\text{V}$ ●		0.6	1.5	mA
t_{ON}	Turn-On Delay	(Note 7)		10		μs
t_{OFF}	Turn-Off Delay	(Note 7)		10		μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1970C is guaranteed functional over the operating temperature range of -40°C and 85°C .

Note 3: The LT1970C is guaranteed to meet specified performance from 0°C to 70°C . The LT1970C is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1970I is guaranteed to meet specified performance from -40°C to 85°C .

Note 4: This parameter is not 100% tested.

Note 5: Full power bandwidth is calculated from slew rate measurements: $\text{FPBW} = \text{SR} / (2 \cdot \pi \cdot V_P)$

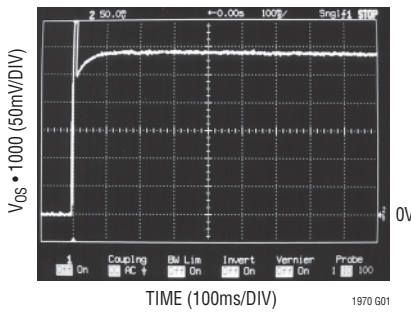
Note 6: The logic low output level of pin $\overline{\text{TSD}}$ is guaranteed by correlating the output level of pin $\overline{\text{ISRC}}$ and pin $\overline{\text{ISNK}}$ over temperature.

Note 7: Turn-on and turn-off delay are measured from V_{ENABLE} crossing 1.6V to the OUT pin at 90% of normal output voltage.

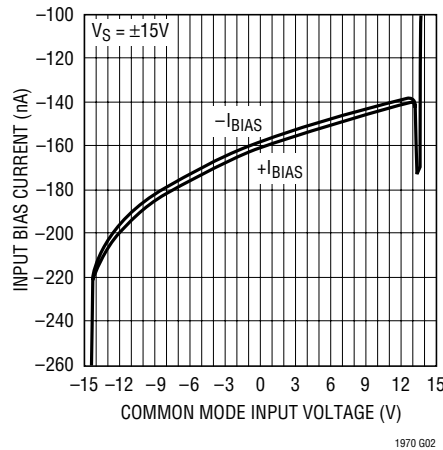
Note 8: Thermal resistance varies depending upon the amount of PC board metal attached to the device. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown and be protected.

TYPICAL PERFORMANCE CHARACTERISTICS

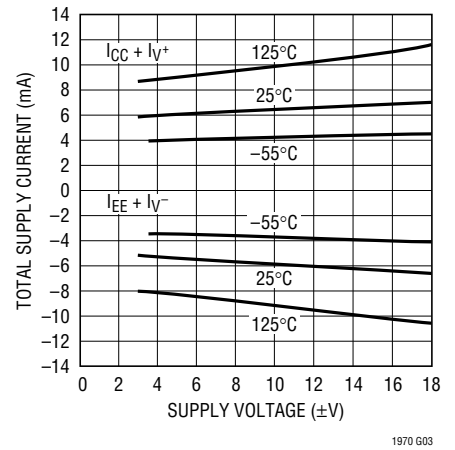
Warm-Up Drift V_{IO} vs Time



Input Bias Current vs V_{CM}

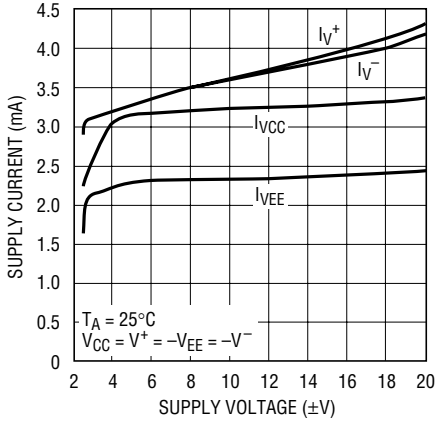


Total Supply Current vs Supply Voltage



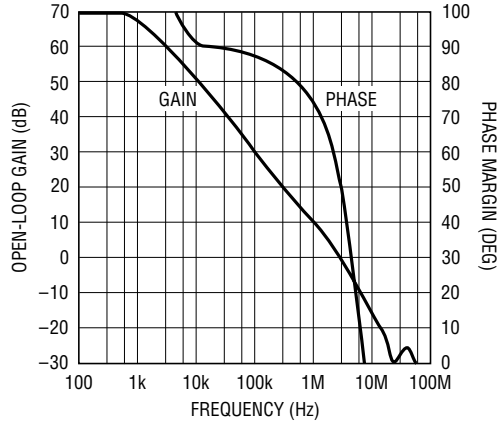
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



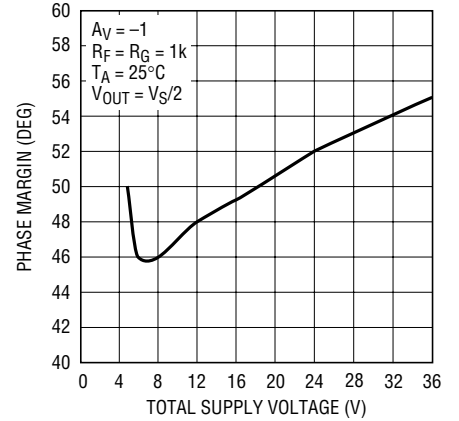
1870 G04

Open-Loop Gain and Phase vs Frequency



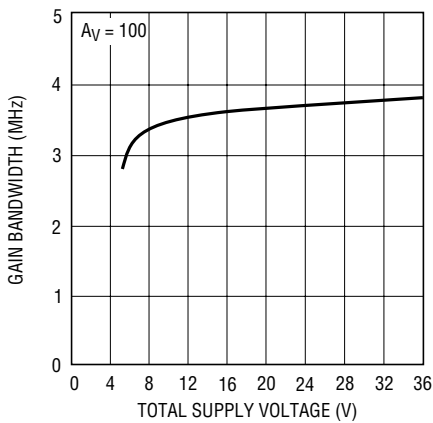
1970 G05

Phase Margin vs Supply Voltage



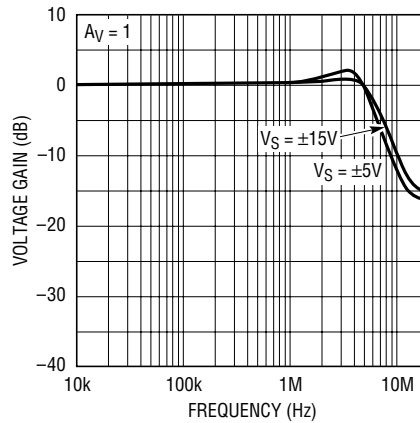
1970 G06

Gain Bandwidth vs Supply Voltage



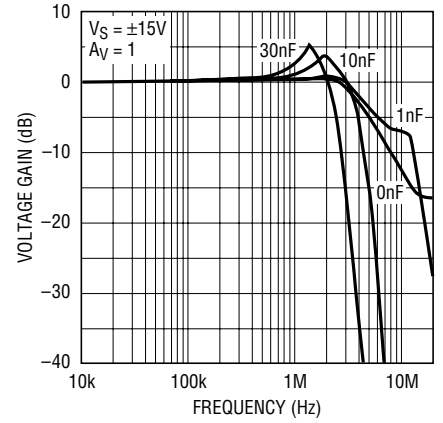
1970 G07

Gain vs Frequency



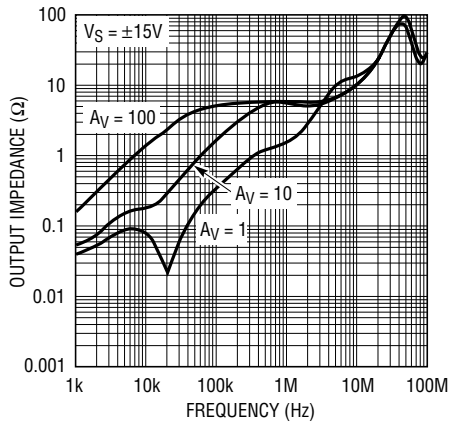
1970 G08

Gain vs Frequency with C_LOAD



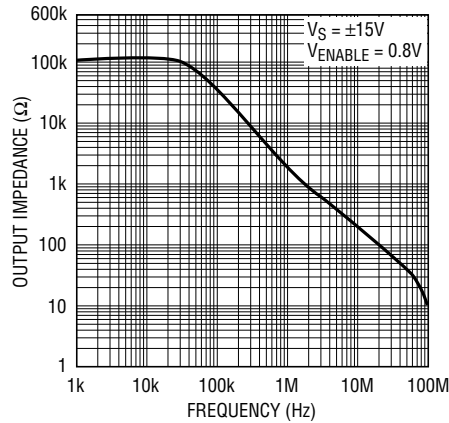
1970 G09

Output Impedance



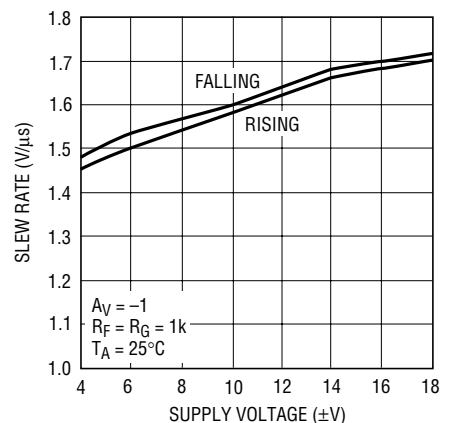
1970 G10

Disabled Output Impedance



1970 G11

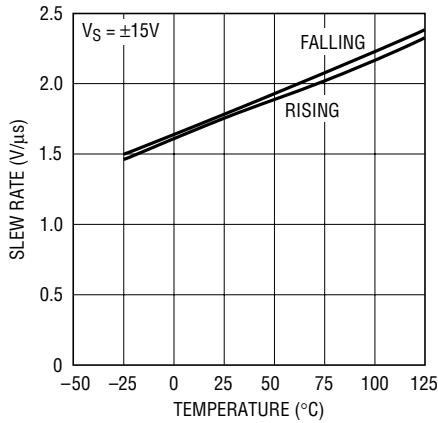
Slew Rate vs Supply Voltage



1970 G12

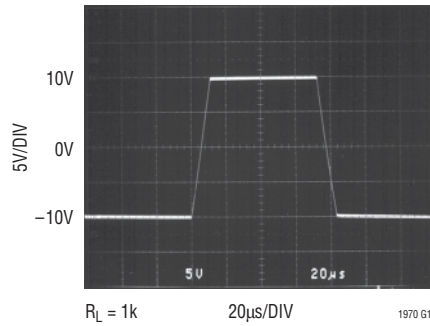
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Temperature



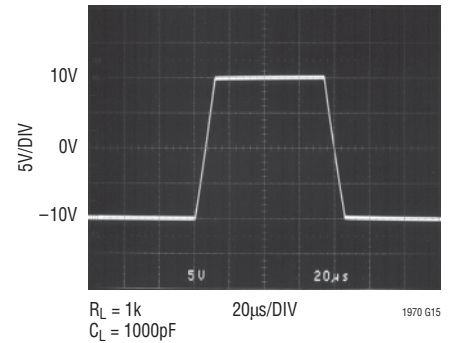
1970 G13

Large-Signal Response, $A_V = 1$



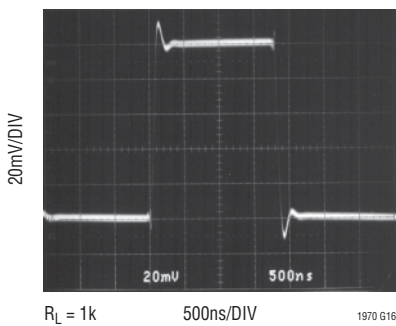
1970 G14

Large-Signal Response, $A_V = -1$



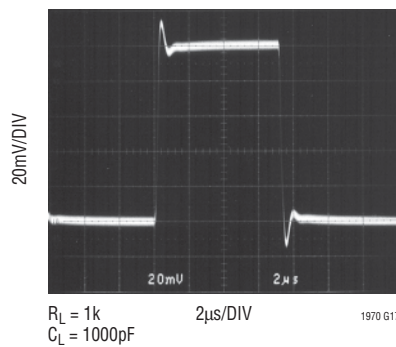
1970 G15

Small-Signal Response, $A_V = 1$



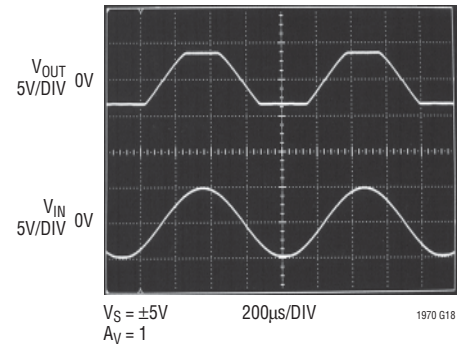
1970 G16

Small-Signal Response, $A_V = -1$



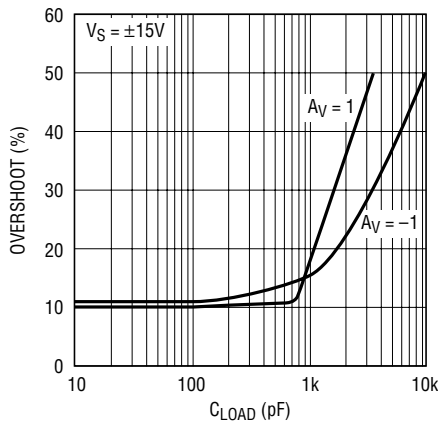
1970 G17

Output Overdriven



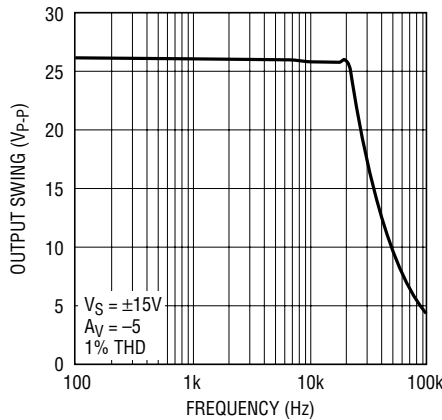
1970 G18

% Overshoot vs C_{LOAD}



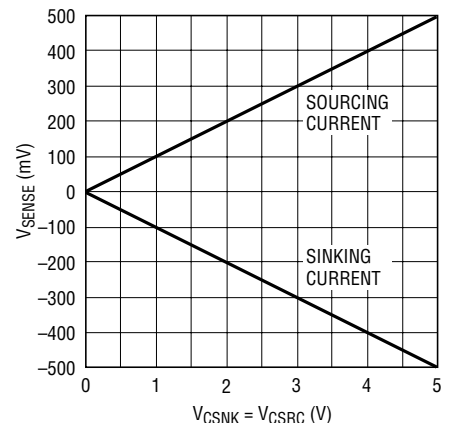
1970 G19

Undistorted Output Swing vs Frequency



1970 G20

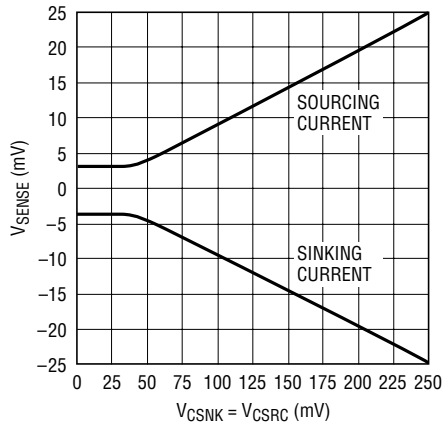
Full Range Current Sense Transfer Curve



1970 G21

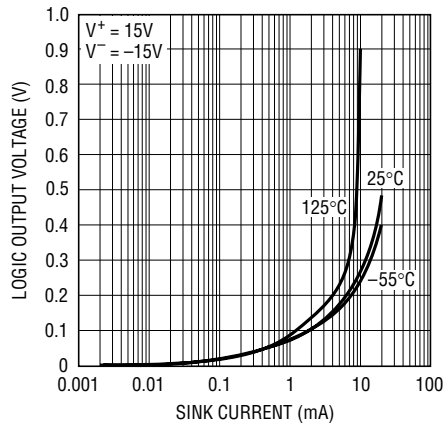
TYPICAL PERFORMANCE CHARACTERISTICS

Low Level Current Sense Transfer Curve



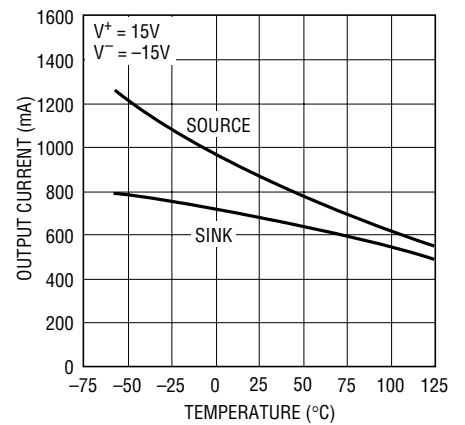
1970 G22

Logic Output Level vs Sink Current (Output Low)



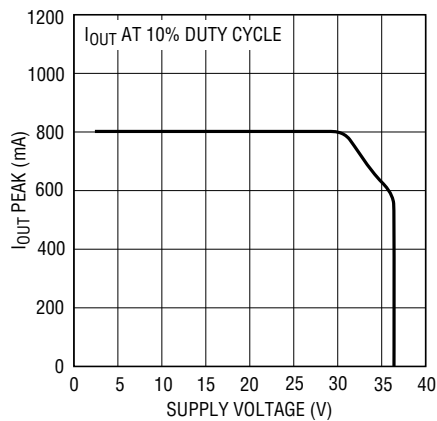
1970 G23

Maximum Output Current vs Temperature



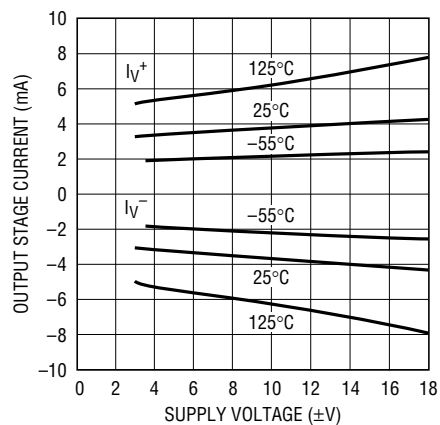
1970 G24

Safe Operating Area



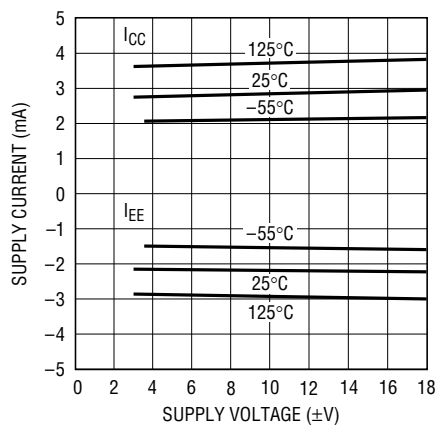
1970 G25

Output Stage Quiescent Current vs Supply Voltage



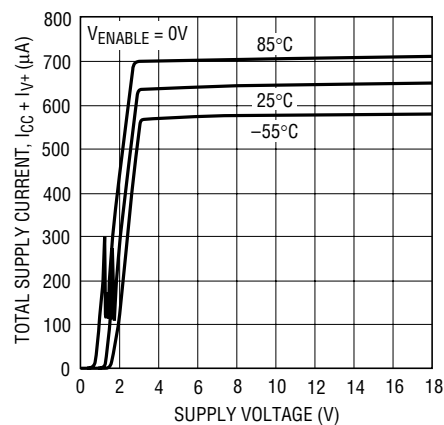
1970 G26

Control Stage Quiescent Current vs Supply Voltage



1970 G27

Supply Current vs Supply Voltage in Shutdown



1970 G28

PIN FUNCTIONS

V_{EE} (Pins 1, 10, 11, 20, Package Base): Minus Supply Voltage. V_{EE} connects to the substrate of the integrated circuit die, and therefore must always be the most negative voltage applied to the part. Decouple V_{EE} to ground with a low ESR capacitor. V_{EE} may be a negative voltage or it may equal ground potential. Any or all of the V_{EE} pins may be used. Unused V_{EE} pins must remain open.

V⁻ (Pin 2): Output Stage Negative Supply. V⁻ may equal V_{EE} or may be smaller in magnitude. Only output stage current flows out of V⁻, all other current flows out of V_{EE}. V⁻ may be used to drive the base/gate of an external power device to boost the amplifier's output current to levels above the rated 500mA of the on-chip output devices. Unless used to drive boost transistors, V⁻ should be decoupled to ground with a low ESR capacitor.

OUT (Pin 3): Amplifier Output. The OUT pin provides the force function as part of a Kelvin sensed load connection. OUT is normally connected directly to an external load current sense resistor and the SENSE⁺ pin. Amplifier feedback is directly connected to the load and the other end of the current sense resistor. The load connection is also wired directly to the SENSE⁻ pin to monitor the load current.

The OUT pin is current limited to ±800mA typical. This current limit protects the output transistor in the event that connections to the external sense resistor are opened or shorted which disables the precision current limit function.

SENSE⁺ (Pin 4): Positive Current Sense Pin. This lead is normally connected to the driven end of the external sense resistor. Sourcing current limit operation is activated when the voltage V_{SENSE} (V_{SENSE+} – V_{SENSE-}) equals 1/10 of the programming control voltage at VC_{SRC} (Pin 13). Sinking current limit operation is activated when the voltage V_{SENSE} equals –1/10 of the programming control voltage at VC_{SNK} (Pin 12).

FILTER (Pin 5): Current Sense Filter Pin. This pin is normally not used and should be left open or shorted to the SENSE⁻ pin. The FILTER pin can be used to adapt the response time of the current sense amplifiers with a 1nF to 100nF capacitor connected to the SENSE⁻ input. An internal 1k resistor sets the filter time constant.

SENSE⁻ (Pin 6): Negative Current Sense Pin. This pin is normally connected to the load end of the external sense resistor. Sourcing current limit operation is activated when the voltage V_{SENSE} (V_{SENSE+} – V_{SENSE-}) equals 1/10 of the programming control voltage at VC_{SRC} (Pin 13). Sinking current limit operation is activated when the voltage V_{SENSE} equals –1/10 of the programming control voltage at VC_{SNK} (Pin 12).

V_{CC} (Pin 7): Positive Supply Voltage. All circuitry except the output transistors draw power from V_{CC}. Total supply voltage from V_{CC} to V_{EE} must be between 3.5V and 36V. V_{CC} must always be greater than or equal to V⁺. V_{CC} should always be decoupled to ground with a low ESR capacitor.

–IN (Pin 8): Inverting Input of Amplifier. –IN may be any voltage from V_{EE} – 0.3V to V_{EE} + 36V. –IN and +IN remain high impedance at all times to prevent current flow into the inputs when current limit mode is active. Care must be taken to insure that –IN or +IN can never go to a voltage below V_{EE} – 0.3V even during transient conditions or damage to the circuit may result. A Schottky diode from V_{EE} to –IN can provide clamping if other elements in the circuit can allow –IN to go below V_{EE}.

+IN (Pin 9): Noninverting Input of Amplifier. +IN may be any voltage from V_{EE} – 0.3V to V_{EE} + 36V. –IN and +IN remain high impedance at all times to prevent current flow into the inputs when current limit mode is active. Care must be taken to insure that –IN or +IN can never go to a voltage below V_{EE} – 0.3V even during transient conditions or damage to the circuit may result. A Schottky diode from V_{EE} to +IN can provide clamping if other elements in the circuit can allow +IN to go below V_{EE}.

PIN FUNCTIONS

VC_{SNK} (Pin 12): Sink Current Limit Control Voltage Input. The current sink limit amplifier will activate when the sense voltage between SENSE⁺ and SENSE⁻ equals $-1.0 \cdot V_{VCSNK}/10$. VC_{SNK} may be set between V_{COMMON} and V_{COMMON} + 6V. The transfer function between VC_{SNK} and V_{SENSE} is linear except for very small input voltages at VC_{SNK} < 60mV. V_{SENSE} limits at a minimum set point of 4mV typical to insure that the sink and source limit amplifiers do not try to operate simultaneously. To force zero output current, the ENABLE pin can be taken low.

VC_{SRC} (Pin 13): Source Current Limit Control Voltage Input. The current source limit amplifier will activate when the sense voltage between SENSE⁺ and SENSE⁻ equals V_{VCSRC}/10. VC_{SRC} may be set between V_{COMMON} and V_{COMMON} + 6V. The transfer function between VC_{SRC} and V_{SENSE} is linear except for very small input voltages at VC_{SRC} < 60mV. V_{SENSE} limits at a minimum set point of 4mV typical to insure that the sink and source limit amplifiers do not try to operate simultaneously. To force zero output current, the ENABLE pin can be taken low.

COMMON (Pin 14): Control and ENABLE inputs and flag outputs are referenced to the COMMON pin. COMMON may be at any potential between V_{EE} and V_{CC} - 3V. In typical applications, COMMON is connected to ground.

ENABLE (Pin 15): ENABLE Digital Input Control. When taken low this TTL-level digital input turns off the amplifier output and drops supply current to less than 1mA. Use the ENABLE pin to force zero output current. Setting VC_{SNK} = VC_{SRC} = 0V allows I_{OUT} = ±4mV/R_{SENSE} to flow in or out of V_{OUT}.

ISRC (Pin 16): Sourcing Current Limit Digital Output Flag. ISRC is an open collector digital output. ISRC pulls low whenever the sourcing current limit amplifier assumes control of the output. This pin can sink up to 10mA of current. The current limit flag is off when the source

current limit is not active. ISRC, ISNK and TSD may be wired “OR” together if desired. ISRC may be left open if this function is not monitored.

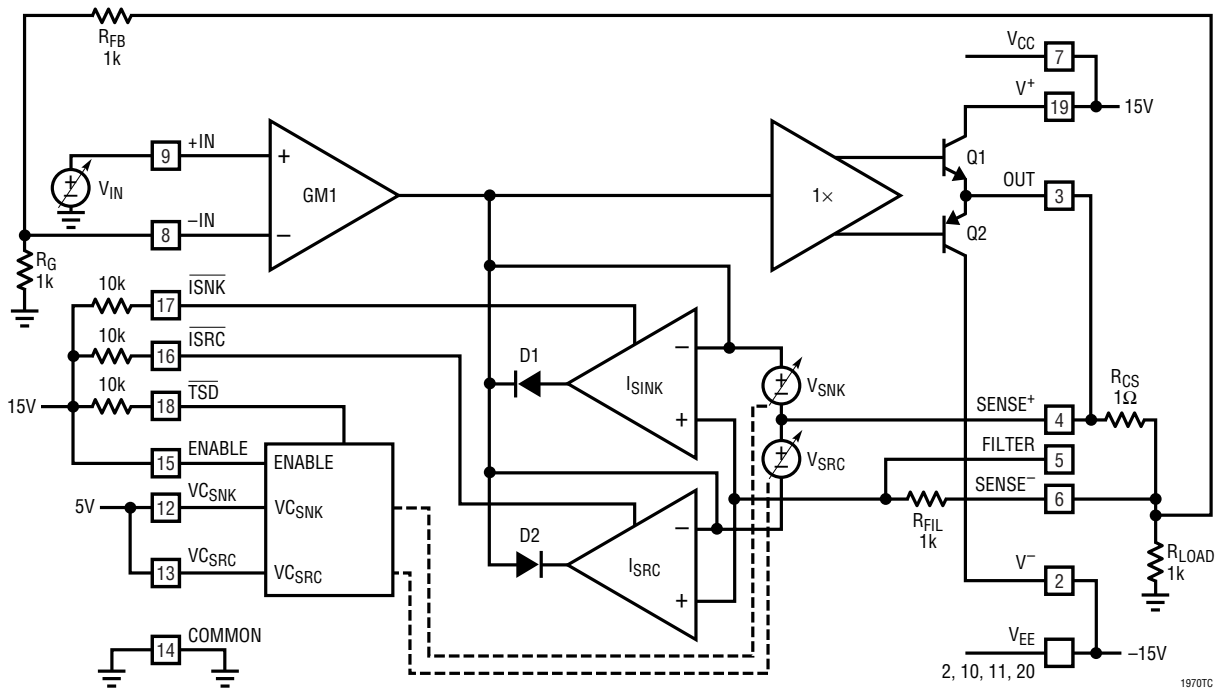
ISNK (Pin 17): Sinking Current Limit Digital Output Flag. ISNK is an open collector digital output. ISNK pulls low whenever the sinking current limit amplifier assumes control of the output. This pin can sink up to 10mA of current. The current limit flag is off when the source current limit is not active. ISRC, ISNK and TSD may be wired “OR” together if desired. ISNK may be left open if this function is not monitored.

TSD (Pin 18): Thermal Shutdown Digital Output Flag. TSD is an open collector digital output. TSD pulls low whenever the internal thermal shutdown circuit activates, typically at a die temperature of 160°C. This pin can sink up to 10mA of output current. The TSD flag is off when the die temperature is within normal operating temperatures. ISRC, ISNK and TSD may be wired “OR” together if desired. ISNK may be left open if this function is not monitored. Thermal shutdown activation should prompt the user to evaluate electrical loading or thermal environmental conditions.

V⁺ (Pin 19): Output Stage Positive Supply. V⁺ may equal V_{CC} or may be smaller in magnitude. Only output stage current flows through V⁺, all other current flows into V_{CC}. V⁺ may be used to drive the base/gate of an external power device to boost the amplifier’s output current to levels above the rated 500mA of the on-chip output devices. Unless used to drive boost transistors, V⁺ should be decoupled to ground with a low ESR capacitor.

Package Base: The exposed backside of the package is electrically connected to the V_{EE} pins on the IC die. The package base should be soldered to a heat spreading pad on the PC board that is electrically connected to V_{EE}.

BLOCK DIAGRAM AND TEST CIRCUIT



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The LT1970 power op amp with precision controllable current limit is a flexible voltage and current source module. The drawing on the front page of this data sheet is representative of the basic application of the circuit, however many alternate uses are possible with proper understanding of the subcircuit capabilities.

CIRCUIT DESCRIPTION

Main Operational Amplifier

Subcircuit block GM1, the 1X unity-gain current buffer and output transistors Q1 and Q2 form a standard operational amplifier. This amplifier has $\pm 500\text{mA}$ current output capability and a 3.6MHz gain bandwidth product. Most applications of the LT1970 will use this op amp in the main signal path. All conventional op amp circuit configurations are supported. Inverting, noninverting, filter, summation or nonlinear circuits may be implemented in a conventional manner. The output stage includes current limiting at $\pm 800\text{mA}$ to protect against fault conditions. The input stage has high differential breakdown of 36V minimum

between $-IN$ and $+IN$. No current will flow at the inputs when differential input voltage is present. This feature is important when the precision current sense amplifiers “ I_{SINK} ” and “ I_{SRC} ” become active.

Current Limit Amplifiers

Amplifier stages “ I_{SINK} ” and “ I_{SRC} ” are very high transconductance amplifier stages with independently controlled offset voltages. These amplifiers monitor the voltage between input pins $SENSE^+$ and $SENSE^-$ which usually sense the voltage across a small external current sense resistor. The transconductance amplifiers outputs connect to the same high impedance node as the main input stage GM1 amplifier. Small voltage differences between $SENSE^+$ and $SENSE^-$, smaller than the user set $VC_{SNK}/10$ and $VC_{SRC}/10$ in magnitude, cause the current limit amplifiers to decouple from the signal path. This is functionally indicated by diodes D1 and D2 in the Block Diagram. When the voltage V_{SENSE} increases in magnitude sufficient to equal or overcome one of the offset voltages $VC_{SNK}/10$ or $VC_{SRC}/10$, the appropriate current limit amplifier becomes active and because of

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its very high transconductance, takes control from the input stage, GM1. The output current is regulated to a value of $I_{OUT} = V_{SENSE}/R_{SENSE} = (V_{CSRC} \text{ or } V_{CSNK})/(10 \cdot R_{SENSE})$. The time required for the current limit amplifiers to take control of the output is typically 4 μ s.

Linear operation of the current limit sense amplifier occurs with the inputs SENSE⁺ and SENSE⁻ ranging between $V_{CC} - 1.5V$ and $V_{EE} + 1.5V$. Most applications will connect pins SENSE⁺ and OUT together, with the load on the opposite side of the external sense resistor and pin SENSE⁻. Feedback to the inverting input of GM1 should be connected from SENSE⁻ to -IN. Ground side sensing of load current may be employed by connecting the load between pins OUT and SENSE⁺. Pin SENSE⁻ would be connected to ground in this instance. Load current would be regulated in exactly the same way as the conventional connection. However, voltage mode accuracy would be degraded in this case due to the voltage across R_{SENSE} .

Creative applications are possible where pins SENSE⁺ and SENSE⁻ monitor a parameter other than load current. The operating principle that at most one of the current limit stages may be active at one time, and that when active, the current limit stages take control of the output from GM1, can be used for many different signals.

Current Limit Threshold Control Buffers

Input pins V_{CSNK} and V_{CSRC} are used to set the response thresholds of current limit amplifiers “ I_{SINK} ” and “ I_{SRC} ”. Each of these inputs may be independently driven by a voltage of 0V to 5V above the COMMON reference pin. The 0V to 5V input voltage is attenuated by a factor of 10 and applied as an offset to the appropriate current limit amplifier. AC signals may be applied to these pins. The AC bandwidth from a V_C pin to the output is typically 2MHz. For proper operation of the LT1970, these control inputs cannot be left floating.

For low V_{CC} supply applications it is important to keep the maximum input control voltages, V_{CSRC} and V_{CSNK} , at least 2.5V below the V_{CC} potential. This ensures linear control of the current limit threshold. Reducing the current limit sense resistor value allows high output current from a smaller control voltage which may be necessary if the V_{CC} supply is only 5V.

The transfer function from V_C to the associated V_{OS} is linear from about 0.1V to 5V in, or 10mV to 500mV at the current limit amplifier inputs. An intentional nonlinearity is built into the transfer functions at low levels. This nonlinearity insures that both the sink and source limit amplifiers cannot become active simultaneously. Simultaneous activation of the limit amplifiers could result in uncontrolled outputs. As shown in the Typical Performance Characteristics curves, the control inputs have a “hockey stick” shape, to keep the minimum limit threshold at 4mV for each limit amplifier.

Figure 1 illustrates an interesting use of the current sense input pins. Here the current limit control amplifiers are used to produce a symmetrically limited output voltage swing. Instead of monitoring the output current, the output voltage is divided down by a factor of 20 and applied to the SENSE⁺ input, with the SENSE⁻ input grounded. When the threshold voltage between SENSE⁺ and SENSE⁻ ($V_{CLAMP}/10$) is reached, the current limit stage takes control of the output and clamps it a level of $\pm 2 \cdot V_{CLAMP}$. With control inputs V_{CSRC} and V_{CSNK} tied together, a single polarity input voltage sets the same + and - output limit voltage for symmetrical limiting. In this circuit the output will current limit at the built-in fail-safe level of typically 800mA.

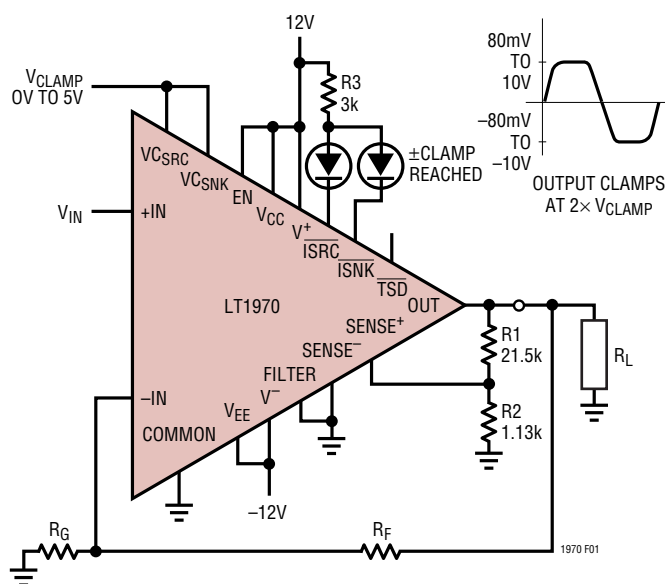


Figure 1. Symmetrical Output Voltage Limiting

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ENABLE Control

The ENABLE input pin puts the LT1970 into a low supply current, high impedance output state. The ENABLE pin responds to TTL threshold levels with respect to the COMMON pin. Pulling the ENABLE pin low is the best way to force zero current at the output. Setting $V_{CSNK} = V_{CSRC} = 0V$ allows the output current to remain as high as $\pm 4mV/R_{SENSE}$.

In applications such as circuit testers (ATE), it may be preferable to apply a predetermined test voltage with a preset current limit to a test node simultaneously. The ENABLE pin can be used to provide this gating action as shown in Figure 2. While the LT1970 is disabled, the load is essentially floating and the input voltage and current limit control voltages can be set to produce the load test levels. Enabling the LT1970 then drives the load. The LT1970 enables and disables in just a few microseconds. The actual enable and disable times at the load are a function of the load reactance.

Operating Status Flags

The LT1970 has three digital output indicators; \overline{TSD} , \overline{ISRC} and \overline{ISNK} . These outputs are open collector drivers referred to the COMMON pin. The outputs have 36V capabilities and can sink in excess of 10mA. \overline{ISRC} and \overline{ISNK}

indicate activation of the associated current limit amplifier. The \overline{TSD} output indicates excessive die temperature has caused the circuit to enter thermal shutdown. The three digital outputs may be wire "OR'd" together, monitored individually or left open. These outputs do not affect circuit operation, but provide an indication of the present operational status of the chip.

For slow varying output signals, the assertion of a low level at the current limit output flags occurs when the current limit threshold is reached. For fast moving signals where the LT1970 output is moving at the slew limit, typically $1.6V/\mu s$, the flag assertion can be somewhat premature at typically 75% of the actual current limit value.

The operating status flags are designed to drive LEDs to provide a visual indication of current limit and thermal conditions. As such, the transition edges to and from the active low state are not particularly sharp and may exhibit some uncertainty. Adding some positive feedback to the current limit control inputs helps to sharpen these transitions.

With the values shown in Figure 3, the current limit threshold is reduced by approximately 0.5% when either current limit status flag goes low. With sharp logic transitions, the status outputs can be used in a system control

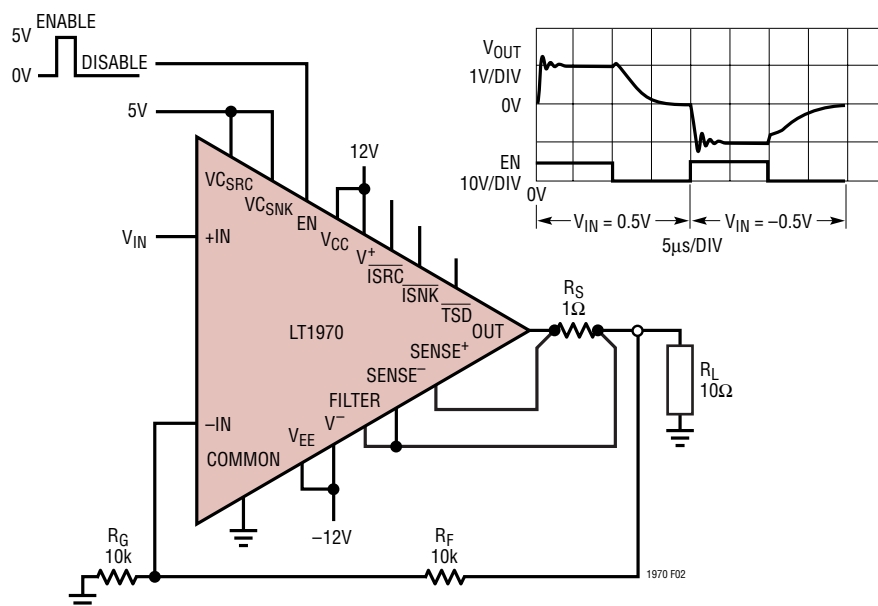


Figure 2. Using the ENABLE pin

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loop to take protective measures when a current limit condition is detected automatically.

The current limit status flag can also be used to produce a dramatic change in the current limit value of the amplifier. Figure 4 illustrates a “snap-back” current limiting characteristic. In this circuit, a simple resistor network

initially sets a high value of current limit (500mA). The circuit operates normally until the signal is large enough to enter current limit. When either current limit flag goes low, the current limit control voltage is reduced by a factor of 10. This then forces a low level of output current (50mA) until the signal is reduced in magnitude. When the load current drops below the lower level, the current limit is then restored to the higher value. This action is similar to a self resettable fuse that trips at dangerously high current levels and resets only when conditions are safe to do so.

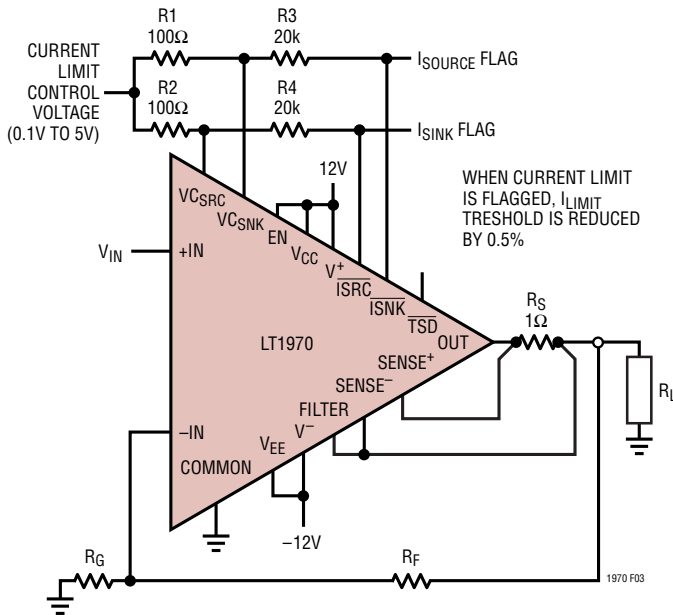


Figure 3. Adding Positive Feedback to Sharpen the Transition Edges of the Current Limit Status Flags

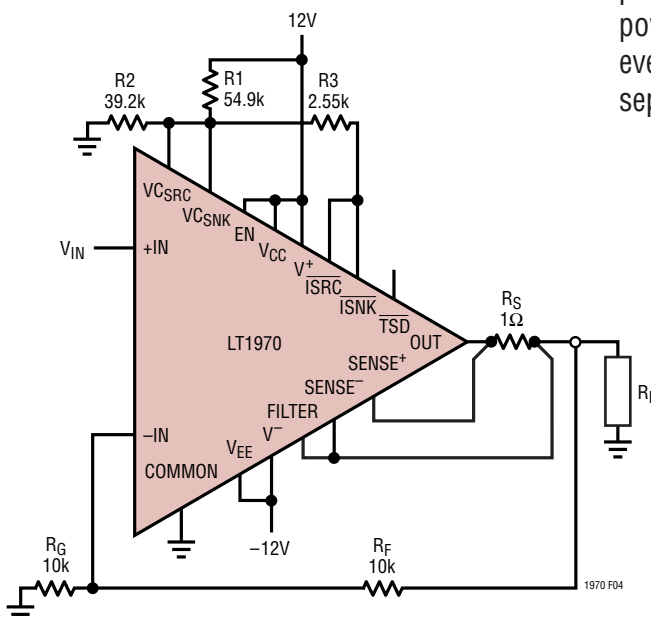


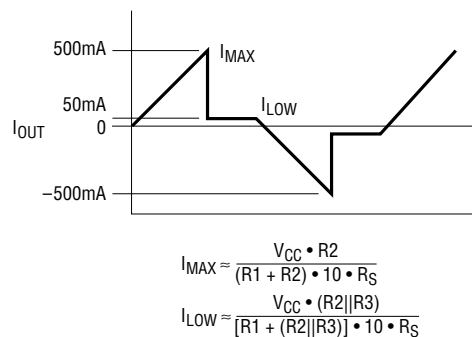
Figure 4. “Snap-Back” Current Limiting

THERMAL MANAGEMENT

Minimizing Power Dissipation

The LT1970 can operate with up to 36V total supply voltage with output currents up to $\pm 500\text{mA}$. The amount of power dissipated in the chip could approach 18W under worst-case conditions. This amount of power will cause die temperature to rise until the circuit enters thermal shutdown. While the thermal shutdown feature prevents damage to the circuit, normal operation is impaired. Thermal design of the LT1970 operating environment is essential to getting maximum utility from the circuit.

The first concern for thermal management is minimizing the heat which must be dissipated. The separate power pins V^+ and V^- can be a great aid in minimizing on-chip power. The output pin can swing to within 1.0V of V^+ or V^- even under maximum output current conditions. Using separate power supplies, or voltage regulators, to set V^+



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and V^- to their minimum values for the required output swing will minimize power dissipation. The supplies V_{CC} and V_{EE} may also be reduced to a minimal value, but these supply pins do not carry high currents, and the power saving is much less. V_{CC} and V_{EE} must be greater than the maximum output swing by 1.5V or more.

When V^- and V^+ are provided separately from V_{CC} and V_{EE} , care must be taken to insure that V^- and V^+ are always less than or equal to the main supplies in magnitude. Protection Schottky diodes may be required to insure this in all cases, including power on/off transients.

Operation with reduced V^+ and V^- supplies does not affect any performance parameters except maximum output swing. All DC accuracy and AC performance specifications guaranteed with $V_{CC} = V^+$ and $V_{EE} = V^-$ are still valid with the reduced output signal swing range.

Heat Sinking

The power dissipated in the LT1970 die must have a path to the environment. With 100°C/W thermal resistance in free air with no heat sink, the package power dissipation is limited to only 1W. The 20-pin TSSOP package with exposed copper underside is an efficient heat conductor if it is effectively mounted on a PC board. Thermal resistances as low as 40°C/W can be obtained by soldering the bottom of the package to a large copper pattern on the PC board. For operation at 85°C, this allows up to 1.625W of power to be dissipated on the LT1970. At 25°C operation, up to 3.125W of power dissipation can be achieved. The PC board heat spreading copper area must be connected to V_{EE} .

Figure 5 shows examples of PCB metal being used for heat spreading. These are provided as a reference for what might be expected when using different combinations of metal area on different layers of a PCB. These examples are with a 4-layer board using 1oz copper on each layer. The most effective layers for spreading heat are those closest to the LT1970 junction. Soldering the exposed thermal pad of the TSSOP package to the board produces a thermal resistance from junction-to-case of approximately 3°C/W.

As a minimum, the area directly beneath the package on all PCB layers can be used for heat spreading. However, limiting the area to that of the metal heat sinking pad is not

very effective. Expanding the area on various layers significantly reduces the overall thermal resistance. The addition of vias (small 13 mil holes which fill during PCB plating) connecting all layers of metal also helps reduce the operating temperature of the LT1970. These are also shown in Figure 5.

It is important to note that the metal planes used for heat sinking are connecting electrically to V_{EE} . These planes must be isolated from any other power planes used in the PCB design.

Another effective way to control the power amplifier operating temperature is to use airflow over the board. Airflow can significantly reduce the total thermal resistance as also shown in Figure 5.

DRIVING REACTIVE LOADS











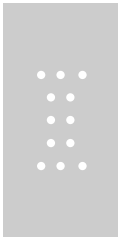
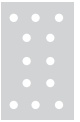
Capacitive Loads

The LT1970 is much more tolerant of capacitive loading than most operational amplifiers. In a worst-case configuration as a voltage follower, the circuit is stable for capacitive loads less than 2.5nF. Higher gain configurations improve the C_{LOAD} handling. If very large capacitive loads are to be driven, a resistive decoupling of the amplifier from the capacitive load is effective in maintaining stability and reducing peaking. The current sense resistor, usually connected between the output pin and the load can serve as a part of the decoupling resistance.

Inductive Loads

Load inductance is usually not a problem at the outputs of operational amplifiers, but the LT1970 can be used as a high output impedance current source. This condition may be the main operating mode, or when the circuit enters a protective current limit mode. Just as load capacitance degrades the phase margin of normal op amps, load inductance causes a peaking in the loop response of the feedback controlled current source. The inductive load may be caused by long lead lengths at the amplifier output. If the amplifier will be driving inductive loads or long lead lengths (greater than 4 inches) a 500pF capacitor from the SENSE⁻ pin to the ground plane will cancel the inductive load and ensure stability.

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STILL AIR θ_{JA}	PACKAGE	TOP LAYER	2ND LAYER	3RD LAYER	BOTTOM LAYER
TSSOP 100°C/W					
TSSOP 50°C/W					
TSSOP 45°C/W					

1970 F05a

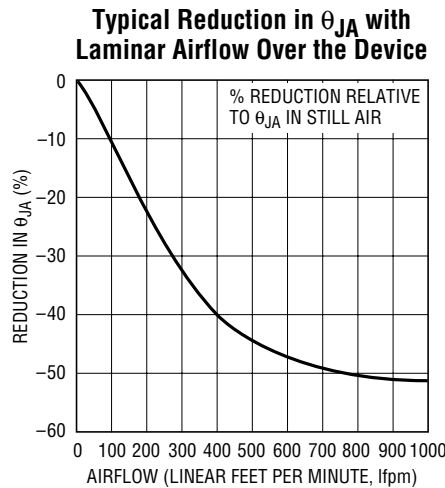


Figure 5. Examples of PCB Metal Used for Heat Dissipation. Driver Package Mounted on Top Layer. Heat Sink Pad Soldered to Top Layer Metal. Metal Areas Drawn to Scale of Package Size

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Figure 6 shows the LT1970 driving an inductive load with a controlled amount of current. This load is shown as a generic magnetic transducer, which could be used to create and modulate a magnetic field. Driving the current limit control inputs directly forces a current through the load that could range up to 2MHz in modulation. Biasing the input stage to the midpoint of the modulation signal allows symmetrical bidirectional current flow through the load. Clamp diodes are added to protect the LT1970 output from large inductive flyback potentials caused by rapid di/dt changes.

Abrupt Load Short Protection

An abrupt short-circuit connection, often referred to as screwdriver or crowbar short, to ground or other supply potentials is the worst-case load condition for the LT1970. The current limit sense amplifier normally operates with an input voltage differential equal to the voltage across the sense resistor, which is only 500mV maximum in a typical application. During an abrupt load short to ground, the load end of the sense resistor is immediately connected to ground while the amplifier output remains at the normal output voltage. This can impose a large differential voltage to the sense amplifier inputs for a brief period. If this delta V can be greater than $\pm 2V$, it is beneficial to add clamps between the current limit sense amplifier inputs. These clamps ensure a smooth transition from the main amplifier control to the current limit amplifier control under all load short conditions that may arise.

Figure 7 shows the connection of these back-to-back clamp diodes between the FILTER pin and the SENSE+ pin. With this connection, the internal 1k resistor between the SENSE- pin and the FILTER pin limits the diode current. The BAV99 diodes are small SOT-23 packaged general purpose silicon diodes. The maximum current limit sense voltage is now the diode voltage drop, determined by the voltage across the sense resistor and the 1k internal resistor. As the diode begins to conduct current, with a voltage drop of around 300mV, an error in the expected current limit level at the high end of the control becomes

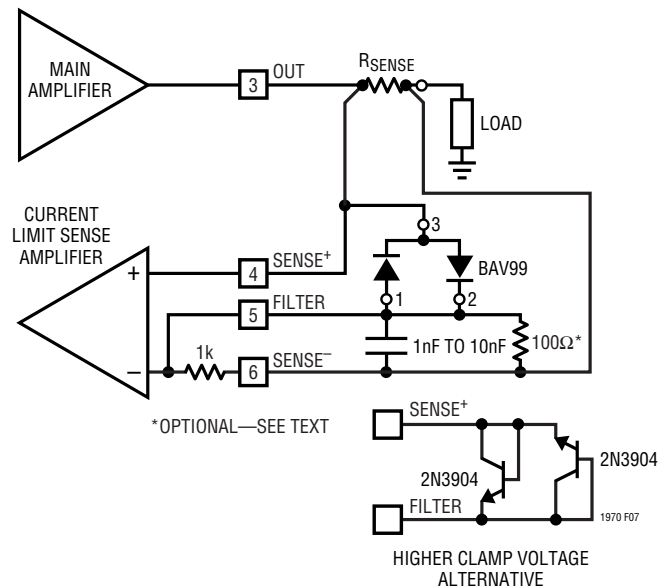


Figure 7. Adding Protection for Abrupt Load Shorts

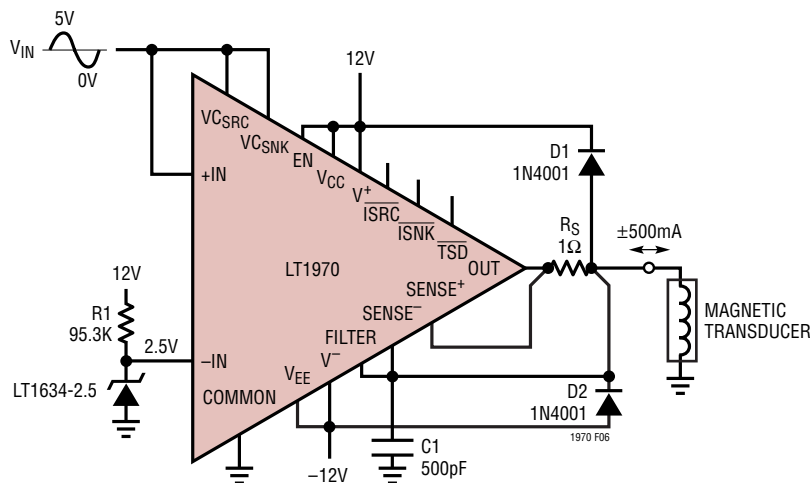


Figure 6. Current Modulation of a Magnetic Transducer

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apparent, as V_{DIODE} is less than the voltage across R_{SENSE} . Adding an optional external 100Ω resistor in parallel with the internal $1k$ resistor forces the diode voltage closer to the sensed current limit voltage and reduces the current limit error.

Alternatively, the base-emitter junctions of back-to-back 2N3904 NPN transistors can provide this clamping action. These diodes begin to conduct at a higher voltage level nearer to $600mV$. With a $500mV$ maximum current limit threshold very little error will be noticed. Comparisons of typical current limit error with three ways of adding clamping protection are shown in Figure 8. Scaling the current sense resistor and the current limit control voltage down so that a $0V$ to $300mV$ current limit sense voltage range also prevents these accuracy errors caused by the abrupt-short clamping diodes.

Also shown in Figure 7 is a small filtering capacitor. This too provides an extra measure of control under abrupt load shorting conditions. A fast short-circuit makes apparent all parasitic interconnect lead inductances between the LT1970 and the load. These distributed parasitic elements can cause significant transient voltage spikes in the short time after the application or removal of a short circuit. These uncontrolled voltage transients could actually couple back to the current limit amplifier and cause polarity reversal from sourcing current limit to sinking or vice versa. This can act as positive feedback and cause the

current limit amplifier to go to the incorrect current limit direction and hang up. Adding a small filter capacitor between the $SENSE^-$ and $FILTER$ pins, $1nF$ to $10nF$ is fairly typical, which charges through the clamp diodes forces the correct current limit polarity at the instant of the load short. This holds the amplifier in current limit until the capacitor discharges through the internal $1k$ resistor, eliminating transient induced behavior and creating a smooth transition into current limit.

Supply Bypassing

The LT1970 can supply large currents from the power supplies to a load at frequencies up to $4MHz$. Power supply impedance must be kept low enough to deliver these currents without causing supply rails to droop. Low ESR capacitors, such as $0.1\mu F$ or $1\mu F$ ceramics, located close to the pins are essential in all applications. When large, high speed transient currents are present additional capacitance may be needed near the chip. Check supply rails with a scope and if signal related ripple is seen on the supply rail, increase the decoupling capacitor as needed.

To ensure proper start-up biasing of the LT1970, it is recommended that the rate of change of the supply voltages at turn-on be limited to be no faster than $6V/\mu s$.

Application Circuit Ideas

The digitally controlled analog pin driver is shown in Figure 9. All of the control signals are provided by an LTC[®]1664 quad, 10-bit DAC by way of a 3-wire serial interface. The LT1970 is configured as a simple difference amplifier with a gain of 3. This gain is required to produce $\pm 15V$ from the $0V$ to $5V$ outputs from DACs C and D. To provide voltage headroom, the supplies for the LT1970 are set to the maximum value of $\pm 18V$. As $\pm 18V$ is the absolute maximum rating of supply voltage for the LT1970, care must be taken to not allow the supply voltage to increase. DACs A and B separately control the sinking and sourcing current limit to the load over the range of $\pm 4mA$ to $\pm 500mA$. An optional ON/OFF control for the pin driver using the ENABLE input is shown. If always enabled the ENABLE pin should be tied to V_{CC} .

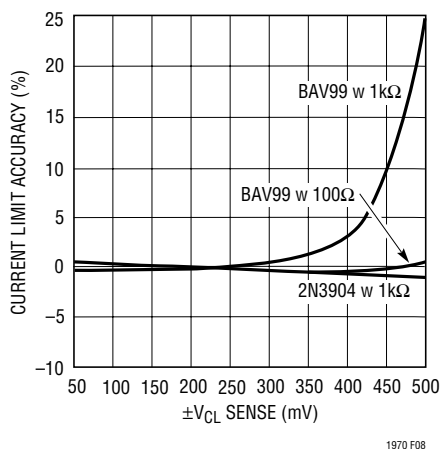


Figure 8. Current Limit Accuracy with Different Clamps

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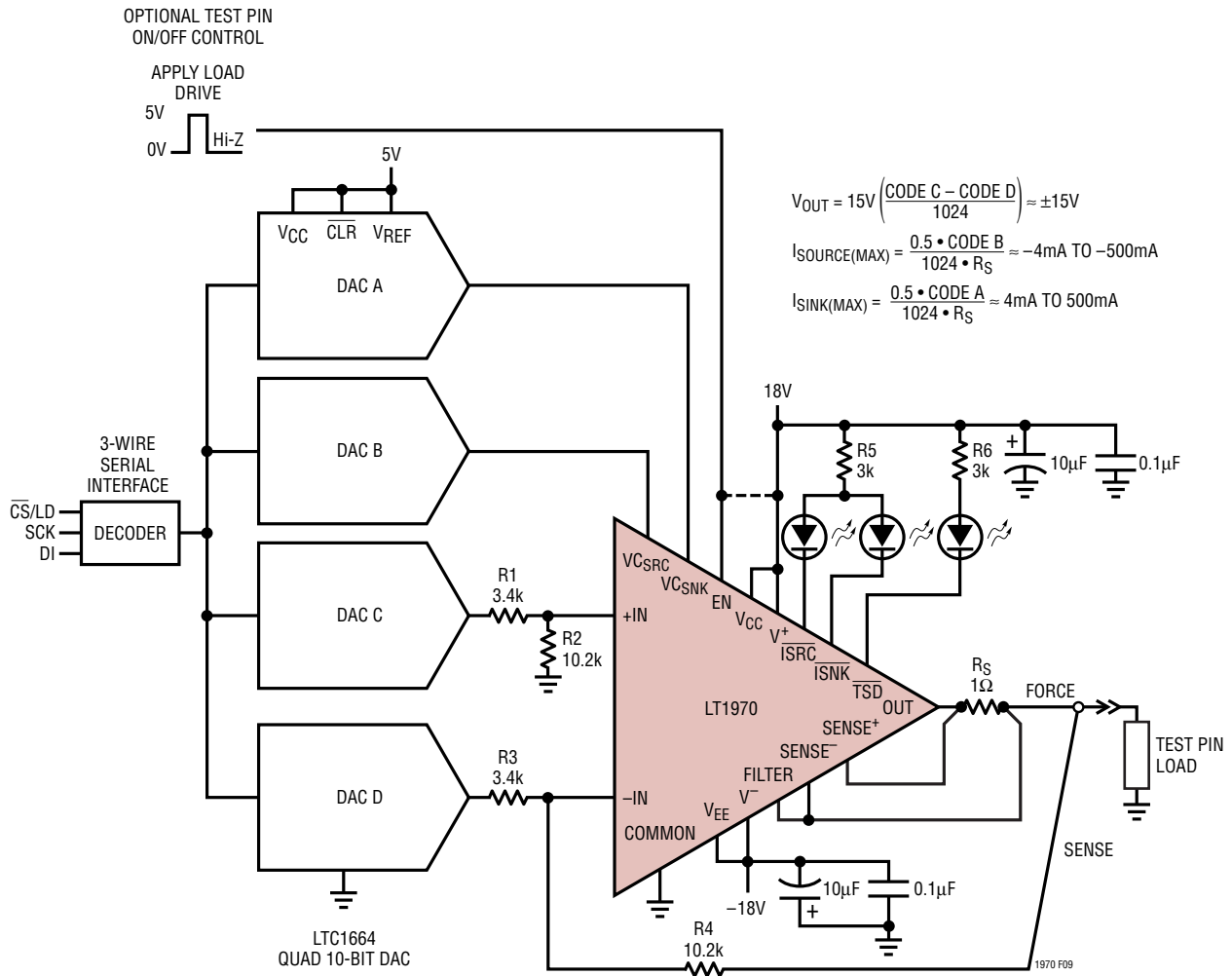


Figure 9. Digitally Controlled Analog Pin Driver

In some applications it may be necessary to know what the current into the load is at any time. Figure 10 shows an LT1787 high side current sense amplifier monitoring the current through sense resistor R_S . The LT1787 is biased from the V_{EE} supply to accommodate the common mode input range of $\pm 10V$. The sense resistor is scaled down to provide a 100mV maximum differential signal to the current sense amplifier to preserve linearity. The LT1880 amplifier provides gain and level shifting to produce a 0V to 5V output signal ($2.5V \text{ DC} \pm 5mV/mA$) with up to 1kHz full-scale bandwidth. An A/D converter could then digitize this instantaneous current reading to provide digital feedback from the circuit.

The LT1970 is just as easy to use as a standard operational amplifier. Basic amplification of a precision reference voltage creates a very simple bench DC power supply as shown in Figure 11. The built-in power stage produces an adjustable 0V to 25V at 4mA to 100mA of output current. Voltage and current adjustments are derived from the LT1634-5 5V reference. The output current capability is 500mA, but this supply is restricted to 100mA for power dissipation reasons. The worst-case output voltage for maximum power dissipated in the LT1970 output stage occurs if the output is shorted to ground or set to a voltage near zero. Limiting the output current to 100mA sets the maximum power dissipation to 3W. To allow the output to

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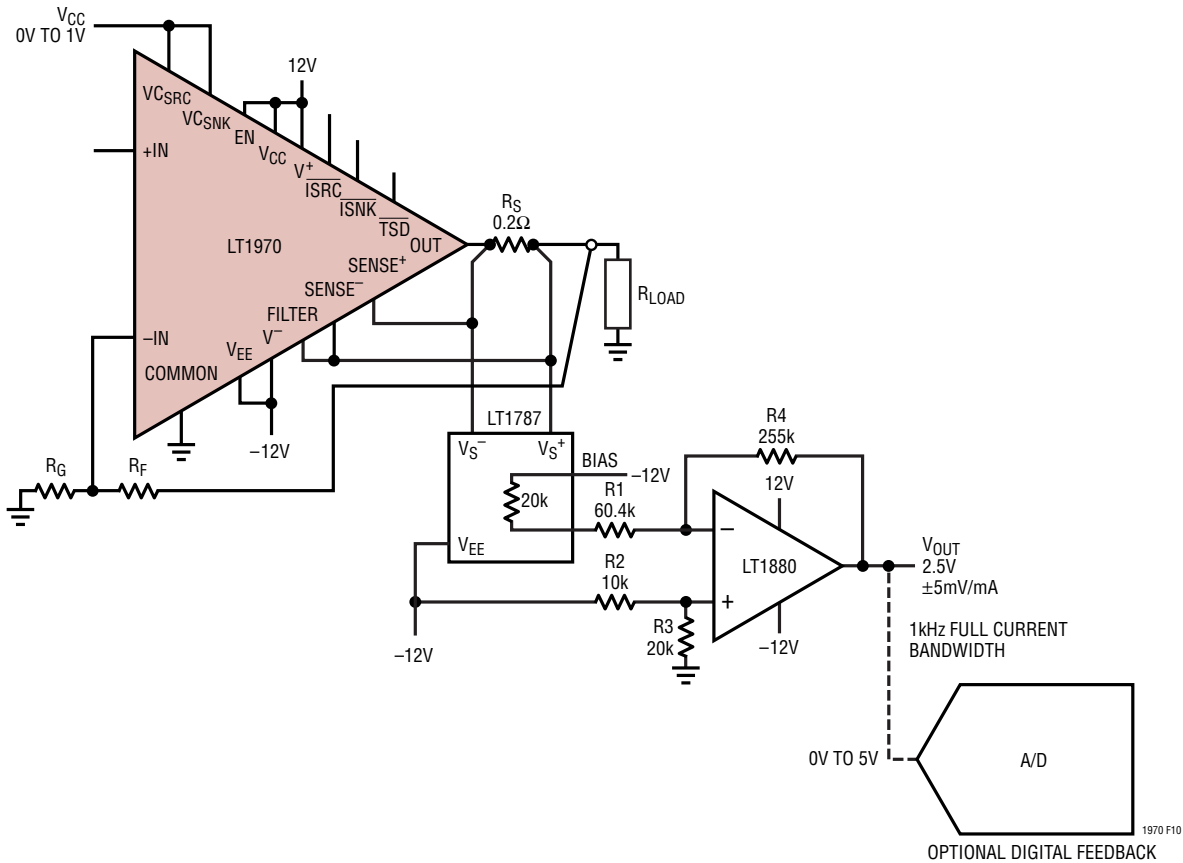


Figure 10. Sensing Output Current

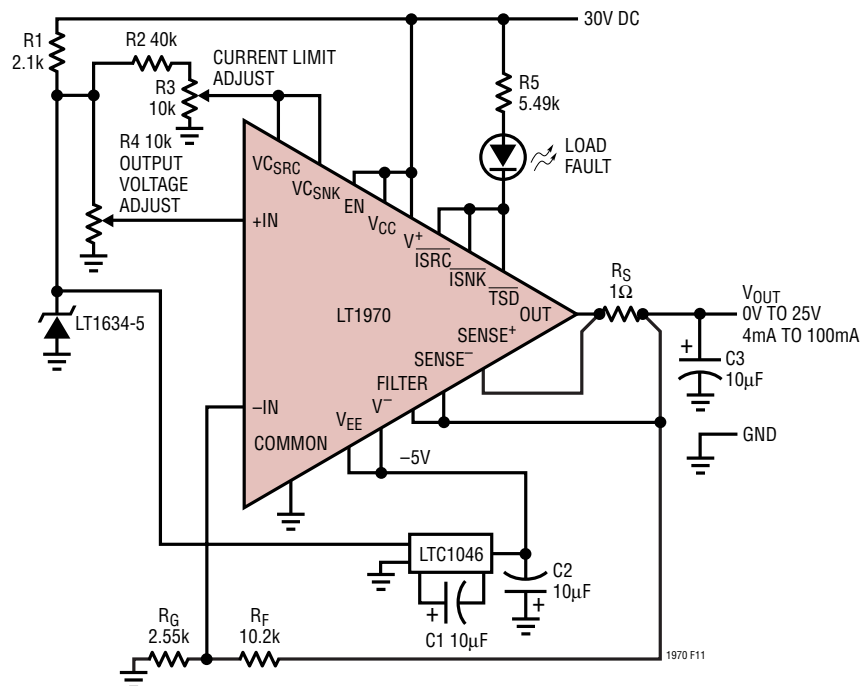


Figure 11. Simple Bench Power Supply

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range all the way to 0V, an LTC1046 charge pump inverter is used to develop a $-5V$ supply. This produces a negative rail for the LT1970 which has to sink only the quiescent current of the amplifier, typically 7mA.

Using a second LT1970, a 0V to $\pm 12V$ dual tracking power supply is shown in Figure 12. The midpoint of two 10k resistors connected between the + and - outputs is held at 0V by the LT1881 dual op amp servo feedback loop. To

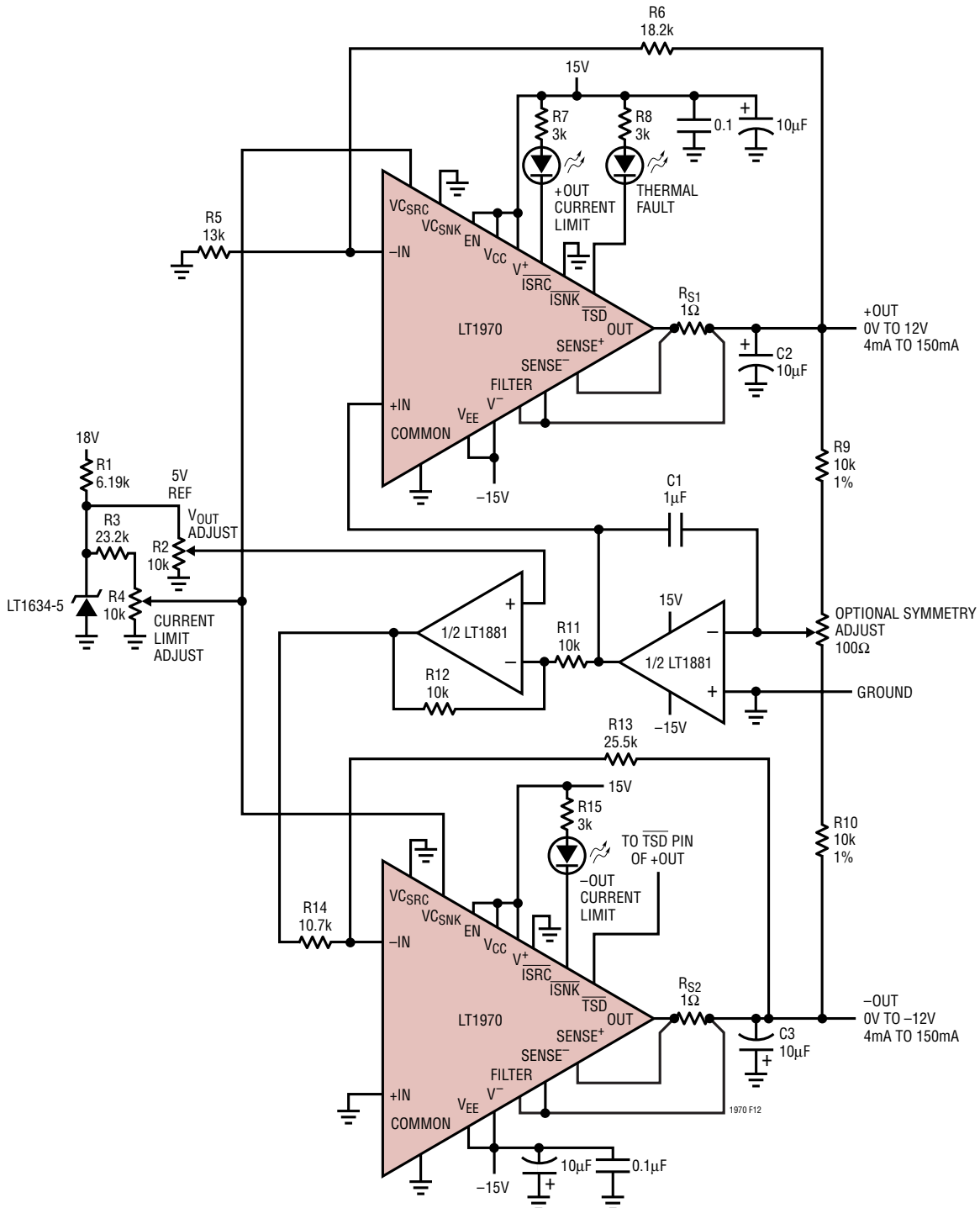


Figure 12. Dual Tracking Bench Power Supply

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maintain 0V, both outputs must be equal and opposite in polarity, thus they track each other. If one output reaches current limit and drops in voltage, the other output follows to maintain a symmetrical + and - voltage across a common load. Again, the output current limit is less than the full capability of the LT1970 due to thermal reasons. Separate current limit indicators are used on each LT1970 because one output only sources current and the other only sinks current. Both devices can share the same thermal shutdown indicator, as the output flags can be OR'ed together.

Another simple linear power amplifier circuit is shown in Figure 13. This uses the LT1970 as a linear driver of a DC motor with speed control. The ability to source and sink the same amount of output current provides for bidirectional rotation of the motor. Speed control is managed by sensing the output of a tachometer built on to the motor. A typical feedback signal of 3V/1000rpm is compared with

the desired speed-set input voltage. Because the LT1970 is unity-gain stable, it can be configured as an integrator to force whatever voltage across the motor as necessary to match the feedback speed signal with the set input signal.

Additionally, the current limit of the amplifier can be adjusted to control the torque and stall current of the motor. For reliability, a feedback scheme similar to that shown in Figure 4 can be used. Assuming that a stalled rotor will generate a current limit condition, the stall current limit can be significantly reduced to prevent excessive power dissipation in the motor windings.

For motor speed control without using a tachometer, the circuit in Figure 14 shows an approach. Using the enable feature of the LT1970, the drive to the motor can be removed periodically. With no drive applied, the spinning motor presents a back EMF voltage proportional to its rotational speed. The LT1782 is a tiny rail-to-rail amplifier

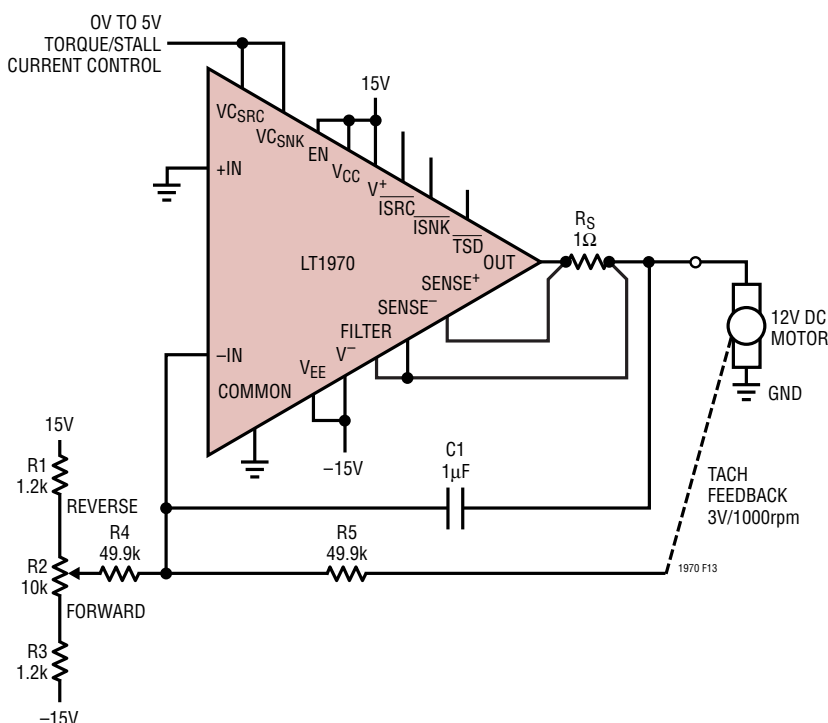


Figure 13. Simple Bidirectional DC Motor Speed Controller

APPLICATIONS INFORMATION

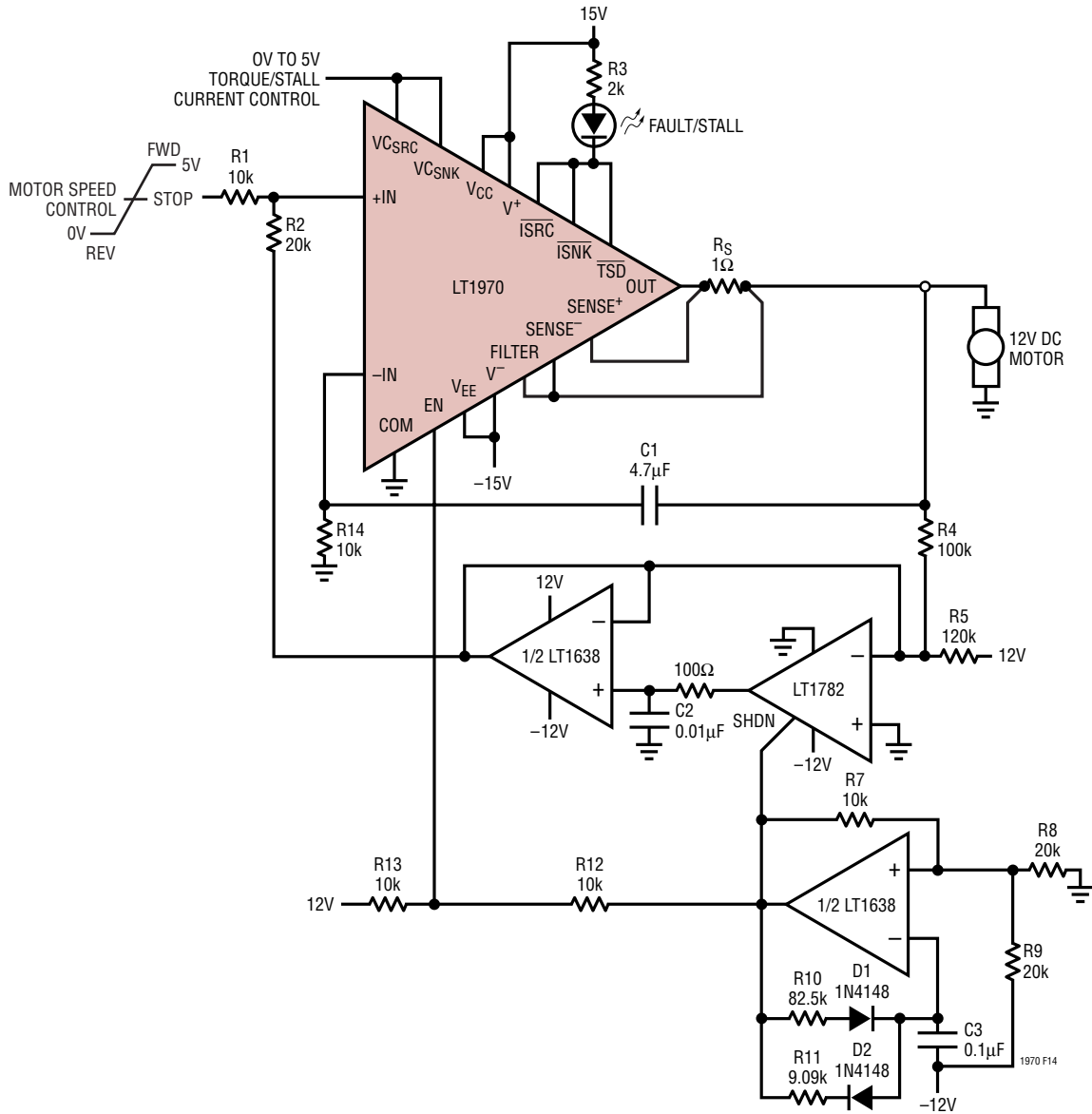


Figure 14. Simple Bidirectional DC Motor Speed Controller Without a Tachometer

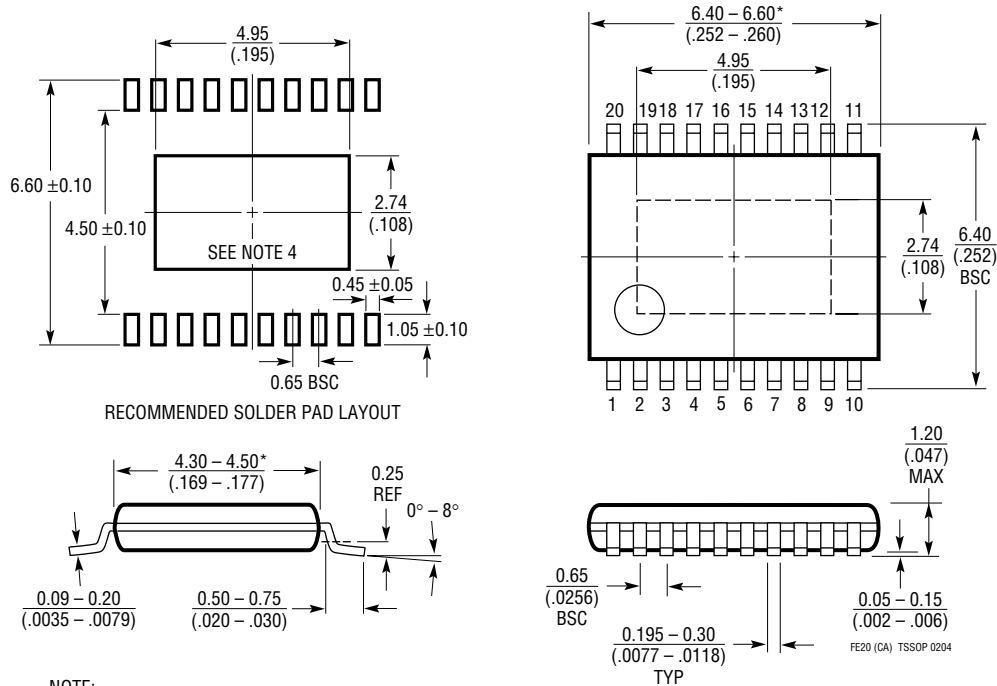
with a shutdown pin. The amplifier is enabled during this interval to sample the back EMF voltage across the motor. This voltage is then buffered by one-half of an LT1638 dual op amp and used to provide the feedback to the LT1970 integrator. When re-enabled the LT1970 will adjust the drive to the motor until the speed feedback voltage,

compared to the speed-set input voltage, settles the output to a fixed value. A 0V to 5V signal for the motor speed input controls both rotational speed and direction.

The other half of the LT1638 is used as a simple pulse oscillator to control the periodic sampling of the motor back EMF.

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
 (Reference LTC DWG # 05-08-1663,
 Exposed Pad Variation CA)



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
 2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{INCHES}}$
 3. DRAWING NOT TO SCALE
 4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
 *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

