Adjustable 3A Single Resistor Low Dropout Regulator

FEATURES

- **Outputs May be Paralleled for Higher Current and Heat Spreading**
- **Output Current: 3A**
- **Single Resistor Programs Output Voltage**
- **50µA Set Pin Current: 1% Initial Accuracy**
- **Output Adjustable to 0V**
- **Low Output Noise: 40µV_{RMS} (10Hz to 100kHz)**
- **Wide Input Voltage Range: 1.2V to 23V (DD-Pak and TO-220 Packages)**
- **Low Dropout Voltage: 310mV**
- <1mV Load Regulation
- <0.001%/V Line Regulation
- Minimum Load Current: 1mA
- Stable with Minimum 10µF Ceramic Capacitor
- Current Limit with Foldback and Overtemperature Protection
- Available in 16-Lead TSSOP, 12-Lead 4mm × 4mm DFN, 5-Lead TO-220 and 5-Lead Surface Mount DD-PAK Packages

APPLICATIONS

- High Current All Surface Mount Supply
- High Efficiency Linear Regulator
- Post Regulator for Switching Supplies
- Low Parts Count Variable Voltage Supply
- Low Output Voltage Power Supplies

DESCRIPTION

The LT®3083 is a 3A low dropout linear regulator that can be paralleled to increase output current or spread heat on surface mounted boards. Architected as a precision current source and voltage follower, this new regulator finds use in many applications requiring high current, adjustability to zero, and no heat sink. The device also brings out the collector of the pass transistor to allow low dropout operation—down to 310mV—when used with multiple supplies.

A key feature of the LT3083 is the capability to supply a wide output voltage range. By using a reference current through a single resistor, the output voltage is programmed to any level between zero and 23V (DD-PAK and TO-220 packages). The LT3083 is stable with 10µF of capacitance on the output, and the IC is stable with small ceramic capacitors that do not require additional ESR as is common with other regulators.

Internal protection circuitry includes current limiting and thermal limiting. The LT3083 is offered in the 16-lead TSSOP (with an exposed pad for better thermal characteristics), 12-lead 4mm × 4mm DFN (also with an exposed pad), 5-lead TO-220, and 5-lead surface mount DD-PAK packages.

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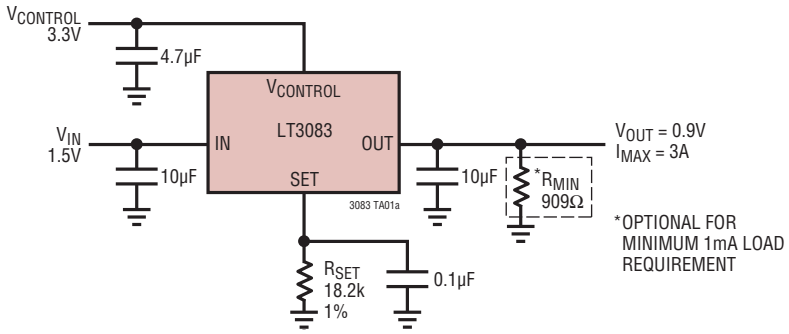
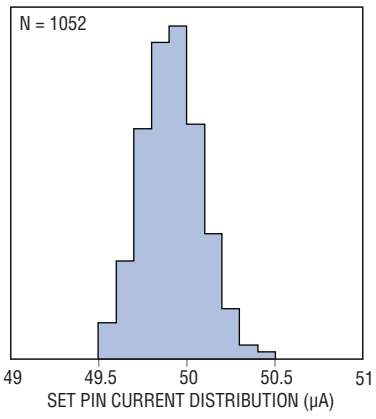
TYPICAL APPLICATION

1.5V to 0.9V at 3A Supply (Using 3.3V $V_{CONTROL}$)



Set Pin Current Distribution



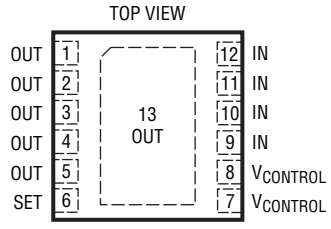
3083 TA01b

ABSOLUTE MAXIMUM RATINGS

(Note 1) All Voltages Relative to V_{OUT}

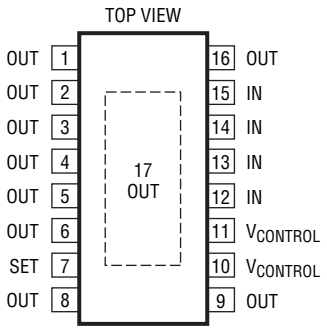
CONTROL Pin Voltage ..... ±28V
IN Pin Voltage (T5, Q Packages) ..... 18V, –0.3V
No Overload or Short-Circuit ..... 23V, –0.3V
IN Pin Voltage (DF, FE Packages) ..... 8V, –0.3V
No Overload or Short-Circuit ..... 14V, –0.3V
SET Pin Current (Note 7) ..... ±25mA
SET Pin Voltage (Relative to OUT) ..... ±10V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Notes 2, 10)
E-, I-grades ..... –40°C to 125°C
MP-grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
T, Q, FE Packages Only ..... 300°C

PIN CONFIGURATION



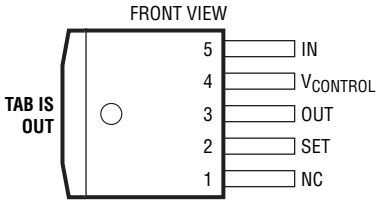
DF PACKAGE
12-LEAD (4mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 13) IS OUT, MUST BE SOLDERED TO PCB



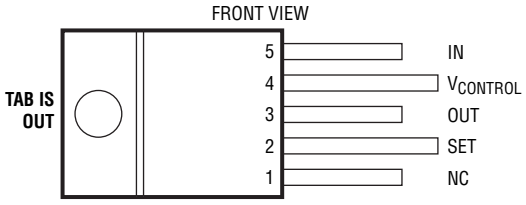
FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 25°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS OUT, MUST BE SOLDERED TO PCB



Q PACKAGE
5-LEAD PLASTIC DD-PAK

T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JC} = 3°C/W



T PACKAGE
5-LEAD PLASTIC TO-220

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 3°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3083EDF#PBF	LT3083EDF#TRPBF	3083	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3083EFE#PBF	LT3083EFE#TRPBF	3083FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3083EQ#PBF	LT3083EQ#TRPBF	LT3083Q	5-Lead Plastic DD-PAK	–40°C to 125°C
LT3083ET#PBF	LT3083ET#TRPBF	LT3083T	5-Lead Plastic TO-220	–40°C to 125°C
LT3083IDF#PBF	LT3083IDF#TRPBF	3083	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3083IFE#PBF	LT3083IFE#TRPBF	3083FE	16-Lead Plastic TSSOP	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3083IQ#PBF	LT3083IQ#TRPBF	LT3083Q	5-Lead Plastic DD-PAK	–40°C to 125°C
LT3083IT#PBF	LT3083IT#TRPBF	LT3083T	5-Lead Plastic TO-220	–40°C to 125°C
LT3083MPDF#PBF	LT3083MPDF#TRPBF	3083	12-Lead (4mm × 4mm) Plastic DFN	–55°C to 125°C
LT3083MPFE#PBF	LT3083MPFE#TRPBF	3083FE	16-Lead Plastic TSSOP	–55°C to 125°C
LT3083MPQ#PBF	LT3083MPQ#TRPBF	LT3083Q	5-Lead Plastic DD-PAK	–55°C to 125°C
LT3083MPT#PBF	LT3083MPT#TRPBF	LT3083T	5-Lead Plastic TO-220	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3083EDF	LT3083EDF#TR	3083	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3083EFE	LT3083EFE#TR	3083FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3083EQ	LT3083EQ#TR	LT3083Q	5-Lead Plastic DD-PAK	–40°C to 125°C
LT3083ET	LT3083ET#TR	LT3083T	5-Lead Plastic TO-220	–40°C to 125°C
LT3083IDF	LT3083IDF#TR	3083	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3083IFE	LT3083IFE#TR	3083FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3083IQ	LT3083IQ#TR	LT3083Q	5-Lead Plastic DD-PAK	–40°C to 125°C
LT3083IT	LT3083IT#TR	LT3083T	5-Lead Plastic TO-220	–40°C to 125°C
LT3083MPDF	LT3083MPDF#TR	3083	12-Lead (4mm × 4mm) Plastic DFN	–55°C to 125°C
LT3083MPFE	LT3083MPFE#TR	3083FE	16-Lead Plastic TSSOP	–55°C to 125°C
LT3083MPQ	LT3083MPQ#TR	LT3083Q	5-Lead Plastic DD-PAK	–55°C to 125°C
LT3083MPT	LT3083MPT#TR	LT3083T	5-Lead Plastic TO-220	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2).

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
SET Pin Current	I_{SET}	V_{IN} = 1V, $V_{CONTROL}$ = 2V, I_{LOAD} = 1mA, T_J = 25°C		49.5	50	50.5	µA
		V_{IN} ≥ 1V, $V_{CONTROL}$ ≥ 2V, 5mA ≤ I_{LOAD} ≤ 3A (Note 9)	●	49	50	51	µA
Output Offset Voltage (V_{OUT} – V_{SET}) V_{IN} = 1V, $V_{CONTROL}$ = 2V, I_{LOAD} = 1mA	V_{OS}	DF, FE Packages		–3	0	3	mV
			●	–4	0	4	mV
		T, Q Packages		–4	0	4	mV
			●	–6	0	6	mV
Load Regulation (DF, FE Packages)	ΔI_{SET}	ΔI_{LOAD} = 1mA to 3A			–10		nA
	ΔV_{OS}	ΔI_{LOAD} = 5mA to 3A (Note 8)	●		–0.4	–1	mV
Load Regulation (T, Q Packages)	ΔI_{SET}	ΔI_{LOAD} = 1mA to 3A			–10		nA
	ΔV_{OS}	ΔI_{LOAD} = 5mA to 3A (Note 8)	●		–0.7	–4	mV
Line Regulation (DF, FE Packages)	ΔI_{SET}	ΔV_{IN} = 1V to 14V, $\Delta V_{CONTROL}$ = 2V to 25V, I_{LOAD} = 1mA			0.1		nA/V
	ΔV_{OS}	ΔV_{IN} = 1V to 14V, $\Delta V_{CONTROL}$ = 2V to 25V, I_{LOAD} = 1mA			0.002	0.01	mV/V
Line Regulation (T, Q Packages)	ΔI_{SET}	ΔV_{IN} = 1V to 23V, $\Delta V_{CONTROL}$ = 2V to 25V, I_{LOAD} = 1mA			0.1		nA/V
	ΔV_{OS}	ΔV_{IN} = 1V to 23V, $\Delta V_{CONTROL}$ = 2V to 25V, I_{LOAD} = 1mA			0.002	0.01	mV/V
Minimum Load Current (Notes 3, 9)		V_{IN} = 1V, $V_{CONTROL}$ = 2V	●		350	500	µA
		V_{IN} = 14V (DF/FE) or 23V (T/Q), $V_{CONTROL}$ = 25V	●			1	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CONTROL}$ Dropout Voltage (Note 4)	I_{LOAD} = 100mA			1.2		V
	I_{LOAD} = 1A	●		1.22	1.55	V
	I_{LOAD} = 3A	●		1.25	1.6	V
V_{IN} Dropout Voltage (Note 4)	I_{LOAD} = 100mA	●		10	25	mV
	I_{LOAD} = 1A, Q, T Packages	●		120	190	mV
	I_{LOAD} = 1A, DF, FE Packages	●		90	160	mV
	I_{LOAD} = 3A, Q, T Packages	●		310	510	mV
	I_{LOAD} = 3A, DF, FE Packages	●		240	420	mV
$V_{CONTROL}$ Pin Current (Note 5)	I_{LOAD} = 100mA	●		5.5	10	mA
	I_{LOAD} = 1A	●		18	35	mA
	I_{LOAD} = 3A	●		40	80	mA
Current Limit	V_{IN} = 5V, $V_{CONTROL}$ = 5V, V_{SET} = 0V, V_{OUT} = –0.1V	●	3	3.7		A
Error Amplifier RMS Output Noise (Note 6)	I_{LOAD} = 500mA, 10Hz ≤ f ≤ 100kHz, C_{OUT} = 10µF, C_{SET} = 0.1µF			40		μV_{RMS}
Reference Current RMS Output Noise (Note 6)	10Hz ≤ f ≤ 100kHz			1		nA_{RMS}
Ripple Rejection V_{RIPPLE} = 0.5V_{P-P}, I_L = 0.1A, C_{SET} = 0.1µF, C_{OUT} = 10µF	f = 120Hz f = 10kHz f = 1MHz			85 75 20		dB dB dB
Thermal Regulation, I_{SET}	10ms Pulse			0.003		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, all voltages are with respect to V_{OUT}. The LT3083 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3083E is 100% tested at T_A = 25°C. Performance of the LT3083E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3083I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3083MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

Note 3: Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

Note 4: For the LT3083, dropout is caused by either minimum control voltage ($V_{CONTROL}$) or minimum input voltage (V_{IN}). Both parameters are specified with respect to the output voltage. The specifications represent the minimum input-to-output differential voltage required to maintain regulation.

Note 5: The $V_{CONTROL}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:60 ratio. The minimum value is equal to the quiescent current of the device.

Note 6: Output noise is lowered by adding a small capacitor across the voltage setting resistor. Adding this capacitor bypasses the voltage setting resistor shot noise and reference current noise; output noise is then equal to error amplifier noise (see the Applications Information section).

Note 7: The SET pin is clamped to the output with diodes through 1k resistors. These resistors and diodes will only carry current under transient overloads.

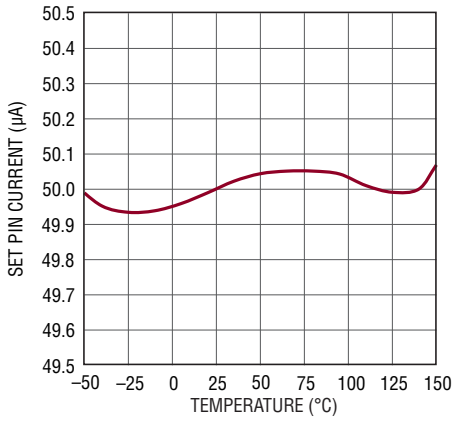
Note 8: Load regulation is Kelvin sensed at the package.

Note 9: Current limit includes foldback protection circuitry. Current limit decreases at higher input-to-output differential voltages.

Note 10: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Overtemperature protection (thermal limit) is typically active at junction temperatures of 165°C. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

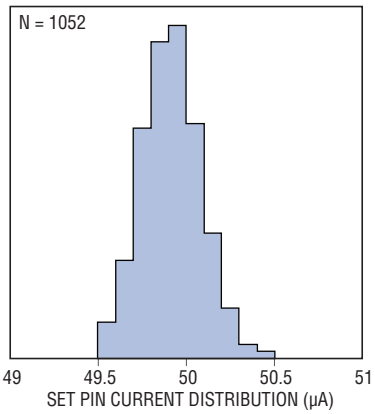
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

SET Pin Current



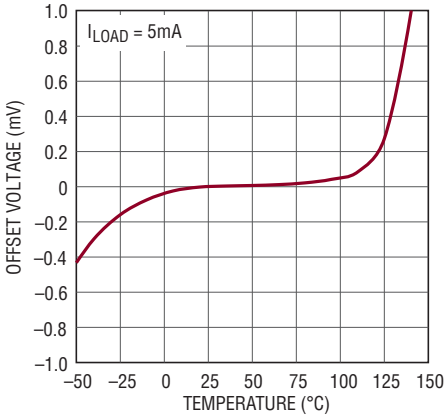
3083 G01

Set Pin Current Distribution



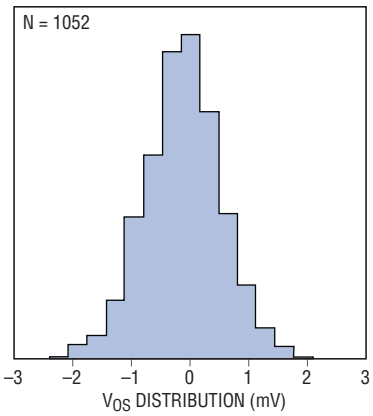
3083 G02

Offset Voltage (V_{OUT} – V_{SET})



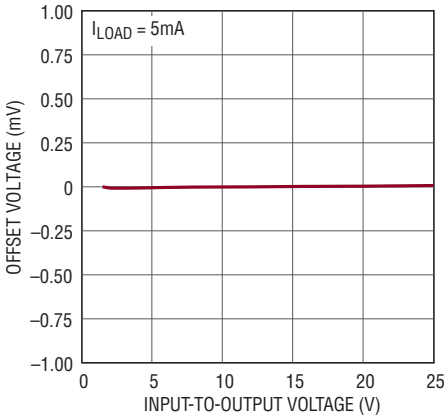
3083 G03

Offset Voltage Distribution



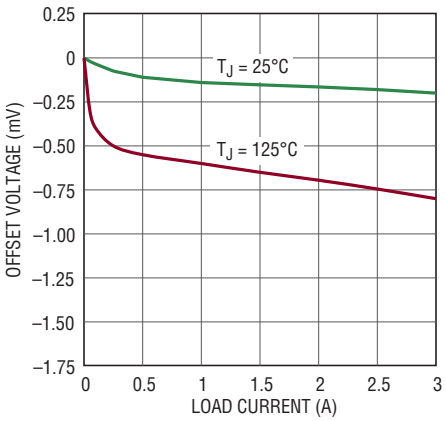
3083 G04

Offset Voltage (V_{OUT} – V_{SET})



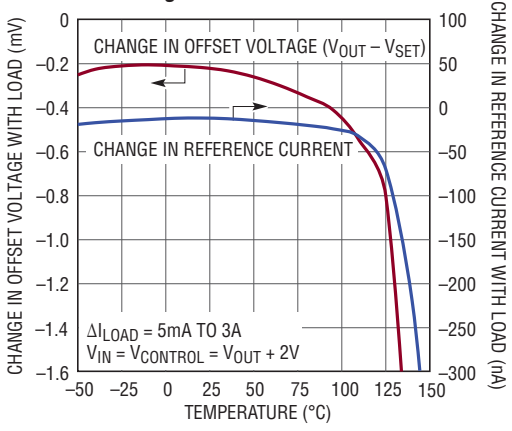
3083 G05

Offset Voltage (V_{OUT} – V_{SET})



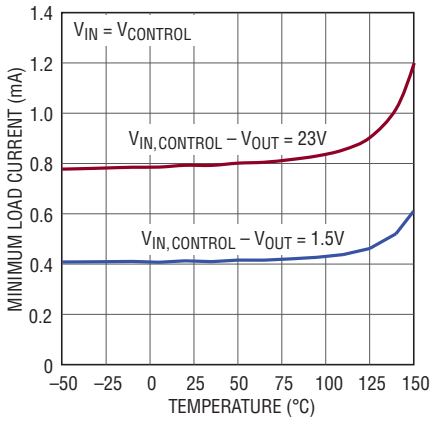
3083 G06

Load Regulation



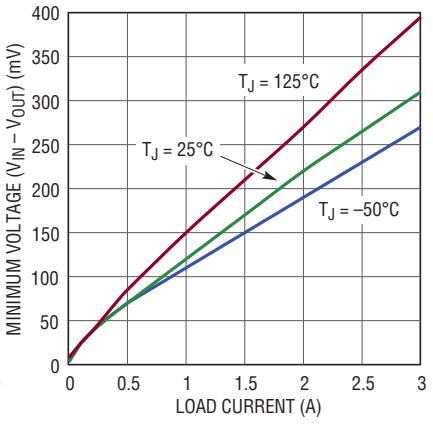
3083 G07

Minimum Load Current



3083 G08

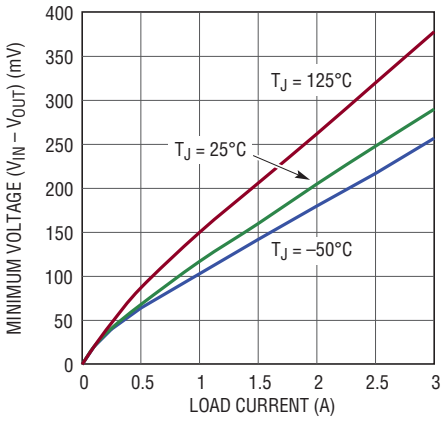
Dropout Voltage, T/Q Packages (Minimum IN Voltage)



3083 G09

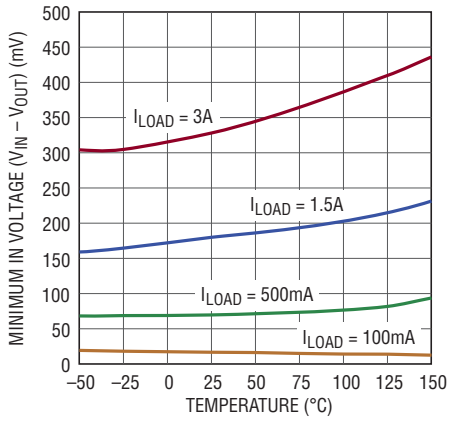
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Dropout Voltage, FE/DF Packages



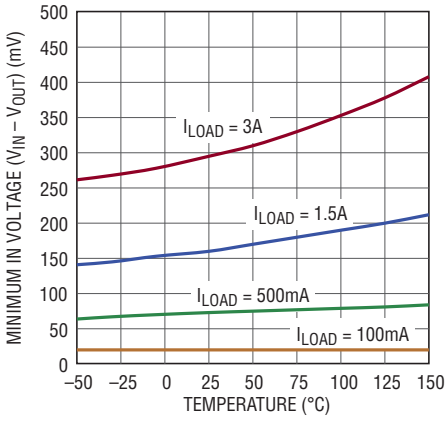
3083 G10

Dropout Voltage, T/Q Packages (Minimum IN Voltage)



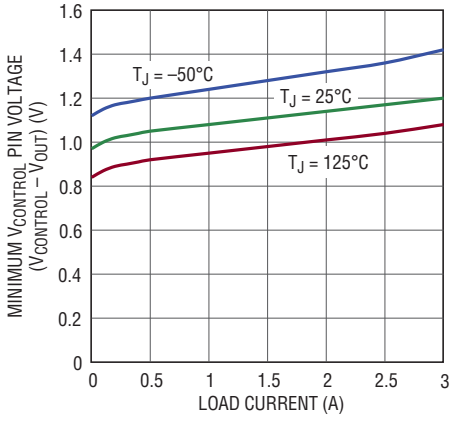
3083 G11

Dropout Voltage, FE/DF Packages (Minimum IN Voltage)



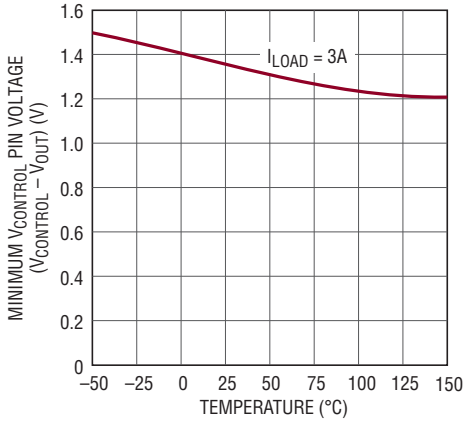
3083 G12

Dropout Voltage (Minimum $V_{CONTROL}$ Pin Voltage)



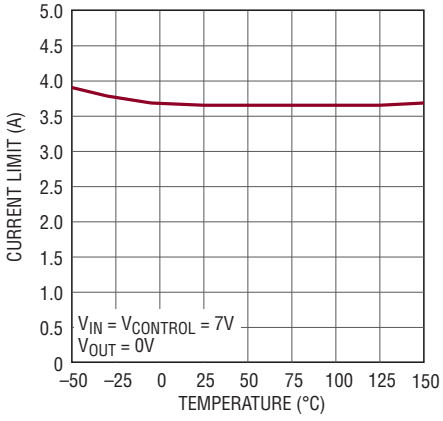
3083 G13

Dropout Voltage (Minimum $V_{CONTROL}$ Pin Voltage)



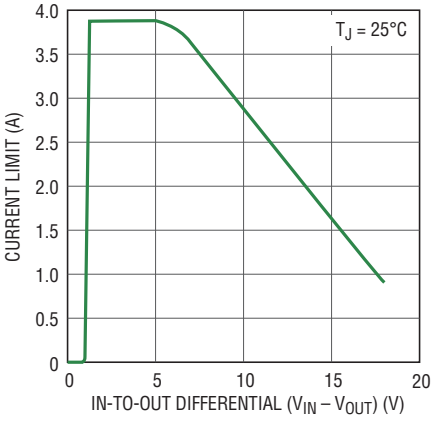
3083 G14

Current Limit



3083 G15

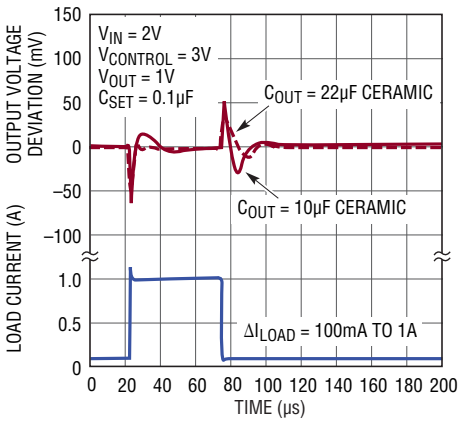
Current Limit



3083 G16

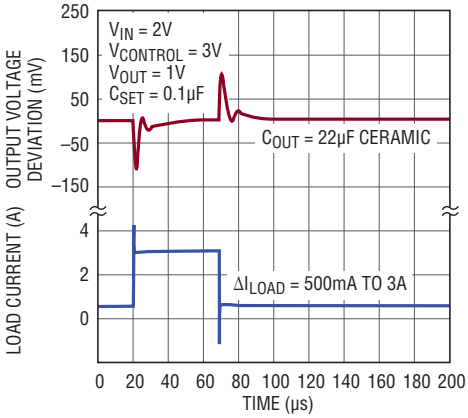
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Load Transient Response



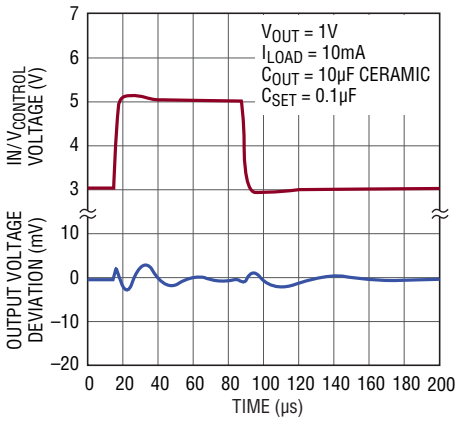
3083 G17

Load Transient Response



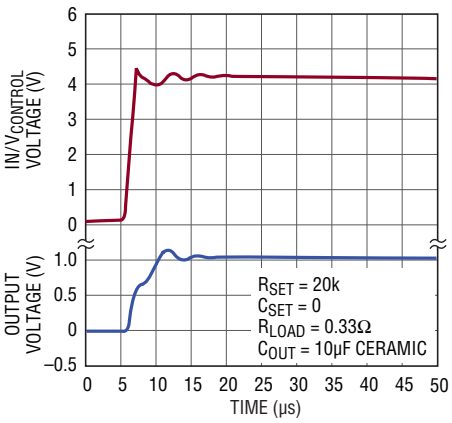
3083 G18

Line Transient Response



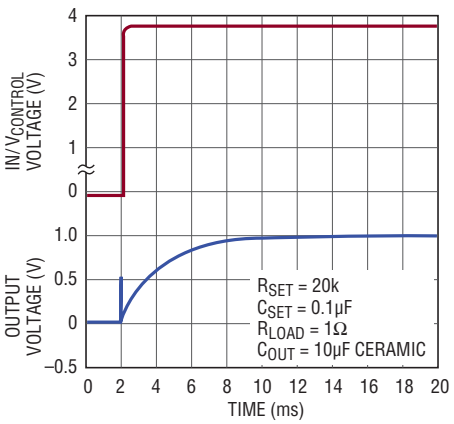
3083 G19

Turn-On Response



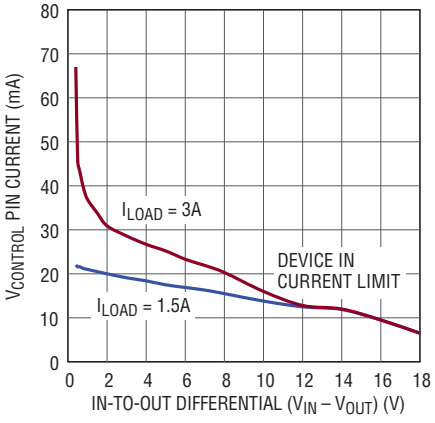
3083 G20

Turn-On Response



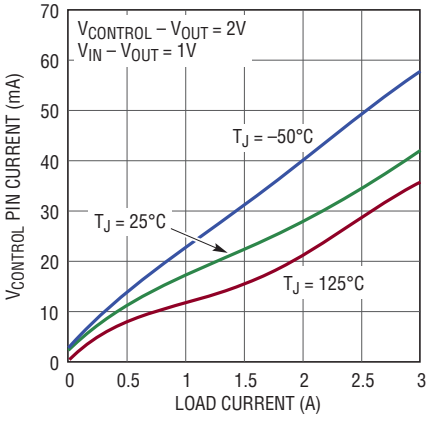
3083 G21

$V_{CONTROL}$ Pin Current



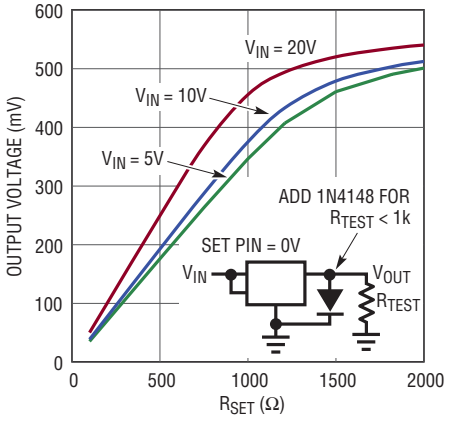
3083 G22

$V_{CONTROL}$ Pin Current



3083 G23

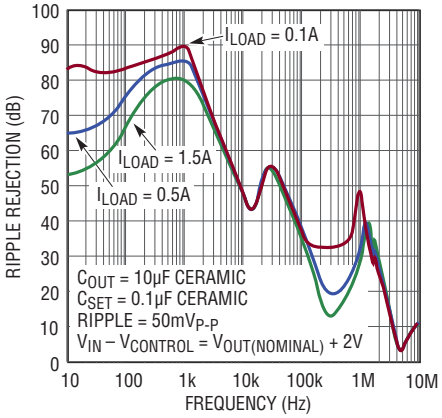
Residual Output Voltage with Less Than Minimum Load



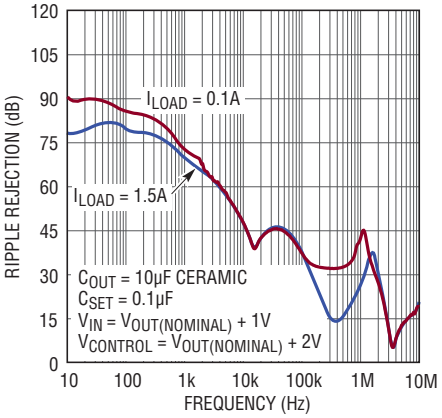
3083 G24

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

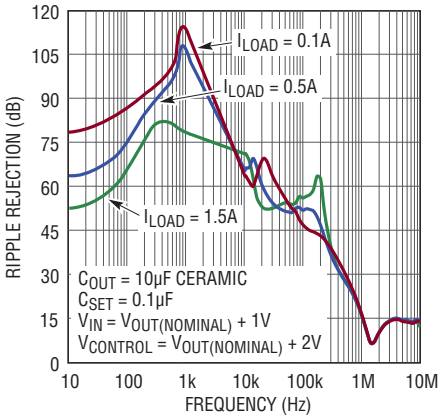
Ripple Rejection, Single Supply



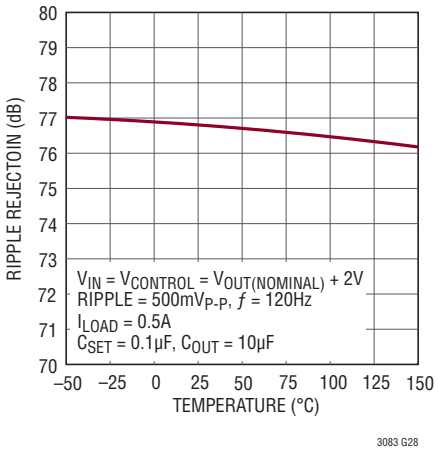
Ripple Rejection, Dual Supply, $V_{CONTROL}$ Pin



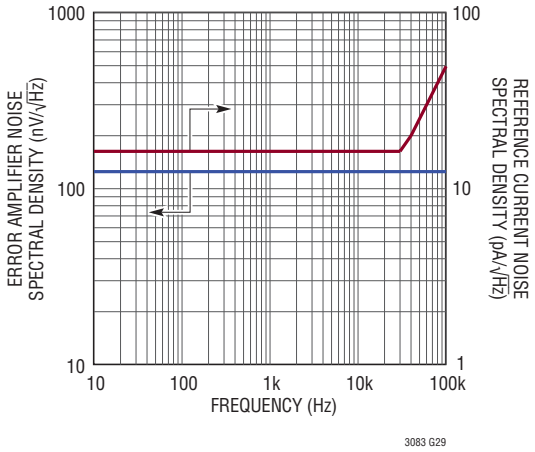
Ripple Rejection, Dual Supply, IN Pin



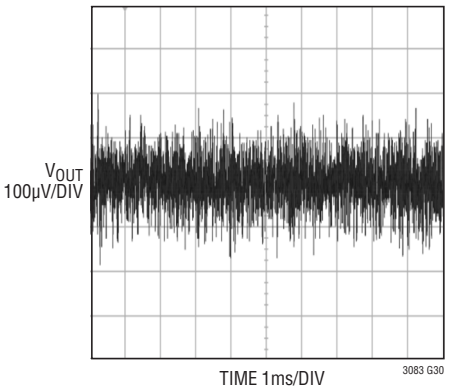
Ripple Rejection (120Hz)



Noise Spectral Density

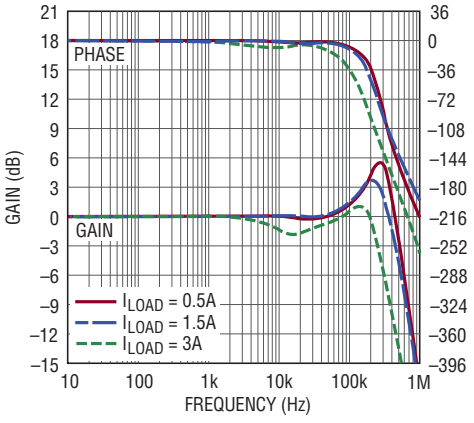


Output Voltage Noise



V_{OUT} = 1V, R_{SET} = 20k
C_{SET} = 0.1µF, C_{OUT} = 10µF
I_{LOAD} = 3A

Error Amplifier Gain and Phase



PIN FUNCTIONS (DF/FE/Q/T Packages)

OUT (Pins 1-5,13/Pins 1-6,8,9,16,17/Pin 3, Tab/Pin 3, Tab): Output. The exposed pad of the DF package (Pin 13) and the FE package (Pin 17) and the Tab of the DD-PAK and TO-220 packages is an electrical connection to OUT. Connect the exposed pad of the DF and FE packages and the Tab of the DD-PAK package directly to OUT on the PCB and the respective OUT pins for each package. There must be a minimum load current of 1mA or the output may not regulate.

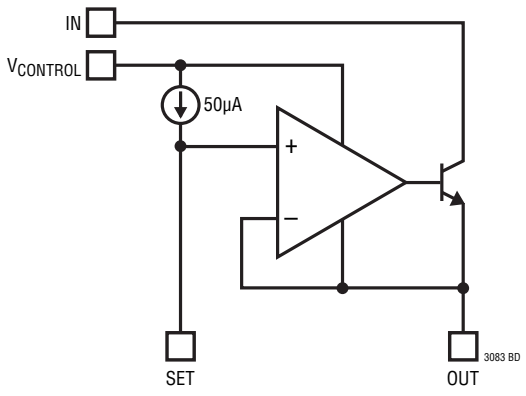
SET (Pin 6/Pin 7/Pin 2/Pin 2): Set Point. This pin is the non-inverting input to the error amplifier and the regulation set point. A fixed current of 50µA flows out of this pin through a single external resistor, which programs the output voltage of the device. Output voltage range is zero to the $V_{IN(MAX)} – V_{DROPOUT}$. Transient performance can be improved by adding a small capacitor from the SET pin to ground.

$V_{CONTROL}$ (Pins 7,8/Pins 10,11/Pin 4/Pin 4): Bias Supply. This is the supply pin for the control circuitry of the device. Minimum input capacitance is 2.2µF (see Input Capacitance and Stability in the Applications Information section). The current flow into this pin is about 1.7% of the output current. For the device to regulate, this voltage must be more than 1.2V to 1.4V greater than the output voltage (see dropout specifications in the Electrical Characteristics section).

IN (Pins 9-12/Pins 12-15/Pin 5/Pin 5): Power Input. This is the collector to the power device of the LT3083. The output load current is supplied through this pin. Minimum IN capacitance is 10µF (see Input Capacitance and Stability in Applications Information section). For the device to regulate, the voltage at this pin must be more than 0.1V to 0.5V greater than the output voltage (see dropout specifications in the Electrical Characteristics section).

NC (NA/NA/Pin 1/Pin 1): No Connection. No Connect pins have no connection to internal circuitry and may be tied to V_{IN}, $V_{CONTROL}$, V_{OUT}, GND, or floated.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3083 regulator is easy to use and has all the protection features expected in high performance regulators. Included are short-circuit protection and safe operating area protection, as well as thermal shutdown with hysteresis.

The LT3083 fits well in applications needing multiple rails. This new architecture adjusts down to zero with a single resistor, handling modern low voltage digital IC's as well as allowing easy parallel operation and thermal management without heat sinks. Adjusting to zero output allows shutting off the powered circuitry. When the input is pre-regulated, such as with a 5V or 3.3V input supply, external resistors can help spread the heat.

A precision "0" TC 50µA reference current source connects to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output to the voltage on the noninverting input. A single resistor from the noninverting input to ground sets the output voltage. If this resistor is set to 0Ω, zero output voltage results. Therefore, any output voltage can be obtained between zero and the maximum defined by the input power supply.

The benefit of using a true internal current source as the reference, as opposed to a bootstrapped reference in older regulators, is not so obvious in this architecture. A true reference current source allows the regulator to have gain and frequency response independent of the impedance on the positive input. On older adjustable regulators, such as the LT1086, loop gain changes with output voltage and bandwidth changes if the adjustment pin is bypassed to ground. For the LT3083, the loop gain is unchanged with output voltage changes or bypassing. Output regulation is not a fixed percentage of output voltage, but is a fixed fraction of millivolts. Use of a true current source allows all of the gain in the buffer amplifier to provide regulation, and none of that gain is needed to amplify up the reference to a higher output voltage.

The LT3083 has the collector of the output transistor connected to a separate pin from the control input. Since the dropout on the collector (IN pin) is typically only 310mV, two supplies can be used to power the LT3083 to reduce dissipation: a higher voltage supply for the control circuitry and a lower voltage supply for the collector. This increases efficiency and reduces dissipation. To further spread the heat, a resistor inserted in series with the collector moves some of the heat out of the IC to spread it on the PC board (see the section *Reducing Power Dissipation*).

The LT3083 can be operated in two modes. Three terminal mode has the $V_{CONTROL}$ pin connected to the IN pin and gives a limitation of 1.25V dropout. Alternatively, the $V_{CONTROL}$ pin is separately tied to a higher voltage and the IN pin to a lower voltage giving 310mV dropout on the IN pin, minimizing total power dissipation. This allows for a 3A supply regulating from $2.5V_{IN}$ to $1.8V_{OUT}$ or $1.8V_{IN}$ to $1.2V_{OUT}$ with low power dissipation.

Programming Output Voltage

The LT3083 sources a 50µA reference current that flows out of the SET pin. Connecting a resistor from SET to ground generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage equals 50µA multiplied by the value of the SET pin resistor. Any voltage can be generated and there is no minimum output voltage for the regulator.

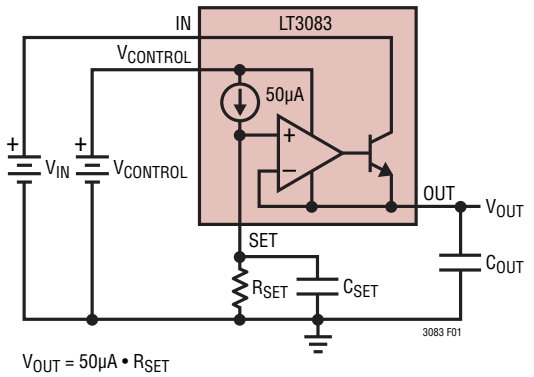


Figure 1. Basic Adjustable Regulator

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Table 1 lists many common output voltages and the closest standard 1% resistor values used to generate that output voltage.

Regulation of the output voltage requires a minimum load current of 1mA. For a true zero voltage output operation, return this 1mA load current to a negative supply voltage.

Table 1. 1% Resistors for Common Output Voltages

V_{OUT} (V)	R_{SET} (k)
1	20
1.2	24.3
1.5	30.1
1.8	35.7
2.5	49.9
3.3	66.5
5	100

With the lower level current used to generate the reference voltage, leakage paths to or from the SET pin can create errors in the reference and output voltages. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Minimize board leakage by encircling the SET pin and circuitry with a guard ring operated at a potential close to itself. Tie the guard ring to the OUT pin. Guard rings on both sides of the circuit board are required. Bulk leakage reduction depends on the guard ring width. 50nA of leakage into or out of the SET pin and its associated circuitry creates a 0.1% reference voltage error. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference drift, especially over the possible operating temperature range. Figure 2 depicts an example of a guard ring layout.

If guard ring techniques are used, this bootstraps any stray capacitance at the SET pin. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This will be most noticeable when operating with minimum output capacitors at full load current. The easiest way to remedy this is to bypass the SET pin with a small amount of capacitance from SET to ground, 10pF to 20pF is sufficient.

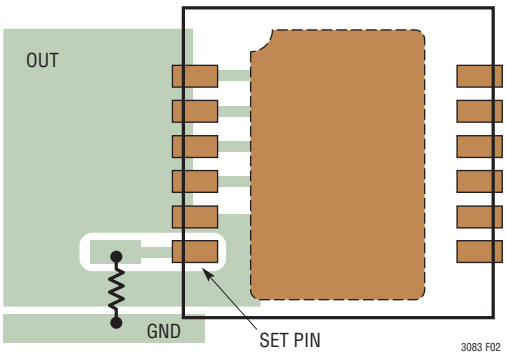

Figure 2. Guard Ring Layout Example for DF Package

Stability and Input Capacitance

Typical minimum input capacitance is 10µF for IN and 2.2µF for $V_{CONTROL}$. These amounts of capacitance work well using low ESR ceramic capacitors when placed close to the LT3083 and the circuit is located in close proximity to the power source. Higher values of input capacitance may be necessary to maintain stability depending on the application.

Oscillating regulator circuits are often viewed as a problem of phase margin and inadequate stability with the output capacitor used. More and more frequently, the problem is not the regulator operating without sufficient output capacitance, but instead with too little input capacitance. The entire circuit must be analyzed and debugged as a whole; conditions relating to the input of the regulator cannot be ignored.

The LT3083 input presents a high impedance to its power source: the output voltage and load current are independent of input voltage variations. To maintain stability of the regulator circuit as a whole, the LT3083 must be powered from a low impedance supply. When using short supply lines or powering directly from a large switching supply, there is no issue—hundreds or thousands of microfarads of capacitance are available through a low impedance.

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When longer supply lines, filters, current sense resistors, or other impedances exist between the supply and the input to the LT3083, input bypassing should be reviewed if stability concerns are seen. Just as output capacitance supplies the instantaneous changes in load current for output transients until the regulator is able to respond, input capacitance supplies local power to the regulator until the main supply responds. When impedance separates the LT3083 from its main supply, the local input can droop so that the output follows. The entire circuit may break into oscillations, usually characterized by larger amplitude oscillations on the input and coupling to the output.

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3083 circuit's IN and GND pins with long input wires combined with low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The input wire inductance found in many battery powered applications, combined with the low ESR ceramic input capacitor, forms a high-Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3083 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has about 465nH of self-inductance.

One of two ways reduces a wire's self-inductance. One method divides the current flowing towards the LT3083 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel, but placing them in close proximity gives the wires mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward- and return- current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If wiring modifications are not permissible for the applications, including series resistance between the power supply and the input of the LT3083 also stabilizes the application. As little as 0.1Ω to 0.5Ω, often less, is effective in damping the LC resonance. If the added impedance between the power supply and the input is unacceptable, adding ESR to the input capacitor also provides the necessary damping of the LC resonance. However, the required ESR is generally higher than the series impedance required.

Stability and Output Capacitance

The LT3083 requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 10µF with an ESR of 0.5Ω or less is recommended to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3083, increase the effective output capacitor value. For improvement in transient performance, place a capacitor across the voltage setting resistor. Capacitors up to 1µF can be used. This bypass capacitor reduces system noise as well, but start-up time is proportional to the time constant of the voltage setting resistor (R_{SET} in Figure 1) and SET pin bypass capacitor.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an

APPLICATIONS INFORMATION

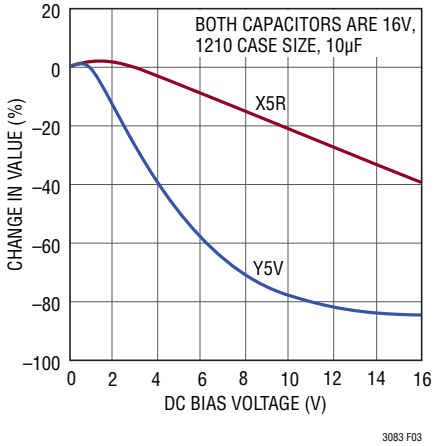

Figure 3. Ceramic Capacitor DC Bias Characteristics

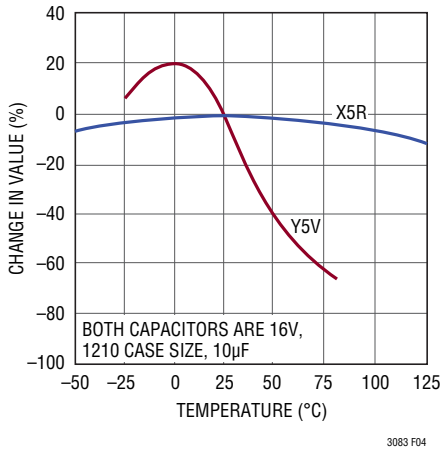

Figure 4. Ceramic Capacitor Temperature Characteristics

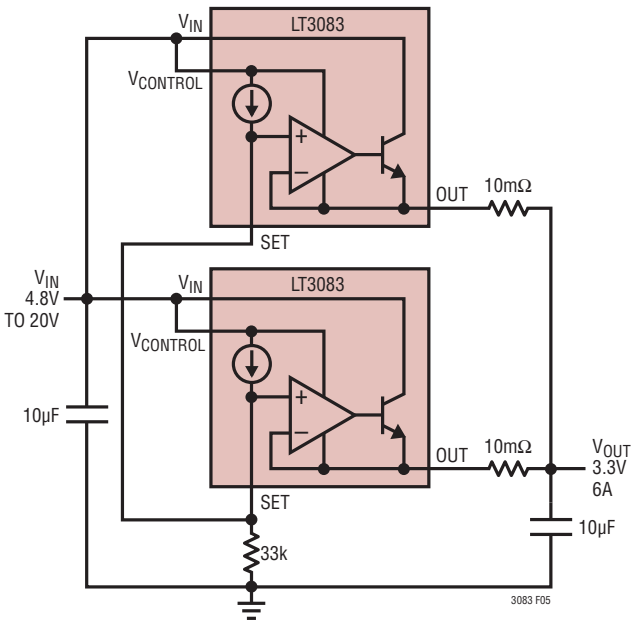

Figure 5. Parallel Devices

effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Paralleling Devices

Higher output current is obtained by paralleling multiple LT3083s together. Tie the individual SET pins together and tie the individual IN pins together. Connect the outputs in common using small pieces of PC trace as ballast resistors to promote equal current sharing. PC trace resistance in mΩ/inch is shown in Table 2. Ballasting requires only a tiny area on the PCB.

Table 2. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in

The worst-case room temperature offset, only ±4mV (DD-PAK, T Packages) between the SET pin and the OUT pin, allows the use of very small ballast resistors.

As shown in Figure 5, each LT3083 has a small 10mΩ ballast resistor, which at full output current gives better than 80% equalized sharing of the current. The external

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resistance of 10mΩ (5mΩ for the two devices in parallel) only adds about 30mV of output regulation drop at an output of 6A. With an output voltage of 3.3V, this only adds 1% to the regulation. Of course, paralleling more than two LT3083s yields even higher output current. Spreading the devices on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output difference is high.

Quieting the Noise

The LT3083 offers numerous noise performance advantages. Every linear regulator has its sources of noise. In general, a linear regulator's critical noise source is the reference. In addition, consider the error amplifier's noise contribution along with the resistor divider's noise gain.

Many traditional low noise regulators bond out the voltage reference to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction. The LT3083 does not use a traditional voltage reference like other linear regulators. Instead, it uses a 50µA reference current. The 50µA current source generates noise current levels of 3.16pA/$\sqrt{Hz}$ (1nA$_{RMS}$) over the 10Hz to 100kHz bandwidth). The equivalent voltage noise equals the RMS noise current multiplied by the resistor value.

The SET pin resistor generates spot noise equal to $\sqrt{4kTR}$ (k = Boltzmann's constant, $1.38 \cdot 10^{-23}$J/°K, and T is absolute temperature) which is RMS summed with the voltage noise. If the application requires lower noise performance, bypass the voltage setting resistor with a capacitor to GND. Note that this noise-reduction capacitor increases start-up time as a factor of the RC time constant.

The LT3083 uses a unity-gain follower from the SET pin to the OUT pin. Therefore, multiple possibilities exist (besides a SET pin resistor) to set output voltage. For example, using a high accuracy voltage reference from SET to GND removes the errors in output voltage due to reference current tolerance and resistor tolerance. Active driving of the SET pin is acceptable.

The typical noise scenario for a linear regulator is that the output voltage setting resistor divider gains up the noise reference, especially if V_{OUT} is much greater than V_{REF}.

The LT3083's noise advantage is that the unity gain follower presents no noise gain whatsoever from the SET pin to the output. Thus, noise figures do not increase accordingly. Error amplifier noise is typically 126.5nV/$\sqrt{Hz}$ (40µV$_{RMS}$) over the 10Hz to 100kHz bandwidth). The error amplifier's noise is RMS summed with the other noise terms to give a final noise figure for the regulator.

Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for both the reference current and error amplifier over the 10Hz to 100kHz bandwidth.

Load Regulation

The LT3083 is a floating device. No ground pin exists on the packages. Thus, the IC delivers all quiescent current and drive current to the load. Therefore, it is not possible to provide true remote load sensing. The connection resistance between the regulator and the load determines load regulation performance. The data sheet's load regulation specification is Kelvin sensed at the package's pins. Negative-side sensing is a true Kelvin connection by returning the bottom of the voltage setting resistor to the negative side of the load (see Figure 6).

Connected as shown, system load regulation is the sum of the LT3083's load regulation and the parasitic line resistance multiplied by the output current. To minimize load regulation, keep the positive connection between the regulator and load as short as possible. If possible, use large diameter wire or wide PC board traces.

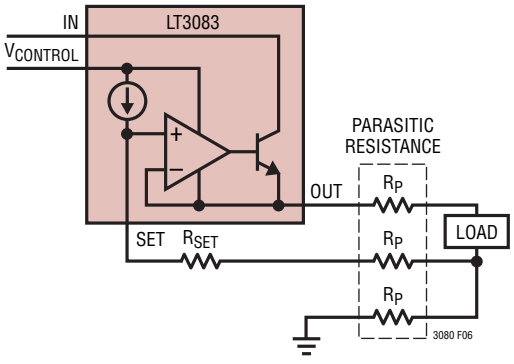

Figure 6. Connections for Best Load Regulation

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Thermal Considerations

The LT3083's internal power and thermal limiting circuitry protects itself under overload conditions. For continuous normal load conditions, do not exceed the 125°C maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

Surface mount packages provide the necessary heat sinking by using the heat spreading capabilities of the PC board, copper traces, and planes. Surface mount heat sinks, plated through-holes and solder-filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the packages to the heat sinking material.

Note that the exposed pad of the DFN and TSSOP packages and the tab of the DD-PAK and TO-220 packages are electrically connected to the output (V_{OUT}).

Tables 3 through 5 list thermal resistance as a function of copper areas on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm. Layers are not connected electrically or thermally.

Table 3. DF Package, 12-Lead DFN

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	18°C/W
1000mm^2	2500mm^2	2500mm^2	22°C/W
225mm^2	2500mm^2	2500mm^2	29°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside.

Table 4. FE Package, 16-Lead TSSOP

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	16°C/W
1000mm^2	2500mm^2	2500mm^2	20°C/W
225mm^2	2500mm^2	2500mm^2	26°C/W
100mm^2	2500mm^2	2500mm^2	32°C/W

*Device is mounted on topside.

Table 5. Q Package, 5-Lead DD-PAK

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	13°C/W
1000mm^2	2500mm^2	2500mm^2	14°C/W
125mm^2	2500mm^2	2500mm^2	16°C/W

*Device is mounted on topside.

T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 3°C/W

For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. Tables 3 through 5 provide thermal resistance numbers for best-case 4-layer boards with 1oz internal and 2oz external copper. Modern, multilayer PCBs may not be able to achieve quite the same level performance as found in these tables.

Calculating Junction Temperature

Example: Given an output voltage of 0.9V, a $V_{CONTROL}$ voltage of 3.3V ±10%, an IN voltage of 1.5V ±5%, output current range from 10mA to 3A and a maximum ambient temperature of 50°C, what will the maximum junction temperature be for the DD-PAK on a 2500mm^2 board with topside copper of 1000mm^2?

APPLICATIONS INFORMATION

The power in the drive circuit equals:

$$P_{DRIVE} = (V_{CONTROL} - V_{OUT})(I_{CONTROL})$$

where $I_{CONTROL}$ is equal to $I_{OUT}/60$. $I_{CONTROL}$ is a function of output current. A curve of $I_{CONTROL}$ vs I_{OUT} can be found in the Typical Performance Characteristics curves.

The total power equals:

$$P_{TOTAL} = P_{DRIVE} + P_{OUTPUT}$$

The current delivered to the SET pin is negligible and can be ignored.

$V_{CONTROL(MAX_CONTINUOUS)}$ = 3.630V (3.3V + 10%)

$V_{IN(MAX_CONTINUOUS)}$ = 1.575V (1.5V + 5%)

V_{OUT} = 0.9V, I_{OUT} = 3A, T_A = 50°C

Power dissipation under these conditions is equal to:

$$P_{DRIVE} = (V_{CONTROL} - V_{OUT})(I_{CONTROL})$$

$$I_{CONTROL} = \frac{I_{OUT}}{60} = \frac{3A}{60} = 50mA$$

P_{DRIVE} = (3.630V – 0.9V)(50mA) = 137mW

$P_{OUTPUT} = (V_{IN} - V_{OUT})(I_{OUT})$

P_{OUTPUT} = (1.575V – 0.9V)(3A) = 2.03W

Total Power Dissipation = 2.16W

Junction Temperature will be equal to:

$T_J = T_A + P_{TOTAL} \bullet \theta_{JA}$ (using tables)

T_J = 50°C + 2.16W • 16°C/W = 84.6°C

In this case, the junction temperature is below the maximum rating, ensuring reliable operation.

Reducing Power Dissipation

In some applications it may be necessary to reduce the power dissipation in the LT3083 package without sacrificing output current capability. Two techniques are available. The first technique, illustrated in Figure 7, employs a resistor in series with the regulator's input. The voltage drop across RS decreases the LT3083's input-to-output differential voltage and correspondingly decreases the LT3083's power dissipation.

As an example, assume: $V_{IN} = V_{CONTROL}$ = 5V, V_{OUT} = 3.3V and $I_{OUT(MAX)}$ = 2A. Use the formulas from the *Calculating Junction Temperature* section previously discussed.

Without series resistor R_S, power dissipation in the LT3083 equals:

$$P_{TOTAL} = (5V - 3.3V) \bullet \left(\frac{2A}{60}\right) + (5V - 3.3V) \bullet 2A$$

$$= 3.46W$$

If the voltage differential (V_{DIFF}) across the NPN pass transistor is chosen as 0.5V, then RS equals:

$$R_S = \frac{5V - 3.3V - 0.5V}{2A} = 0.6\Omega$$

Power dissipation in the LT3083 now equals:

$$P_{TOTAL} = (5V - 3.3V) \bullet \left(\frac{2A}{60}\right) + 0.5V \bullet 2A = 1.06W$$

The LT3083's power dissipation is now only 30% compared to no series resistor. R_S dissipates 2.4W of power. Choose appropriate wattage resistors or use multiple resistors in parallel to handle and dissipate the power properly.

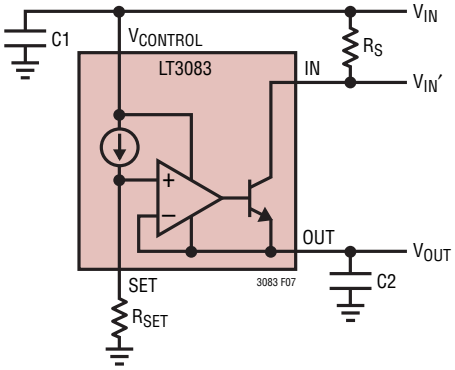


Figure 7. Reducing Power Dissipation Using a Series Resistor

APPLICATIONS INFORMATION

The second technique for reducing power dissipation, shown in Figure 8, uses a resistor in parallel with the LT3083. This resistor provides a parallel path for current flow, reducing the current flowing through the LT3083. This technique works well if input voltage is reasonably constant and output load current changes are small. This technique also increases the maximum available output current at the expense of minimum load requirements.

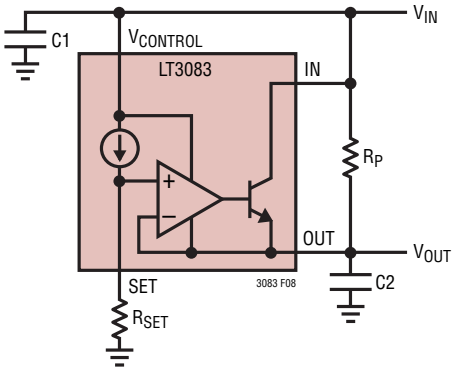


Figure 8. Reducing Power Dissipation Using a Parallel Resistor

As an example, assume: $V_{IN} = V_{CONTROL} = 5V$, $V_{IN(MAX)} = 5.5V$, $V_{OUT} = 3.3V$, $V_{OUT(MIN)} = 3.2V$, $I_{OUT(MAX)} = 2A$ and $I_{OUT(MIN)} = 0.7A$. Also, assuming that R_P carries no more than 90% of $I_{OUT(MIN)} = 630mA$.

Calculating R_P yields:

$$R_P = \frac{5.5V - 3.2V}{0.63A} = 3.65\Omega$$

(5% Standard Value = 3.6Ω)

The maximum total power dissipation is (5.5V – 3.2V) • 2A = 4.6W. However, the LT3083 supplies only:

$$2A - \frac{5.5V - 3.2V}{3.6\Omega} = 1.36A$$

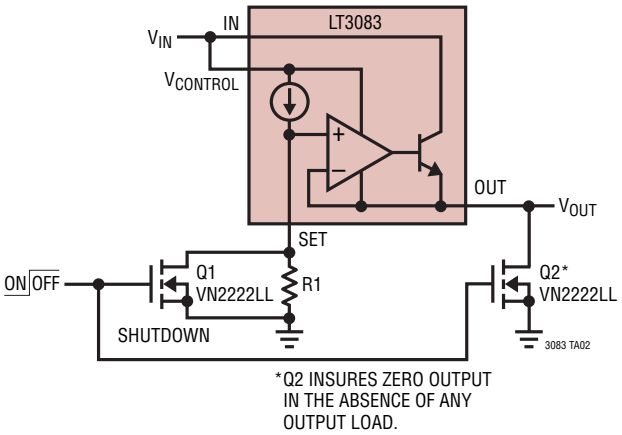
Therefore, the LT3083's power dissipation is only:

$$P_{DISS} = (5.5V - 3.2V) \bullet 1.36A = 3.13W$$

R_P dissipates 1.47W of power. As with the first technique, choose appropriate wattage resistors to handle and dissipate the power properly. With this configuration, the LT3083 supplies only 1.36A. Therefore, load current can increase by 1.64A to a total output current of 3.64A while keeping the LT3083 in its normal operating range.

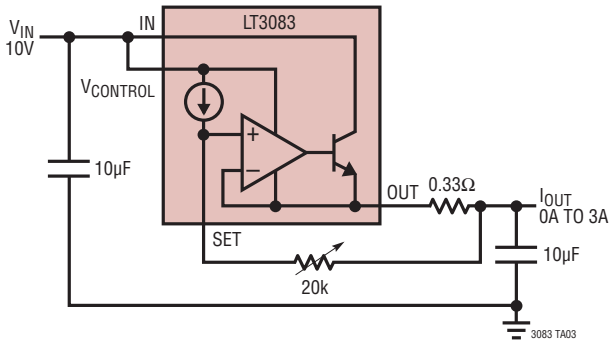
TYPICAL APPLICATIONS

Adding Shutdown

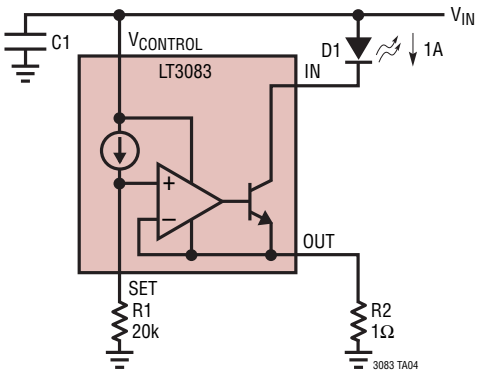


*Q2 INSURES ZERO OUTPUT IN THE ABSENCE OF ANY OUTPUT LOAD.

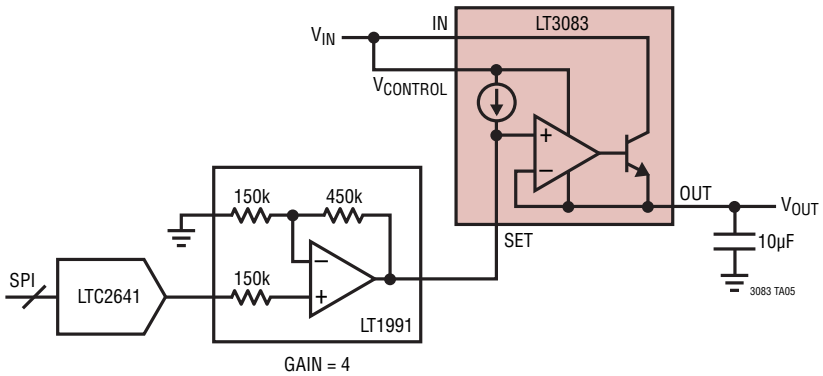
Current Source



Low Dropout Voltage LED Driver



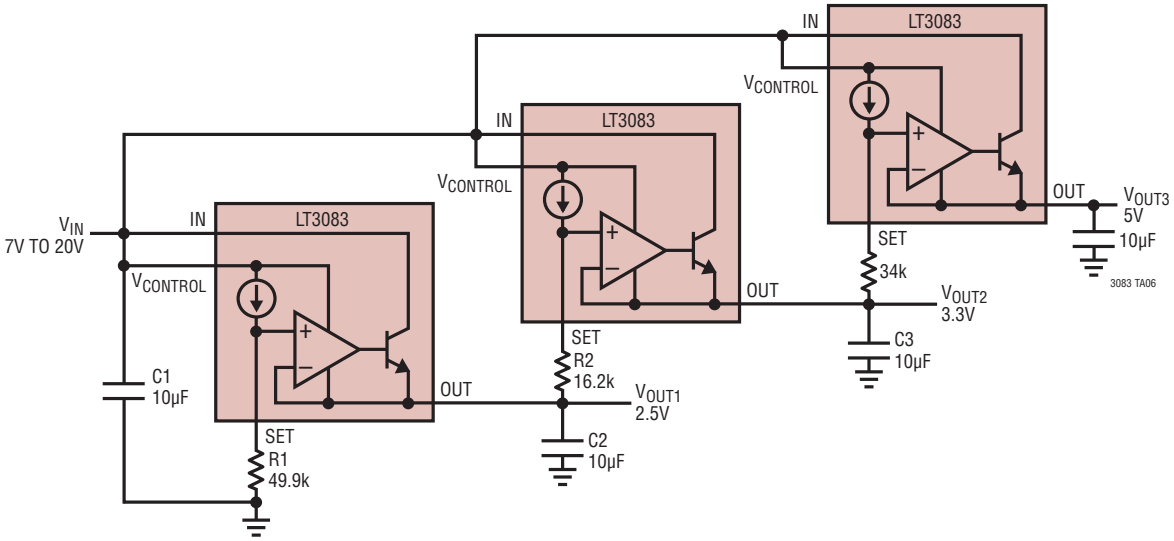
DAC-Controlled Regulator



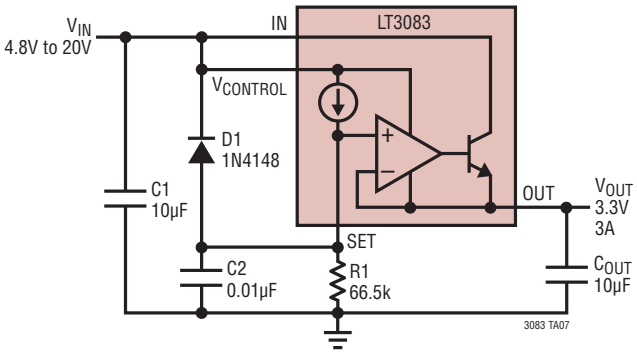
GAIN = 4

TYPICAL APPLICATIONS

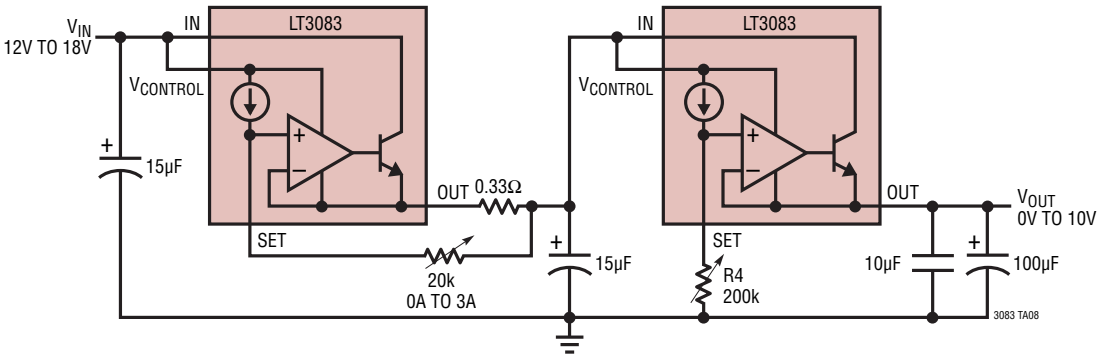
Coincident Tracking



Adding Soft-Start

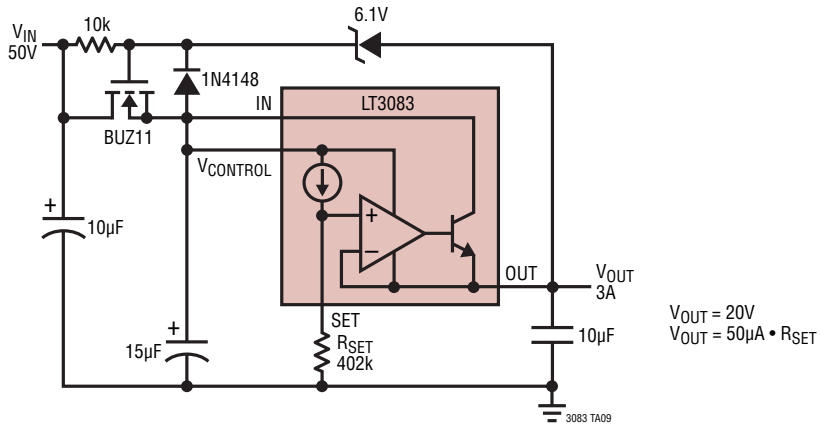


Lab Supply



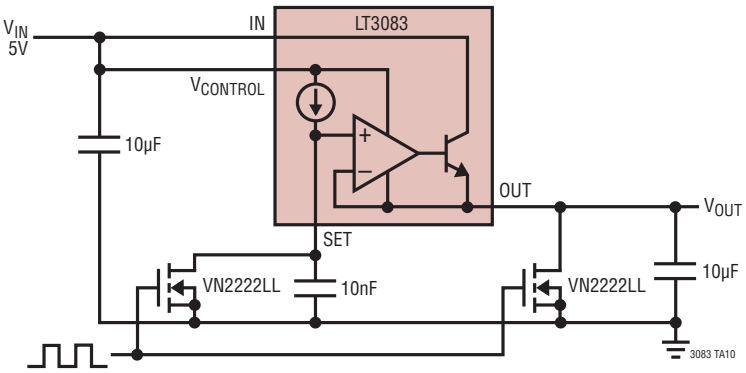
TYPICAL APPLICATIONS

High Voltage Regulator

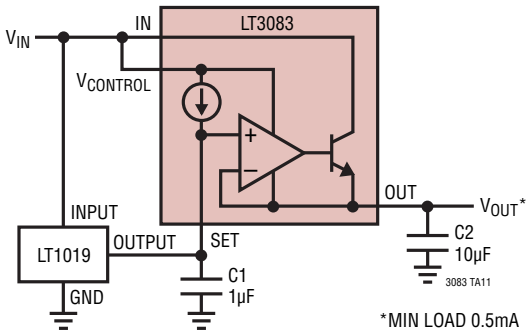


V_{OUT} = 20V
V_{OUT} = 50µA • R_{SET}

Ramp Generator

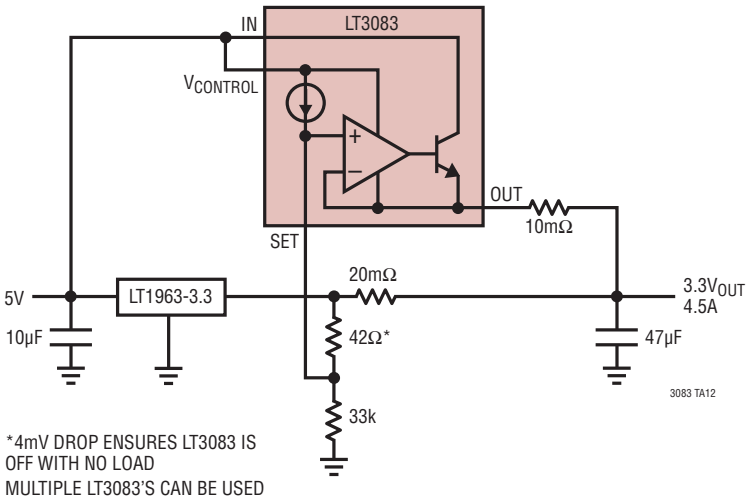


Reference Buffer



*MIN LOAD 0.5mA

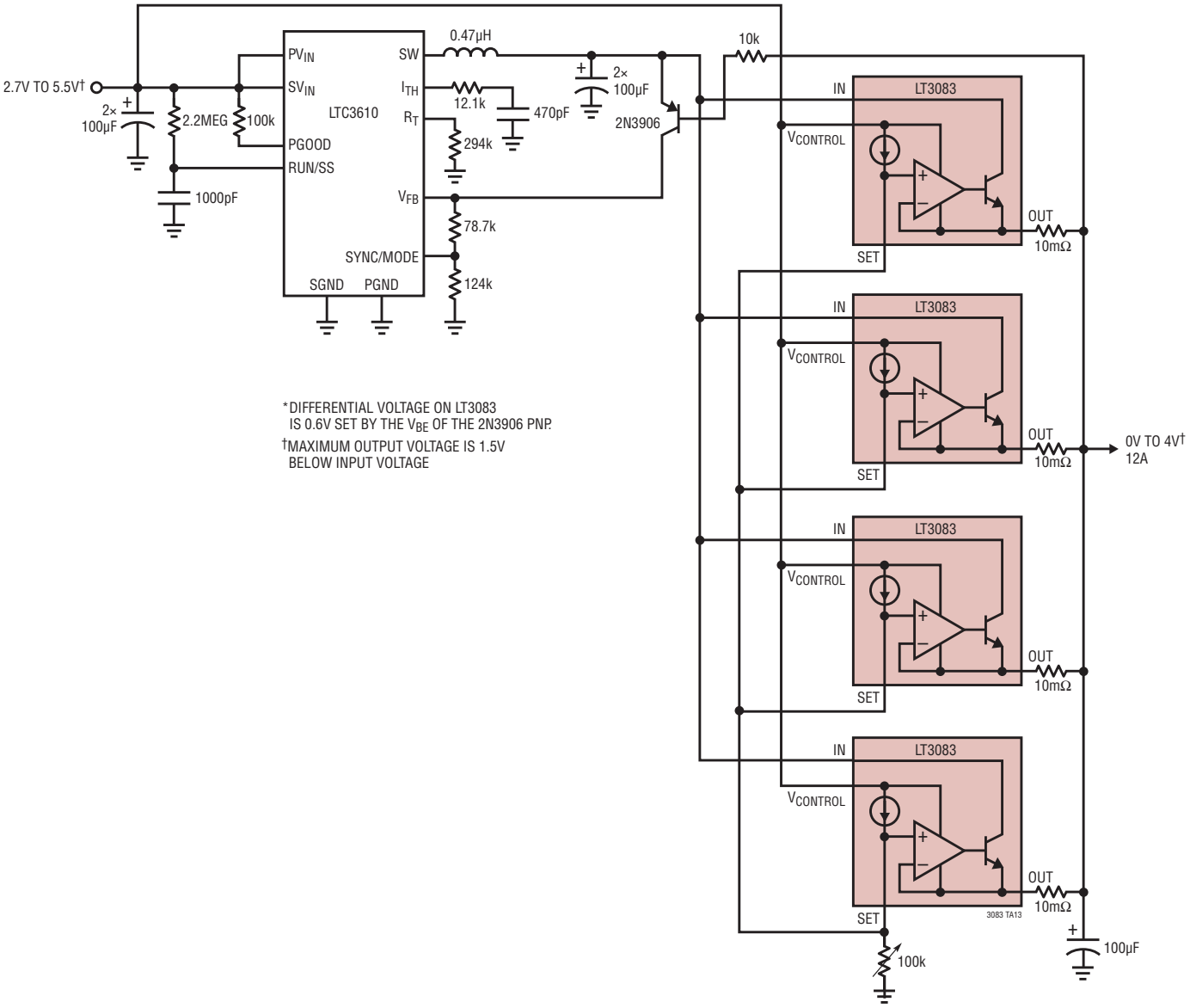
Boosting Fixed Output Regulators



*4mV DROP ENSURES LT3083 IS OFF WITH NO LOAD
MULTIPLE LT3083'S CAN BE USED

TYPICAL APPLICATIONS

Low Voltage, High Current Adjustable High Efficiency Regulator*

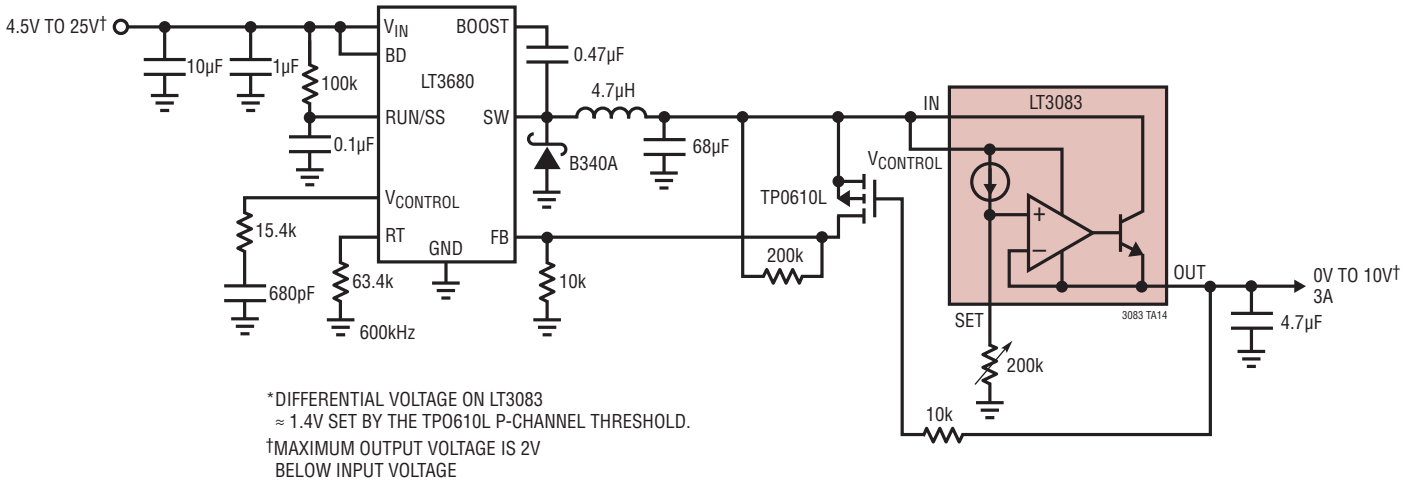


*DIFFERENTIAL VOLTAGE ON LT3083 IS 0.6V SET BY THE V_{BE} OF THE 2N3906 PNP.

†MAXIMUM OUTPUT VOLTAGE IS 1.5V BELOW INPUT VOLTAGE

TYPICAL APPLICATIONS

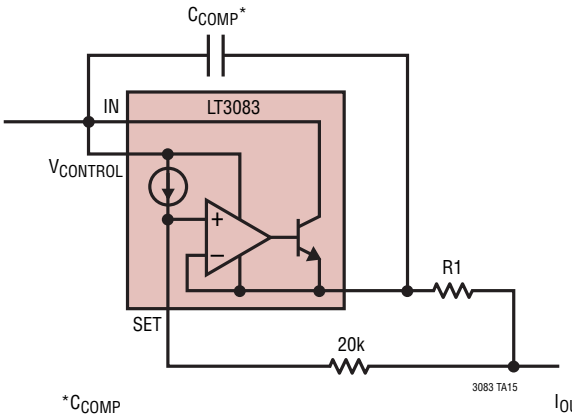
Adjustable High Efficiency Regulator*



*DIFFERENTIAL VOLTAGE ON LT3083
≈ 1.4V SET BY THE TPO610L P-CHANNEL THRESHOLD.

†MAXIMUM OUTPUT VOLTAGE IS 2V
BELOW INPUT VOLTAGE

2 Terminal Current Source



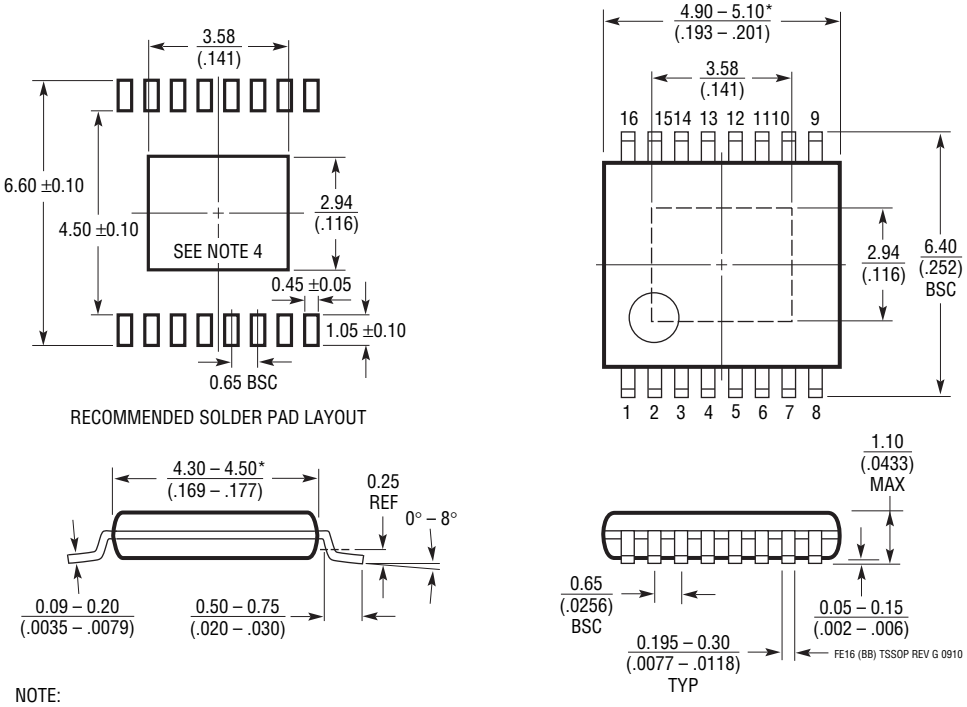
*CCOMP
R1 ≤ 10Ω 10µF
R1 ≥ 10Ω 2.2µF

$I_{OUT} = \frac{1V}{R1}$

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev H)

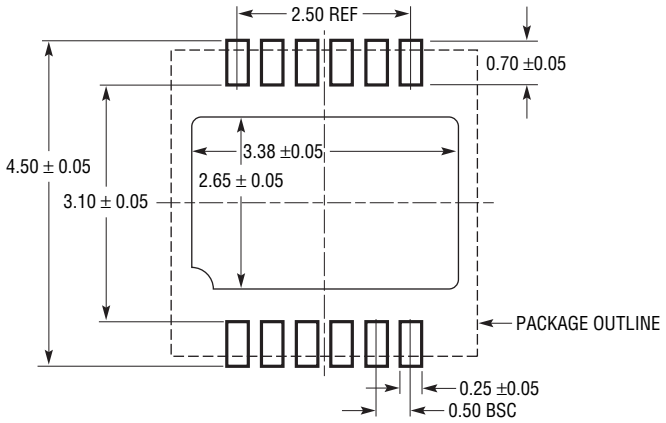
Exposed Pad Variation BB



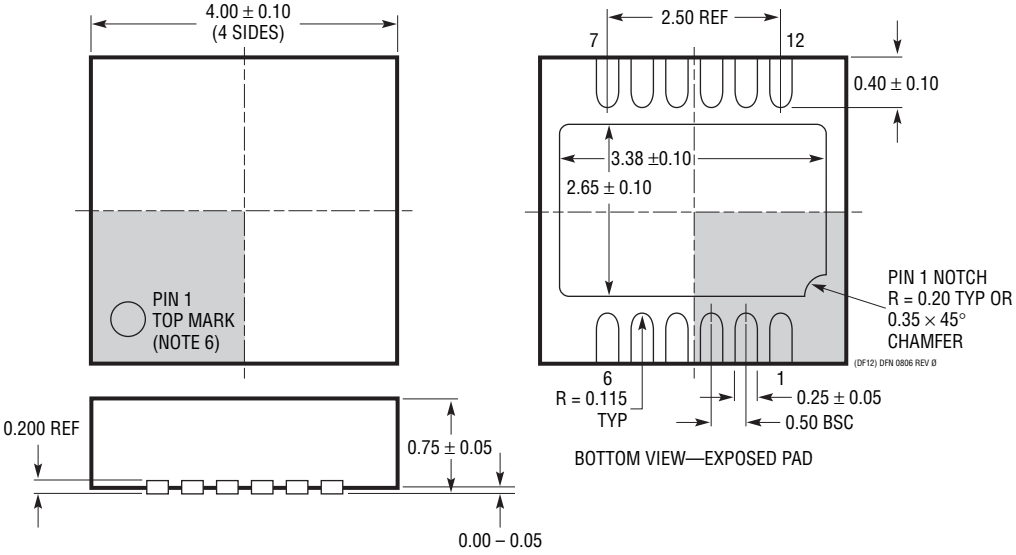
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

DF Package
12-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1733 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

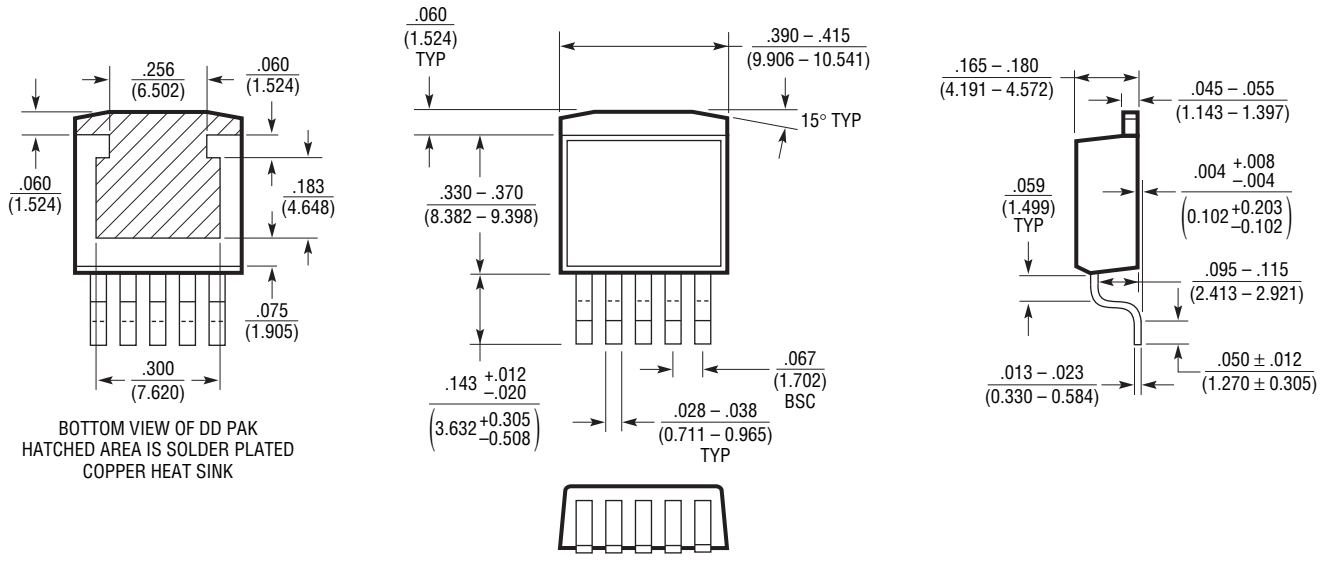


BOTTOM VIEW—EXPOSED PAD

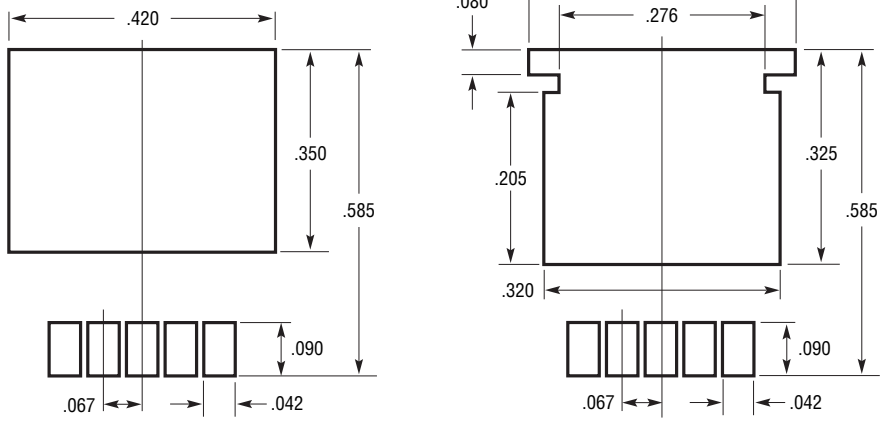
NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Q Package
5-Lead Plastic DD-PAK
(Reference LTC DWG # 05-08-1461 Rev E)



BOTTOM VIEW OF DD PAK
HATCHED AREA IS SOLDER PLATED
COPPER HEAT SINK



RECOMMENDED SOLDER PAD LAYOUT

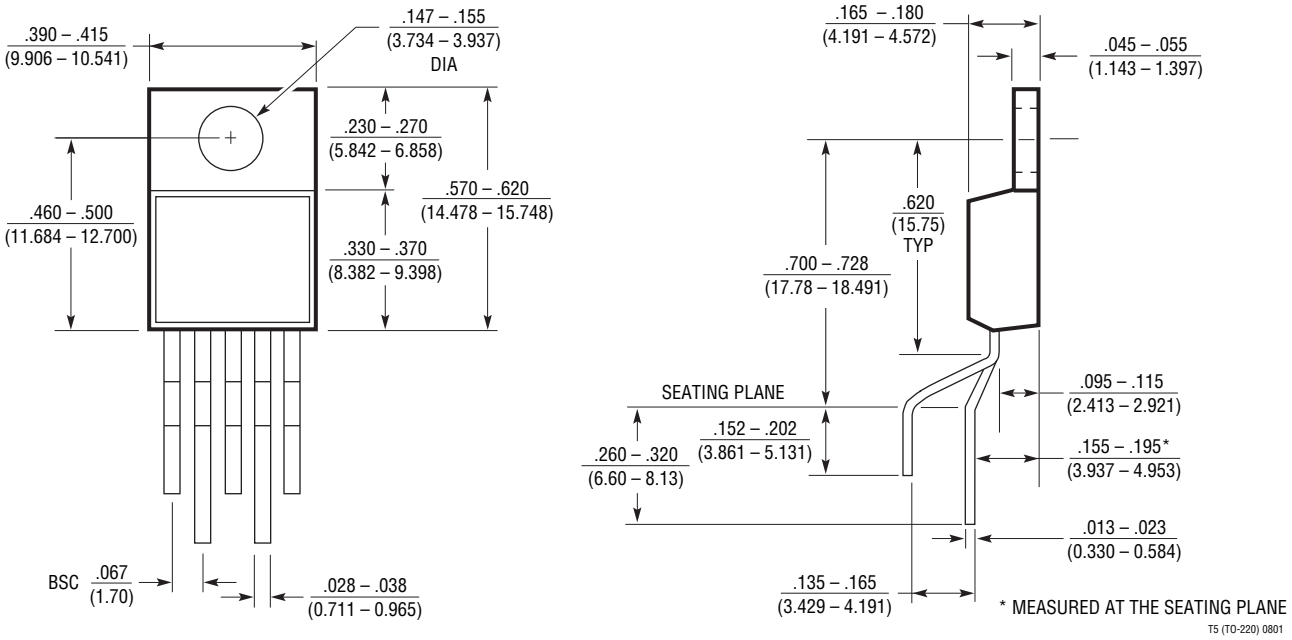
RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

Q(DD5) 0610 REV E

PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



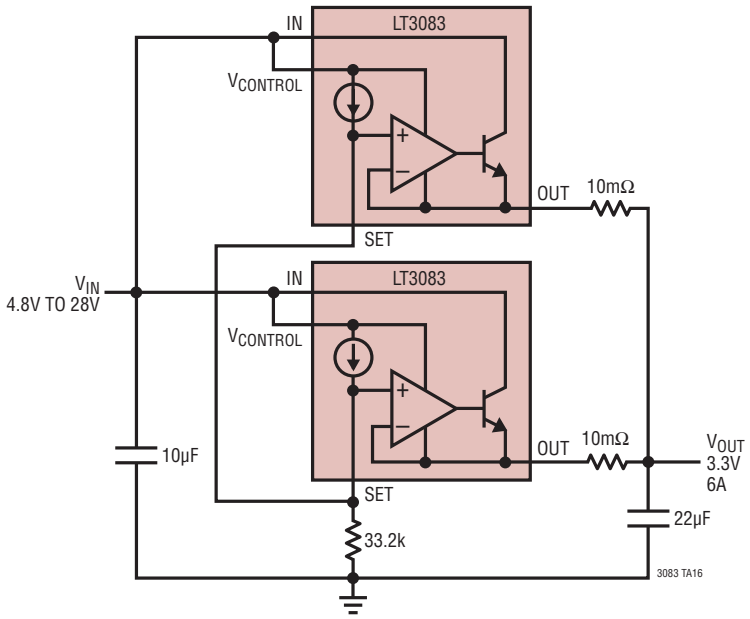
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/11	Revised part markings in Order Information section	3

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Paralleling Regulators



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1185	3A Negative Low Dropout Regulator	V_{IN}: –4.5V to –35V, 0.8V Dropout Voltage, DD-PAK and TO-220 Packages
LT1764/ LT1764A	3A, Fast Transient Response, Low Noise LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.7V to 20V, TO-220 and DD Packages. "A" Version Stable Also with Ceramic Capacitors
LT1963/A	1.5A Low Noise, Fast Transient Response LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.5V to 20V, "A" Version Stable with Ceramic Capacitors, TO-220, DD, SOT-223 and SO-8 Packages
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-PAK, MSOP and 3mm × 3mm DFN Packages
LT3022	1A, Low Voltage, VLDO Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage: 145mV Typical, Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Stable with Low ESR, Ceramic Output Capacitors, 16-Pin DFN (5mm × 3mm) and 16-Lead MSOP Packages
LT3070	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	Dropout Voltage: 85mV, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise: 25µV_{RMS} (10Hz to 100kHz), Parallelable: Use Two for a 10A Output, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT3071	5A, Low Noise, Programmable Vout, 85mV Dropout Linear Regulator with Analog Margining	Dropout Voltage: 85mV, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Analog Margining: ±10%, Low Output Noise: 25µV_{RMS} (10Hz to 100kHz), Parallelable: Use Two for a 10A Output, I_{MON} Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, DD-PAK, SOT-223, MS8E and 3mm × 3mm DFN-8 Packages; "-1" Version Has Integrated Internal Ballast Resistor
LT3082	200mA, Parallelable, Single Resistor, Low Dropout Linear Regulator	Outputs May Be Paralleled for Higher Output, Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 0.22µF, Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, MS8E and 2mm × 3mm DFN-6 Packages
LTC3026	1.5A, Low Input Voltage VLDO Linear Regulator	V_{IN}: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V), V_{DO} = 0.1V, I_Q = 950µA, Stable with 10µF Ceramic Capacitors, 10-Lead MSOP-E and DFN-10 Packages

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