75V DC/DC Converter for APD Bias

FEATURES

- **High APD Voltage: Up to 70V**
- **Integrated Schottky Diode**
- **75V, 370mA Internal Switch**
- **High Side Fixed Voltage Drop APD Current Monitor**
- Adjustable Frequency: 250kHz to 2MHz
- Frequency Synchronization
- Wide V_{IN} Range: 2.7V to 20V
- Constant-Voltage and Constant-Current Regulation
- Programmable Current Limit Protection
- Surface Mount Components
- Low Shutdown Current <1µA
- Internal Soft-Start
- Internal Compensation
- CTRL Pin Allows Output Adjustment with No Polarity Inversion
- 3mm × 3mm 16-Lead QFN Package

APPLICATIONS

- APD Bias
- PIN Diode Bias
- Optical Receivers and Modules
- Fiber Optic Network Equipment

DESCRIPTION

The LT®3571 is a current mode step-up DC/DC converter designed to bias avalanche photodiodes (APDs) in optical receivers with an output voltage up to 75V. The LT3571 features a high side fixed voltage drop APD current monitor with better than 10% relative accuracy over the entire temperature range. The integrated power switch, Schottky diode and APD current monitor allow a small solution footprint and low solution cost. It combines a traditional voltage loop and a unique current loop to operate as a constant-current source or constant-voltage source. The inductor-based topology ensures an input free from switching noise. The integrated high side current monitor produces a current proportional to the APD current with better than 10% relative accuracy over four decades of dynamic range in the input range of 250nA to 2.5mA. This current can be used as a reference to provide a digitally programmed output voltage via the CTRL pin. The LT3571 is available in the tiny footprint (3mm × 3mm) 16-lead QFN package.

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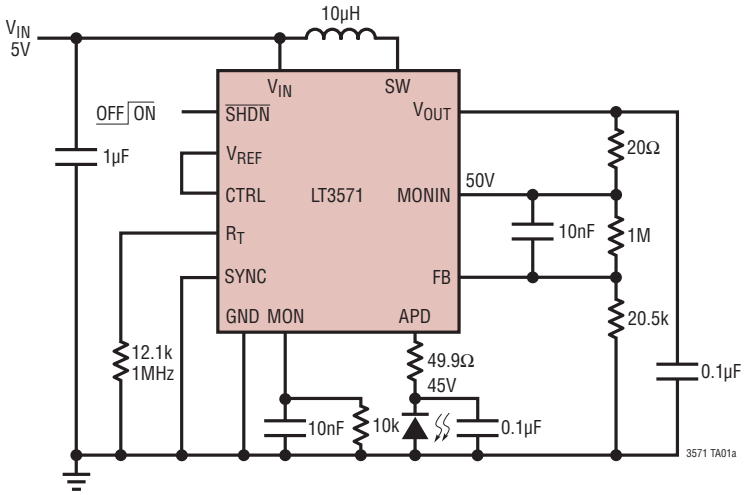
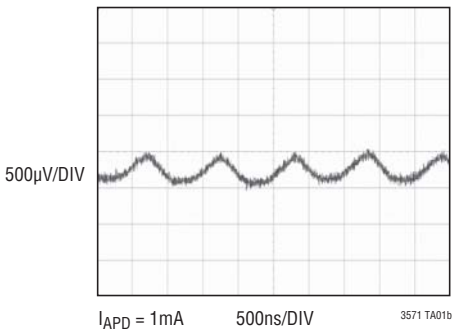
TYPICAL APPLICATION

45V Low Noise APD Bias Power Supply



APD Bias Ripple

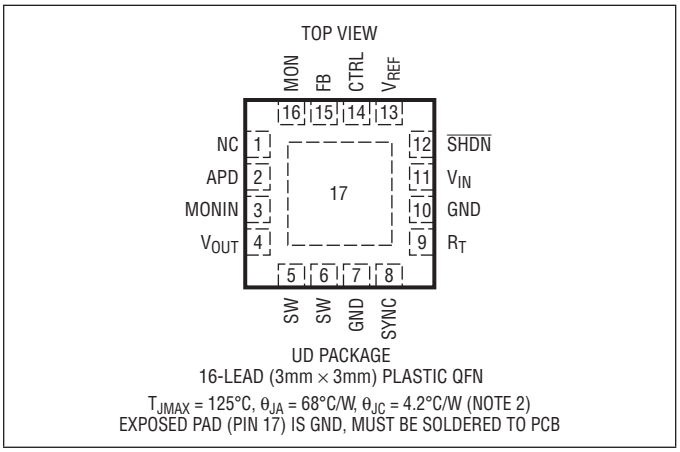


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (V_{IN}), $\overline{SHDN}$ 20V
V_{OUT}, MONIN, APD.....75V
MON.....12V
SW.....75V
CTRL, FB, SYNC.....5V
R_T, V_{REF} 1.5V
Operating Ambient Temperature Range
(Note 2) .....–40°C to 125°C
Operating Junction Temperature
(Note 2) .....–40°C to 125°C
Storage Temperature Range.....–65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W (NOTE 2)
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3571EUD#PBF	LT3571EUD#TRPBF	LDTN	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3571IUD#PBF	LT3571IUD#TRPBF	LDTN	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3V, $V_{\overline{SHDN}}$ = 3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage					2.7	V
Maximum Operating Voltage					20	V
Supply Current	V_{FB} = 1.3V, Not Switching $V_{\overline{SHDN}}$ = 0V			1.7 0.1	2.2 0.5	mA µA
Feedback Voltage	V_{CTRL} = 1.25V, V_{OUT} = V_{MONIN}	 ●	0.985 0.97	1	1.015 1.03	V V
Feedback Line Regulation	2.7V < V_{IN} < 20V			0.03	0.07	%/V
Current Sense Voltage (V_{OUT} – V_{MONIN})	V_{OUT} = 30V	●	185	200	215	mV
FB Pin Bias Current	V_{FB} = 0V	●		60	100	nA
V_{REF} Pin Voltage	I_{REF} = –100µA	●	1.200	1.222	1.240	V
V_{REF} Pin Line Regulation	2.7V < V_{IN} < 20V			0.03	0.07	%V
R_T Voltage				1		V
SYNC Resistance to GND	V_{SYNC} = 2V			45		kΩ
SYNC Input Low					0.4	V
SYNC Input High			1.5			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3V, $V_{\overline{SHDN}}$ = 3V, unless otherwise noted.

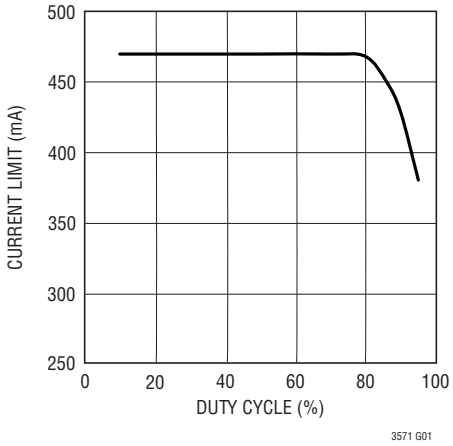
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency	R_T = 12.1k R_T = 4.22k R_T = 56.2k	● 	0.85 1.7 210	1 2 250	1.15 2.3 280	MHz MHz kHz
Maximum Duty Cycle	R_T = 56.2k (250kHz) SYNC = 300kHz Clock Signal, R_T = 56.2k R_T = 12.1k (1MHz) R_T = 4.22k (2MHz)	 ● 	95 92 85 75	97 96 90 80	 	% % % %
Switch Current Limit			370	470	570	mA
Switch V_{CESAT}	I_{SW} = 200mA			240		mV
Switch Leakage Current	V_{SW} = 75V				2	µA
Schottky Forward Voltage	$I_{SCHOTTKY}$ = 200mA			850		mV
Schottky Reverse Leakage	$V_{OUT} - V_{SW}$ = 75V				5	µA
$\overline{SHDN}$ Voltage High			1.5			V
$\overline{SHDN}$ Voltage Low					0.4	V
$\overline{SHDN}$ Pin Bias Current				50	65	µA
CTRL to FB Offset	V_{CTRL} = 0.5V	 ●	–5 –10	5 5	15 20	mV mV
CTRL Input Bias Current	Current Out of Pin, V_{CTRL} = 0.5V			20	100	nA
APD Current Monitor Gain	250nA ≤ I_{APD} < 10µA, 10V < V_{MONIN} < 75V 10µA ≤ I_{APD} ≤ 2.5mA, 20V < V_{MONIN} < 75V	● ●	0.185 0.194	0.20 0.20	0.215 0.206	
Monitor Output Voltage Clamp				11.5		V
APD Monitor Voltage Drop	$V_{MONIN} - V_{APD}$, I_{APD} = 1mA	●	4.8	5	5.2	V
MONIN Pin Current Limit	V_{MONIN} = 40V, V_{APD} = 0V			30		mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

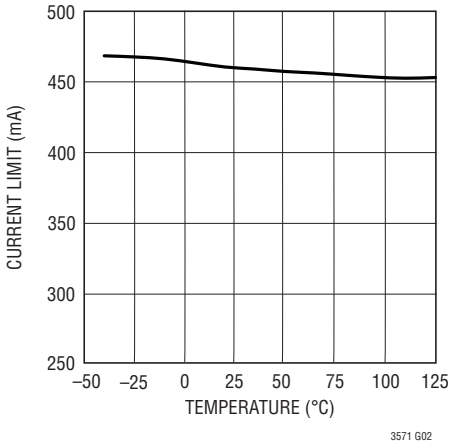
Note 2: The LT3571E is guaranteed to meet specified performance from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3571I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

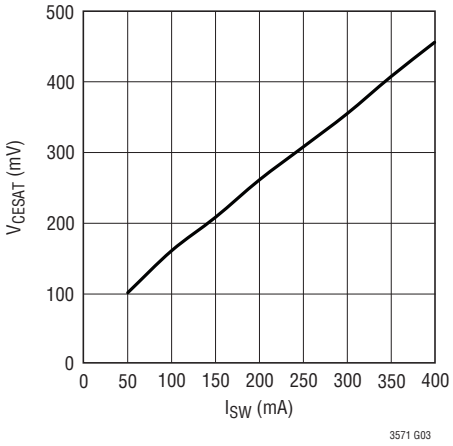
Switch Current Limit vs Duty Cycle



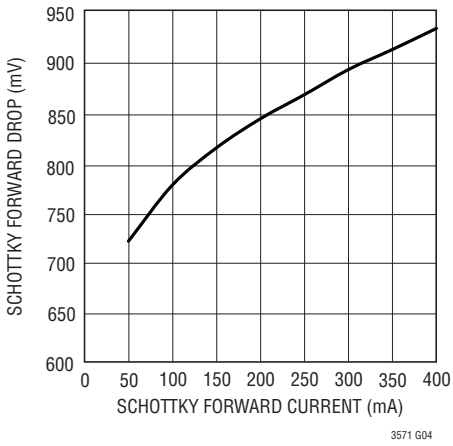
Switch Current Limit vs Temperature



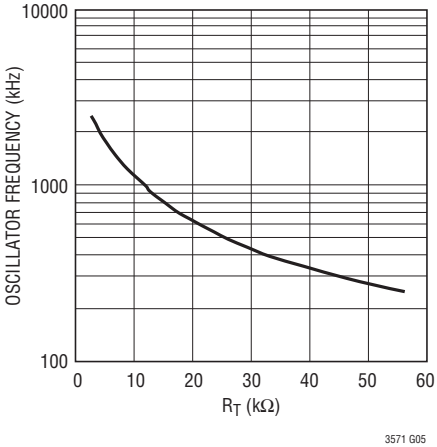
Switch Saturation Voltage (V_{CESAT})



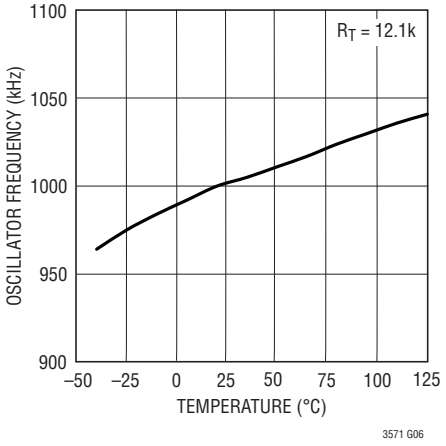
Schottky Forward Drop



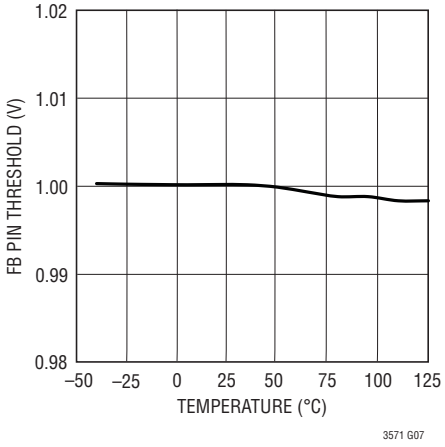
Oscillator Frequency vs R_T



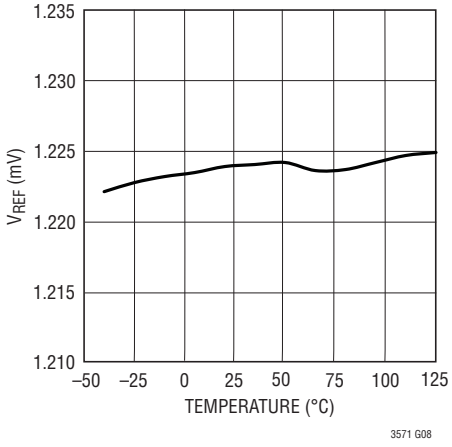
Oscillator Frequency vs Temperature



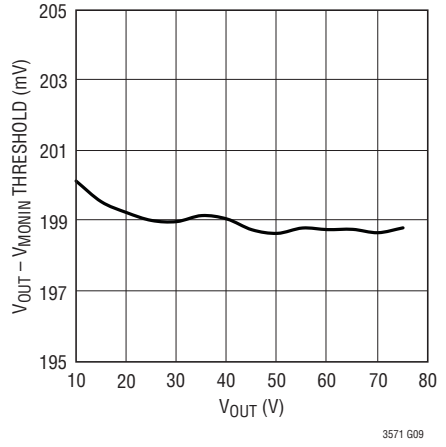
FB Pin Voltage vs Temperature



V_{REF} Voltage vs Temperature

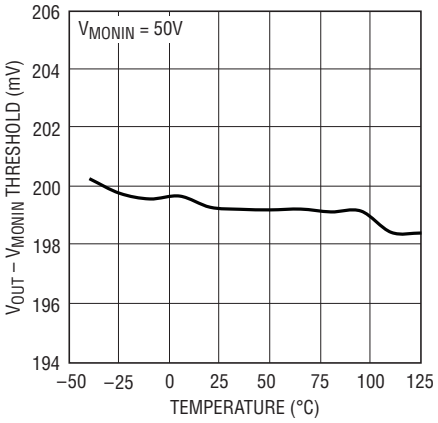


V_{OUT} – V_{MONIN} Threshold vs V_{OUT}

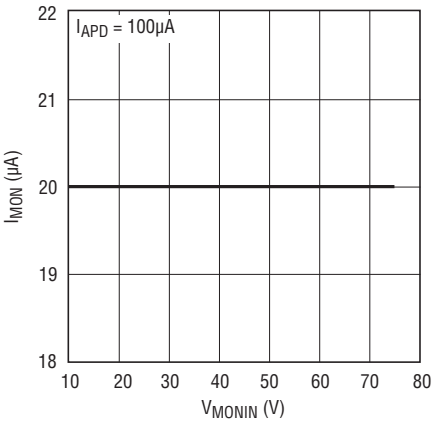


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

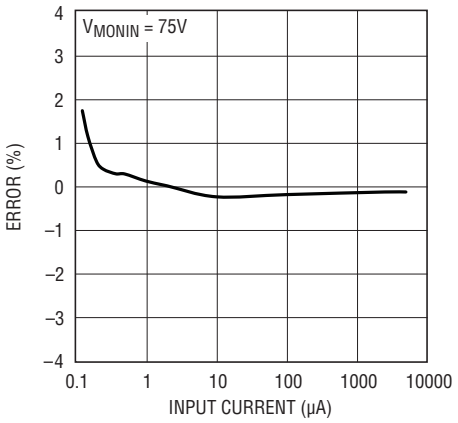
V_{OUT} – V_{MONIN} Threshold vs Temperature



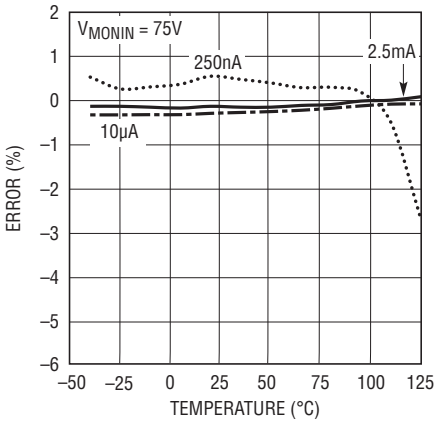
Current Monitor Output vs V_{MONIN}



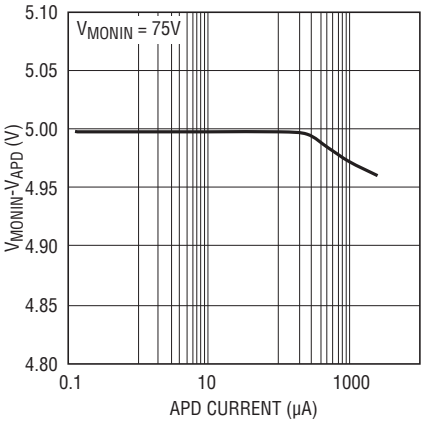
Current Monitor Accuracy



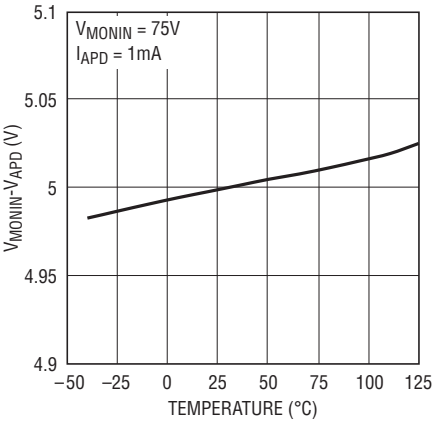
Current Monitor Accuracy vs Temperature



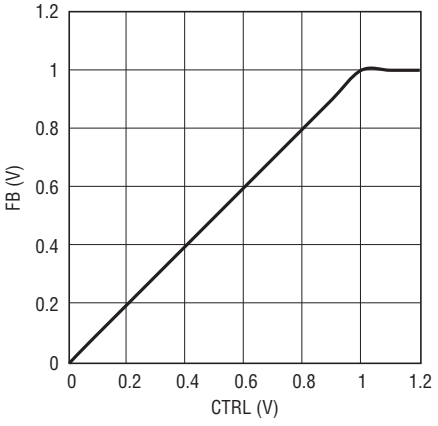
V_{MONIN} - V_{APD} vs APD Current



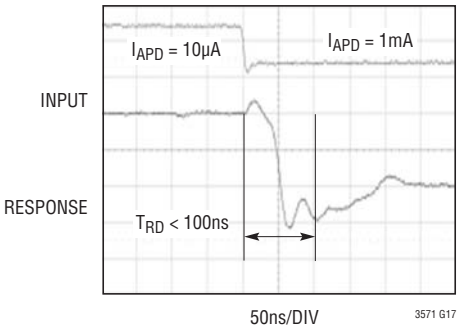
V_{MONIN} – V_{APD} vs Temperature



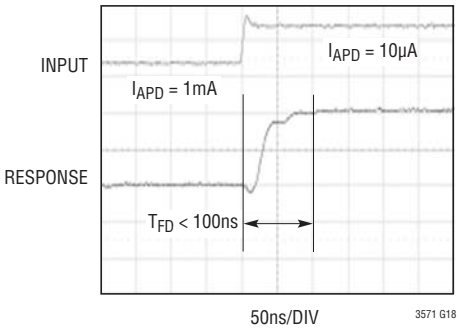
FB vs CTRL



Current Monitor Transient Response (Rising Edge)



Current Monitor Transient Response (Falling Edge)



PIN FUNCTIONS

NC (Pin 1): No Connect.

APD (Pin 2): APD Cathode Pin. Connect APD cathode to this pin.

MONIN (Pin 3): Current Monitor Power Supply Pin. An external lowpass filter can be included here to further reduce supply voltage ripple. This pin also serves as the inverting input of the current sense amplifier. Put a sense resistor between the MONIN pin and the V_{OUT} pin to set the boost converter output current limit as 200mV/R_{SENSE}. Connect the MONIN pin directly to the V_{OUT} pin if the output current limit function is not used.

V_{OUT} (Pin 4): Boost Output Pin. Put a capacitor between this pin and GND plane. Minimize the length of the trace to the capacitor. Also serves as the noninverting input of the current sense amplifier.

SW (Pin 5, 6): Switch Pin. Minimize the trace length on this pin to reduce EMI.

GND (Pin 7, 10): Ground. Pins connected internally. For best performance, connect both pins to board ground.

SYNC (Pin 8): Frequency Synchronization Pin. Connect an external clock signal here. R_T resistor should be chosen to program a switching frequency 20% slower than the SYNC pulse frequency. Synchronization (switch turn-on) occurs a fixed delay after the rising edge of SYNC. Tie the SYNC pin to ground if this feature is not used.

R_T (Pin 9): Switching Frequency Pin. Set switching frequency using a resistor to GND (see Typical Performance Characteristics for values). For SYNC function, choose the resistor to program a frequency 20% slower than the SYNC pulse frequency. Do not leave this pin open.

V_{IN} (Pin 11): Input Supply Pin. This pin must be locally bypassed.

$\overline{SHDN}$ (Pin 12): Shutdown Pin. Tie to 1.5V or higher to enable device; 0.4V or less to disable device. Also functions as soft-start. Use RC filter as shown in Figure 1.

V_{REF} (Pin 13): Reference Output Pin. This pin can supply up to 100µA. Do not over drive this pin. Bypass with a 10nF or larger capacitor.

CTRL (Pin 14): Internal Reference Override Pin. The CTRL pin allows the FB voltage to be externally adjusted between 0V and 1V to adjust the output voltage. Tie this pin higher than 1.2V to use the internal reference of 1V.

FB (Pin 15): Feedback Pin. Connect to output resistor divider tap.

MON (Pin 16): Current Monitor Output Pin. Sources a current equal to 20% of the APD current and converts to a reference voltage through an external resistor.

Exposed Pad (Pin 17): Ground. The Exposed Pad must be soldered to the PCB.

BLOCK DIAGRAM

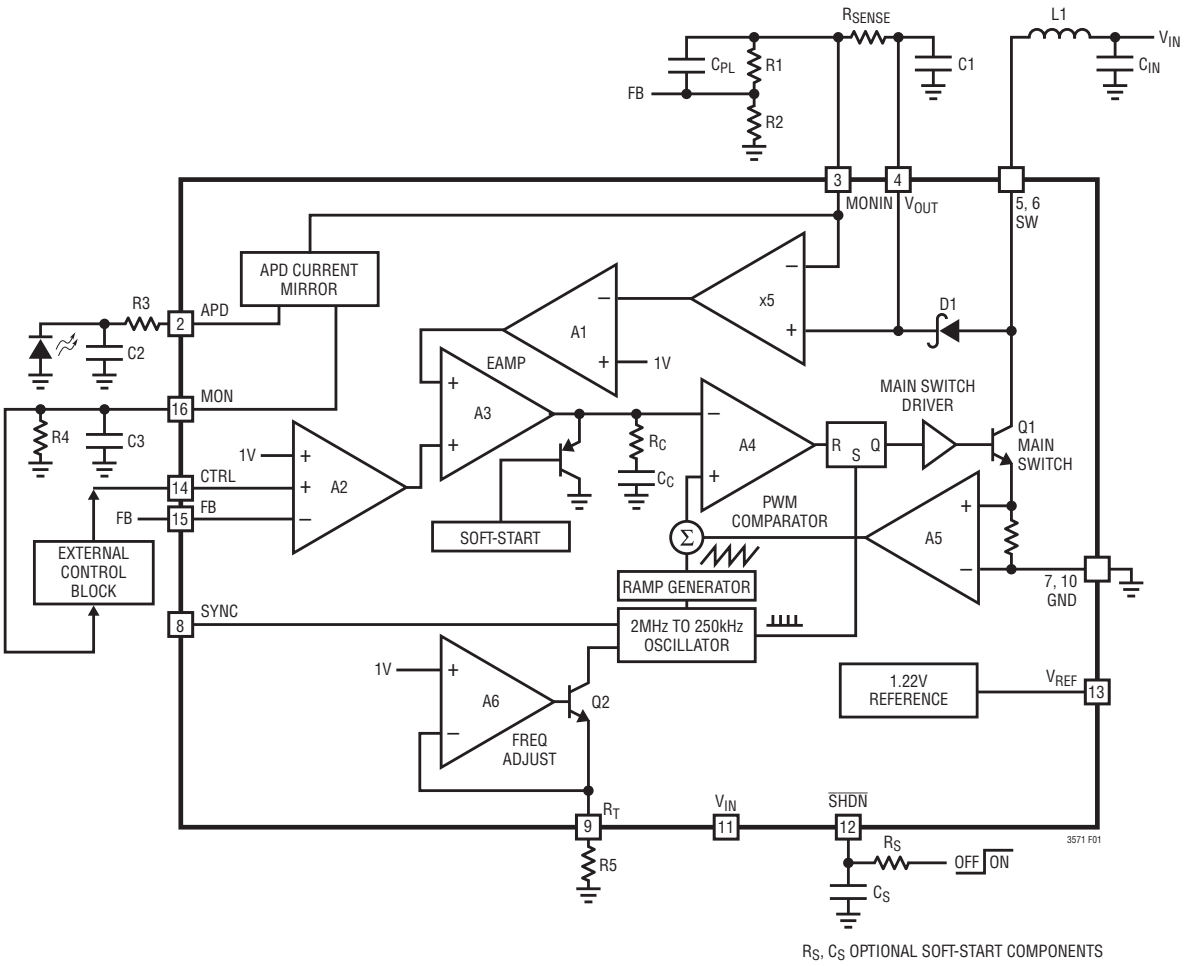


Figure 1. Block Diagram

OPERATION

The LT3571 boost converter uses a constant-frequency current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1. At the start of each oscillator cycle, the SR latch is set, which turns on the Q1 power switch. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator, A4. When this voltage exceeds the level at the negative input of A4, the SR latch is reset, turning off the power switch. The level at the negative input of A4 is set by the error amplifier A3. A3 has two inputs, one from the voltage feedback loop and the other one from the current loop. Whichever feedback input is lower takes precedence and forces the converter into either constant-current or constant-voltage mode. The LT3571 is designed to transition cleanly between these two modes of operation. The current sense amplifier senses the voltage across R_{SENSE} and provides a pre-gain to amplifier A1. The output of A1 is simply an amplified version of the difference between the voltage across R_{SENSE} and 200mV. In this manner, the error amplifier sets the correct peak switch current level to regulate through R_{SENSE}. The FB voltage loop is implemented by the amplifier A2. When the voltage loop dominates, the error amplifier regulates the FB pin to the lower of 1V, or externally provided CTRL voltage (constant-voltage mode), and sets the correct peak current level to keep the output in regulation.

The LT3571 has an integrated high side APD current monitor with a 5:1 ratio. The voltage drop across the MONIN pin and APD pin is fixed at 5V. The MONIN pin can accept a supply voltage up to 75V, which is suitable for APD photodiode applications. The MON pin has an open-circuit protection feature and is internally clamped to 11.5V.

If an APD is tied to the APD pin, the current will be mirrored to the MON pin and converted to a voltage signal by the resistor R4. This voltage signal can be used to drive an external control block to adjust the APD voltage by adjusting the feedback threshold of EAMP A2 through the CTRL input.

APPLICATIONS INFORMATION

Switching Frequency

There are two methods to set the switching frequency of the LT3571. Both methods require a resistor connected at the R_T pin. Do not leave the R_T pin open. Also, do not load this pin with a capacitor. A resistor must always be connected for proper operation. One way to set the frequency is simply connecting an external resistor between the R_T pin and GND. See Table 1 or the Oscillator Frequency vs R_T graph in the Typical Performance Characteristics for resistor values and corresponding switching frequencies. The other way is to make the LT3571 synchronize with an external clock via the SYNC pin. For proper operation, a resistor should be connected at the R_T pin and able to generate a switching frequency 20% lower than the external clock when the external clock is absent.

Table 1. Switching Frequency vs R_T

Switching Frequency (kHz)	R_T (k)
250	56.2
500	26.1
1000	12.1
1500	6.81
2000	4.22
2500	2.67

Inrush Current

The LT3571 has a built-in Schottky diode for the boost converter. When supply voltage is applied to the V_{IN} pin, the voltage difference between V_{IN} and V_{OUT} generates inrush current flowing from input through the inductor and the Schottky diode (D1 in the Block Diagram), to charge the output capacitor. The selection of inductor and capacitor value should ensure the peak of the inrush current to below 1A. In addition, the LT3571 turn-on should be delayed until the inrush current is less than the maximum current limit. The peak inrush current can be estimated as follows:

$$I_P = \frac{V_{IN} - 0.9}{\sqrt{\frac{L}{C} - 1}} \bullet \exp\left(-\frac{\pi}{2\sqrt{\frac{L}{C} - 1}}\right)$$

where L is the inductance, and C is the output capacitance.

Table 2 gives inrush peak currents for some component selections.

Table 2. Inrush Peak Current

V_{IN} (V)	L (µH)	C (µF)	I_P (A)
5	10	1	0.81
5	22	1	0.63

Setting Output Voltage

The LT3571 is equipped with both an internal 1V reference and an auxiliary reference input (the CTRL pin). This feature allows users to select between using the built-in reference and supplying an external reference voltage. The voltage at the CTRL pin can be adjusted while the chip is operating, to alter the output voltage of LT3571 for purposes such as APD's bias voltage adjustment. To use the internal 1V reference, the CTRL pin should be held higher than 1.2V, which can be done by tying it to V_{REF}. When the CTRL pin is between 0V and 1V, the LT3571 will regulate the output such that the FB pin voltage is equal to the CTRL pin voltage. To set the output voltage, select the values of R1 and R2 (see Figure 2) according to the following equation:

$$R1 = R2\left(\frac{V_{MONIN}}{V1} - 1\right)$$

where V1 = 1V if the internal reference is used, or V1 = CTRL if CTRL is between 0V and 1V. R2 can be selected to load the output to maintain a constant switching frequency when the APD load is very low. Preventing entry into pulse-skipping mode is an important consideration for post filtering the regulator output.

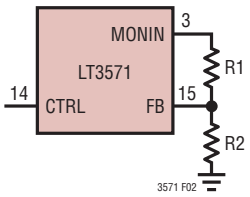


Figure 2. Output Voltage Feedback Connection

APPLICATIONS INFORMATION

Inductor Selection

The inductors used with the LT3571 should have a saturation current rating of 0.4A, or greater. If the device is used in an application where the input supply will be hot-plugged, the saturation current rating should be equal to, or greater than, the peak inrush current. For best loop stability, the inductor value selected should provide a ripple current of 80mA or more. For a given V_{IN} and V_{OUT}, the inductor value to use in continuous conduction mode (CCM) is estimated by the formula:

$$L = \frac{D \bullet V_{IN}}{f \bullet 80mA}$$

where:

$$D = \frac{V_{OUT} + 1 - V_{IN}}{V_{OUT} + 1}$$

and f is the switching frequency.

To achieve low output voltage ripple, a small value inductor should be selected to force the LT3571 to operate in discontinuous conduction mode (DCM). The inequality is true when the LT3571 is operating in discontinuous conduction mode.

$$L < \frac{D \bullet V_{IN}}{f \bullet I_{LIMIT}}$$

where I_{LIMIT} is the switch current limit. Operating in DCM reduces the maximum load current and the conversion efficiency.

Capacitor Selection

Low ESR capacitors should be used at the output to minimize the output voltage ripple. Use only X5R and X7R types, because they retain their capacitance over wider voltage and temperature ranges than other types. High output voltages typically require less capacitance for loop stability. Typically, use a 1µF capacitor for output voltage less than 25V, and a 0.22µF capacitor for output voltage beyond 25V. Place the output capacitor as close as possible to the V_{OUT} lead and to the GND of the IC.

Either ceramic or solid tantalum capacitors may be used for the input decoupling capacitor, which should be placed as close as possible to the LT3571. A 1µF capacitor is sufficient for most applications.

Phase Lead Capacitor

A small value capacitor (i.e., 10pF to 22pF) can be added in parallel with the resistor between the output and the FB pin to reduce output perturbation due to a load step and to improve transient response. This phase lead capacitor introduces a pole-zero pair to the feedback that boosts the phase margin near the crossover frequency. The APD is very sensitive to a noisy bias supply. To lowpass filter noise from the internal reference and error amplifier, a 0.1µF phase lead capacitor can be used. The corner frequency of the noise filter is R1 • C_{PL}.

APD Current Monitor

The power supply switching noise associated with a switching power supply can interfere with the photodiode DC measurement. To suppress this noise, a 0.1µF capacitor is recommended at the APD pin. An additional series resistor is necessary to ensure enough high frequency compensation at the APD pin over the full operating range of the LT3571, as shown in Figure 1. An additional output lowpass filter, a 10k resistor and a 10nF capacitor in parallel at MON pin can further reduce the power supply noise, and other wide band noise, which might limit the measurement accuracy of low current levels.

For applications requiring fast current monitor response time, an RC lowpass filter at the MONIN pin is used to replace the 0.1µF capacitor at the APD pin, as illustrated in Figure 3.

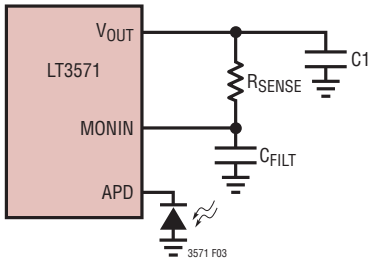


Figure 3. RC Filter at MONIN Pin

APPLICATIONS INFORMATION

APD Current Monitor Transient Response Measurement

The transient response of the APD current monitor is a key performance characteristic. It is essentially a function of the input step-signal levels, since the small signal bandwidth increases with the input signal. At greater than 10µA, the LT3571 APD current mirror typically has several hundred nanoseconds response time. To measure such fast transient response, any capacitor at the APD and the MON pin should be removed. Figure 4 shows a suggested transient response test setup. Choose V_L and V_H, corresponding to the input step current levels, respectively. At the MON pin, a wideband transimpedence amplifier is implemented using the LT1815. Operating in a shunt configuration, the amplifier buffers the MON output current and dramatically reduces the effective output impedence at the OUT node. Note that there is an inversion and a DC offset present when this measurement technique is used. A regular oscilloscope probe can then be used to capture the fast transient response at the OUT node.

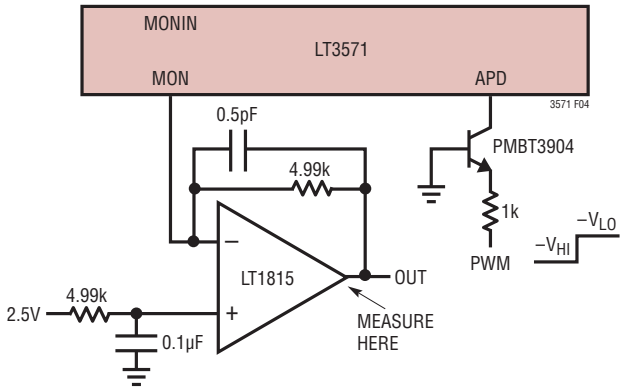


Figure 4. Transient Response Measurement Set-Up

APD Bias Voltage Temperature Compensation

Typically, the APD reverse bias voltage has a positive temperature coefficient. The APD pin voltage can be adjusted with temperature via the CTRL pin. One simple solution is to form a resistor divider from the V_{REF} pin to the CTRL pin, as shown in Figure 5. By carefully choosing the resistor values, a temperature coefficient can be applied to the APD reverse bias voltage. A more complicated and precise way to set the APD temperature coefficient involves a transistor network as shown in the "5V to 50V APD Bias Power Supply with Temperature Compensation". Please consult with factory for this type applications.

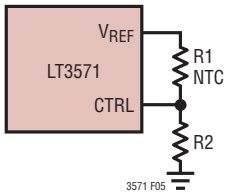


Figure 5. Setting Temperature Compensation

APPLICATIONS INFORMATION

Setting APD Current Limit

The LT3571 has a unique current loop to limit the APD current. Choose the sense resistor R_{SENSE} across V_{OUT} and MONIN pins to set the APD current limit by using the following formula:

$$R_{SENSE} = \frac{200mV}{1.2 \times I_{APD}\,(mA) + 0.3mA}$$

where I_{APD} is the APD current limit.

Layout Hints

The high speed operation of the LT3571 demands careful attention to board layout. Advertised performance will not be achieved with a careless layout. To prevent radiation and high frequency resonance problems, proper layout of the high frequency switching path is essential. Keep the output switch (SW pin), diode and output capacitor as close together as possible. Minimize the length and area of all traces connected to the switch pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The high speed switching current path is shown in Figure 6. The signal path, including the switch, output diode and output capacitor contains nanosecond rise and fall times and should be kept as short as possible.

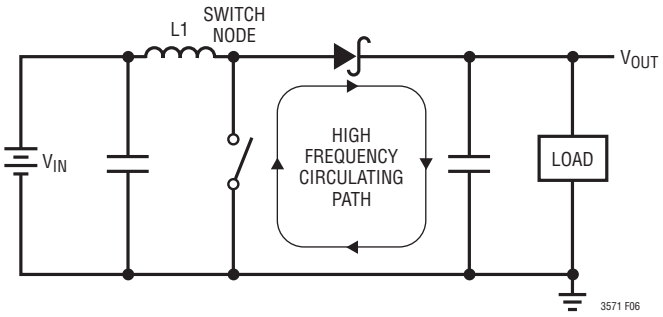
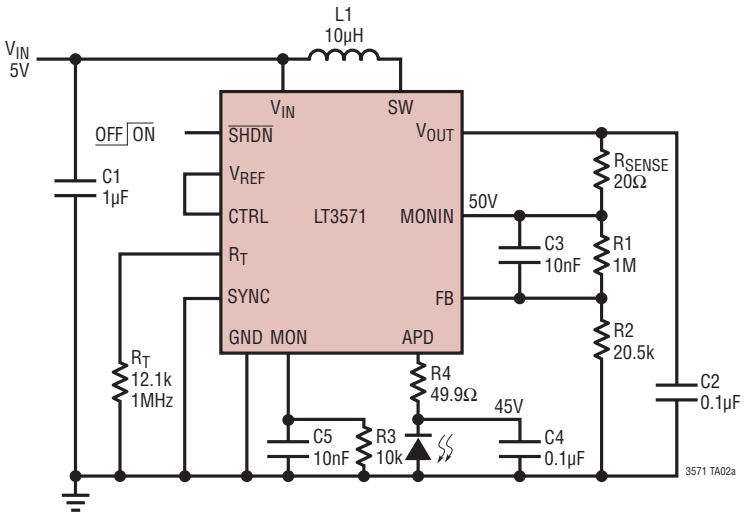


Figure 6. High Frequency Path

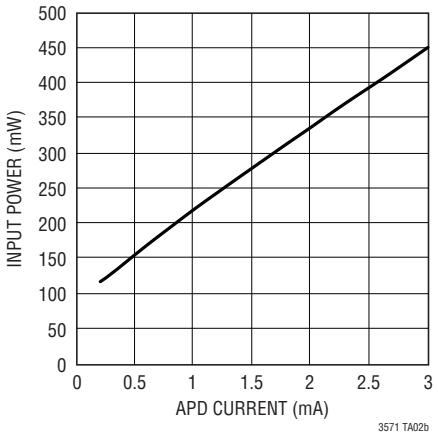
TYPICAL APPLICATIONS

5V to 45V APD Bias Power Supply



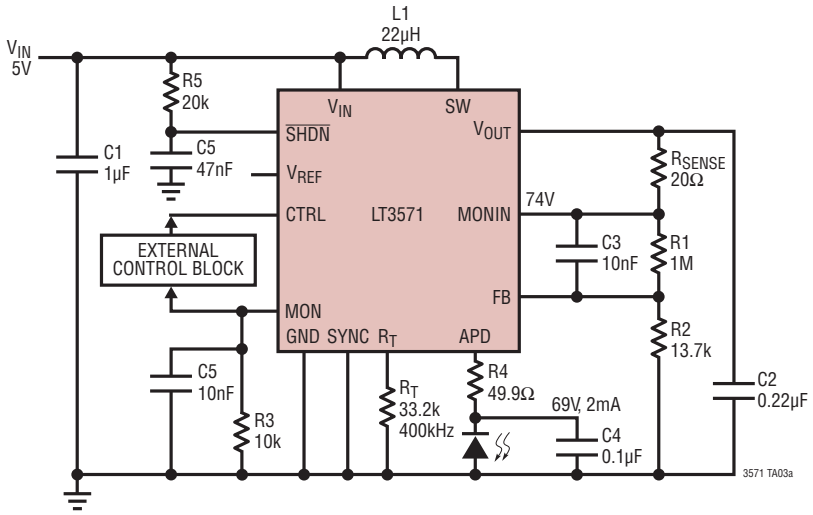
L: TDK VLF3010AT – 100MR49
C1: TDK X7R C1608X7R1C105KT
C2, C4: MURATA X7R GRM188R72A104KA35
C3: AVX X7R 06031C103K
C5: MURATA X7R GRM155R71H103K

Input Power vs APD Current



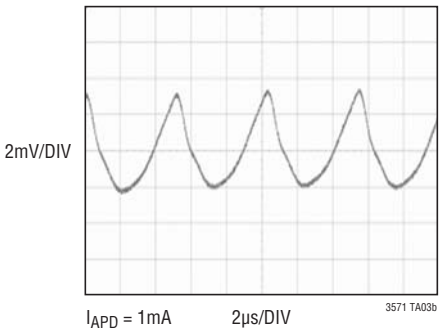
TYPICAL APPLICATIONS

5V to 69V APD Bias Supply with Soft-Start

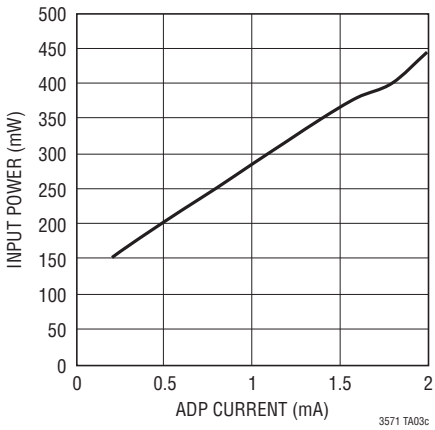


L: TDK VLF4012AT-220MR51
C1: TDK X7R C1608X7R1C105KT
C2: MURATA X7R GRM21AR72A224KAC5L
C3: AVX X7R 06031C103K
C4: MURATA X7R GRM188R72A104KA35
C5: MURATA X7R GRM155R7H103K
C6: MURATA X7R GCM155R471C473K

APD Bias Ripple

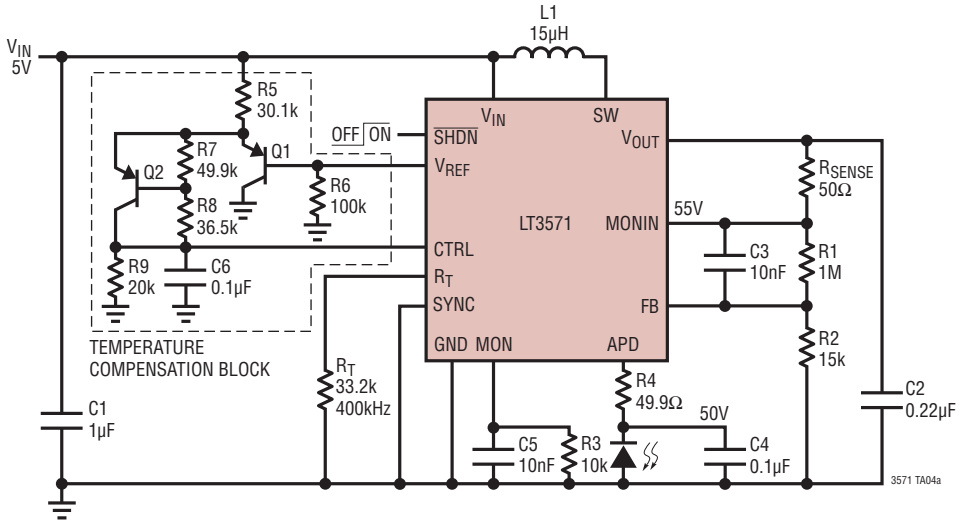


Input Power vs APD Current



TYPICAL APPLICATIONS

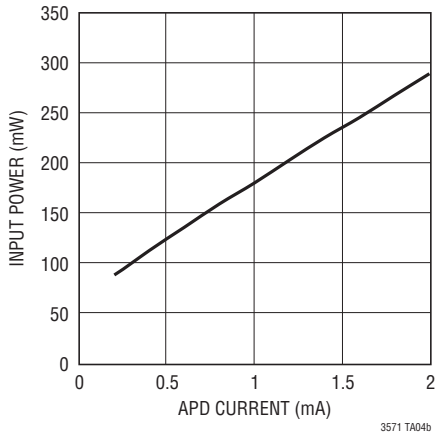
5V to 50V APD Bias Power Supply with Temperature Compensation



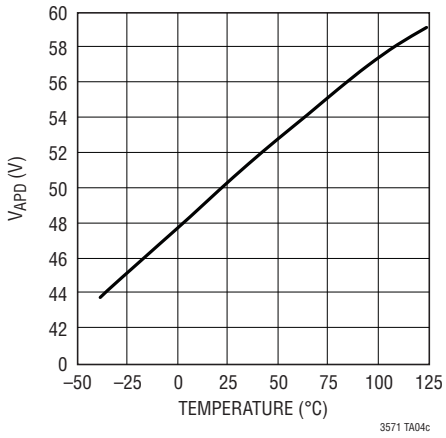
L1: TDK VLF4012AT – 150MR63
C1: TDK X7R C1608X7R1C105KT
C2: MURATA X7R GRM21AR72A224KAC5L
C3: AVX X7R 06031C103K
C4: MURATA X7R GRM188R72A104KA35
C5: MURATA X7R GRM155R71H103K
C6: MURATA X7R GRM155R71A104KA01D

Q1, Q2 = PHILIPS PEMT1

Input Power vs APD Current

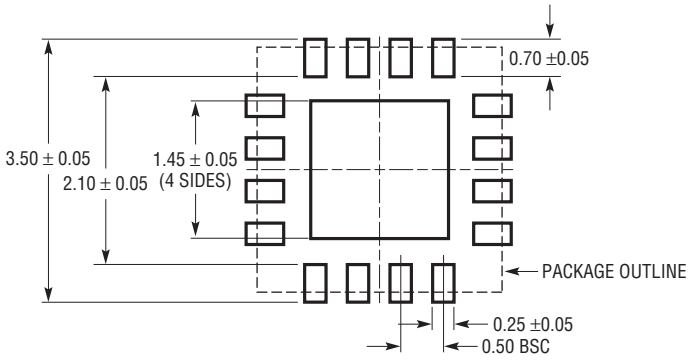


Temperature Response

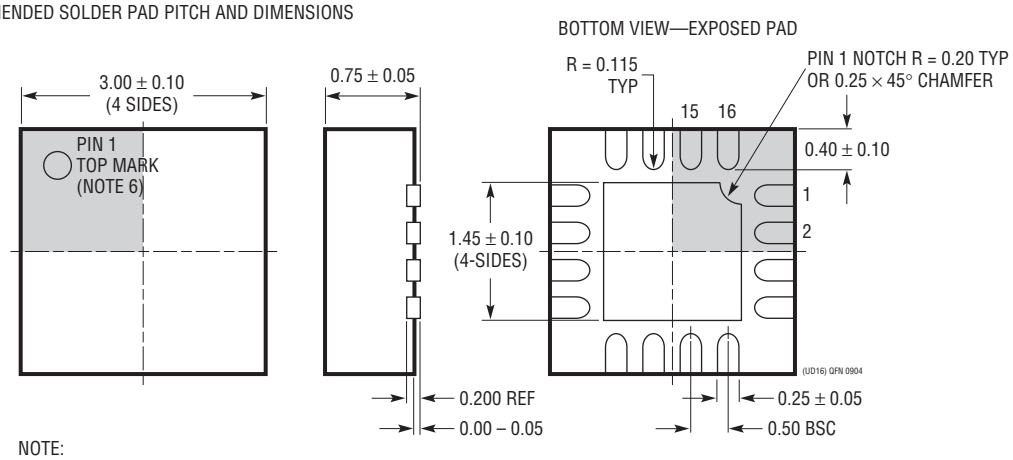


PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



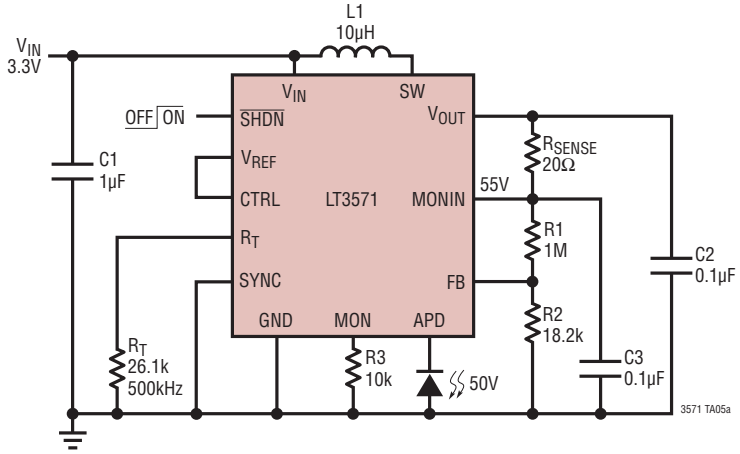
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

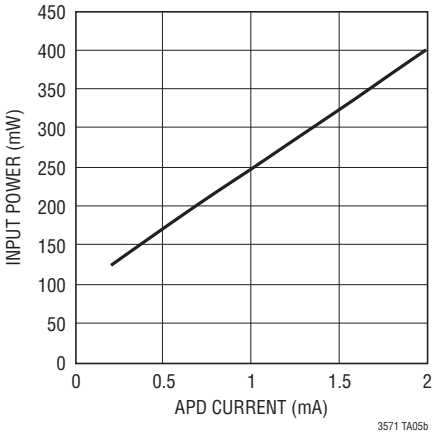
TYPICAL APPLICATIONS

3.3V to 50V APD Bias Power Supply

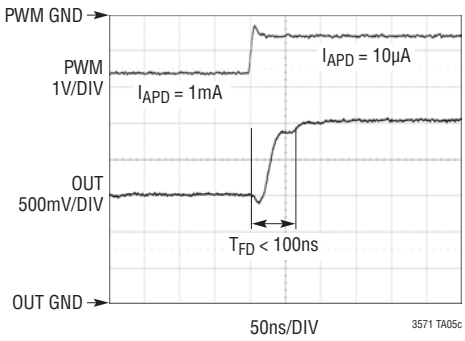


L1: TDK VLF3010AT-100MR49
C1: MURATA X7R GRM21BR71C105KA01B
C2, C3: MURATA X7R GRM188R72A104KA35

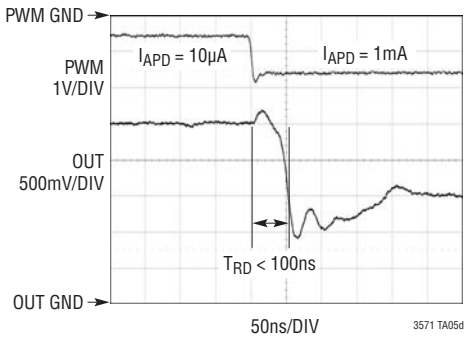
Input Power vs APD Current



Transient Response on Input Signal Falling Edge (1mA to 10µA)



Transient Response on Input Signal Falling Edge (10µA to 1mA)



FOR TRANSIENT RESPONSE, PLEASE REFER TO FIGURE 4

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1930/LT1930A	1A(I_{SW}), 1.2MHz/2.2MHz High Efficiency Step-Up DC/DC Converters	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} <1µA, ThinSOT™ Package
LT3460/LT3460-1	0.3A (I_{SW}), 1.3MHz, 650kHz High Efficiency Step-Up DC/DC Converters	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 2mA, I_{SD} <1µA, SC70 and ThinSOT Packages
LT3461/LT3461A	0.3A (I_{SW}), 1.3MHz/3MHz High Efficiency Step-Up DC/DC Converters with Integrated Schottky	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 2.8mA, I_{SD} <1µA, ThinSOT Package
LT3482	0.3A (I_{SW}), 650k/1.1MHz Step-Up DC/DC Converter with APD Current Monitor	V_{IN}: 2.5V to 16V, $V_{OUT1(MAX)}$ = 48V, $V_{OUT2(MAX)}$ = 90V, I_Q = 3.3mA, I_{SD} <1µA, 3mm × 3mm QFN Package

ThinSOT is a trademark of Linear Technology Corporation.

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