40V_{IN}, 75V_{OUT} LED Controllers

FEATURES

- **3000:1 True Color PWM™ Dimming**
- **Wide Input Voltage Range: 4.5V to 40V**
- **Output Voltage Up to 75V**
- **Constant-Current and Constant-Voltage Regulation**
- 100mV High Side Current Sense
- Drives LEDs in Boost, Buck Mode, Buck-Boost Mode, SEPIC or Flyback Topology
- Adjustable Frequency: 100kHz to 1MHz
- Open LED Protection
- Programmable Undervoltage Lockout with Hysteresis
- Improved Open LED Status Pin (LT3755-2)
- Frequency Synchronization (LT3755-1)
- PWM Disconnect Switch Driver
- CTRL Pin Provides Analog Dimming
- Low Shutdown Current: <1µA
- Programmable Soft-Start
- Thermally Enhanced 16-Lead QFN (3mm × 3mm) and MSOP Packages

APPLICATIONS

- High Power LED
- Battery Chargers
- Accurate Current Limited Voltage Regulators

DESCRIPTION

The LT®3755, LT3755-1 and LT3755-2 are DC/DC controllers designed to operate as a constant-current source for driving high current LEDs. They drive a low side external N-channel power MOSFET from an internal regulated 7.15V supply. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. A ground referenced voltage FB pin serves as the input for several LED protection features, and also makes it possible for the converter to operate as a constant-voltage source. A frequency adjust pin allows the user to program the frequency from 100kHz to 1MHz to optimize efficiency, performance or external component size.

The LT3755/LT3755-1/LT3755-2 sense output current at the high side of the LED string. High side current sensing is the most flexible scheme for driving LEDs, allowing boost, buck mode or buck-boost mode configuration. The PWM input provides LED dimming ratios of up to 3000:1, and the CTRL input provides additional analog dimming capability.

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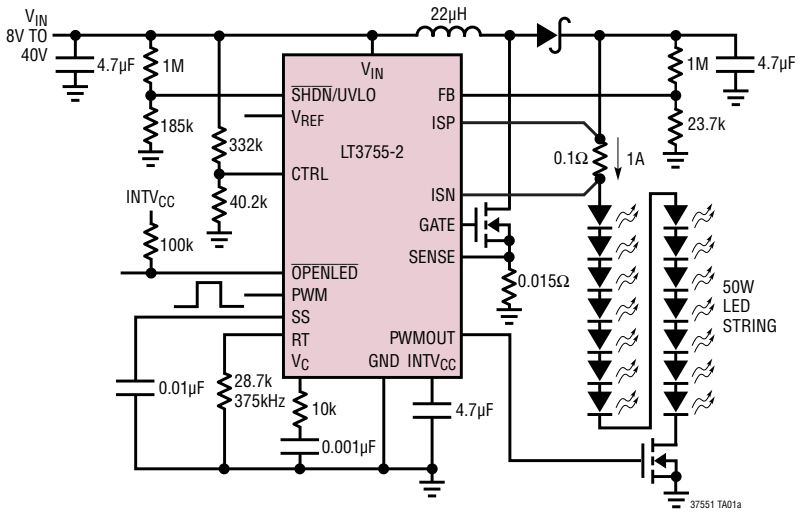
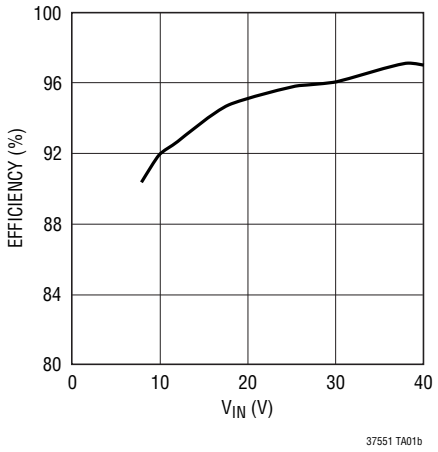
Protected by U.S. Patents including 7199560, 7321203.

TYPICAL APPLICATION

50W White Automotive LED Headlamp Driver



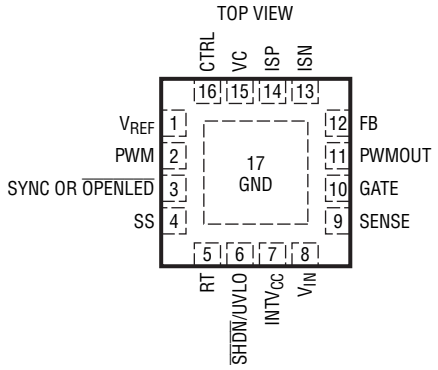
Efficiency vs V_{IN}



ABSOLUTE MAXIMUM RATINGS (Note 1)

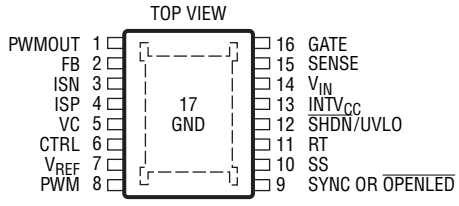
V_{IN} 40V
$\overline{SHDN}$/UVLO (Note 3) 40V
ISP, ISN 75V
$INTV_{CC}$ ..... V_{IN} + 0.3V, 8V
GATE, PWMOUT (Note 4) ..... $INTV_{CC}$ + 0.3V
CTRL, PWM, $\overline{OPENLED}$ 12V
V_C, V_{REF}, SS, FB 3V
SYNC 8V
RT 1.5V
SENSE 0.5V
Operating Junction Temperature Range (Notes 2, 5)
LT3755E/LT3755I ..... –40°C to 125°C
LT3755H ..... –40°C TO 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C (E, I GRADES), T_{JMAX} = 150°C (H GRADE), θ_{JA} = 43°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3755EUD#PBF	LT3755EUD#TRPBF	LDGC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755IUD#PBF	LT3755IUD#TRPBF	LDGC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755EUD-1#PBF	LT3755EUD-1#TRPBF	LDMS	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755IUD-1#PBF	LT3755IUD-1#TRPBF	LDMS	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755EUD-2#PBF	LT3755EUD-2#TRPBF	LFJZ	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755IUD-2#PBF	LT3755IUD-2#TRPBF	LFJZ	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3755EMSE#PBF	LT3755EMSE#TRPBF	3755	16-Lead Plastic MSOP	–40°C to 125°C
LT3755IMSE#PBF	LT3755IMSE#TRPBF	3755	16-Lead Plastic MSOP	–40°C to 125°C
LT3755EMSE-1#PBF	LT3755EMSE-1#TRPBF	37551	16-Lead Plastic MSOP	–40°C to 125°C
LT3755IMSE-1#PBF	LT3755IMSE-1#TRPBF	37551	16-Lead Plastic MSOP	–40°C to 125°C
LT3755EMSE-2#PBF	LT3755EMSE-2#TRPBF	37552	16-Lead Plastic MSOP	–40°C to 125°C
LT3755IMSE-2#PBF	LT3755IMSE-2#TRPBF	37552	16-Lead Plastic MSOP	–40°C to 125°C
LT3755HMSE-2#PBF	LT3755HMSE-2#TRPBF	37552	16-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, $\overline{SHDN}$/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Minimum Operating Voltage	V_{IN} Tied to $INTV_{CC}$	●			4.5	V
V_{IN} Shutdown I_Q	$\overline{SHDN}$/UVLO = 0V, PWM = 0V $\overline{SHDN}$/UVLO = 1.15V, PWM = 0V			0.1	1 5	µA µA
V_{IN} Operating I_Q (Not Switching)	PWM = 0V			1.4	1.7	mA
V_{REF} Voltage	100µA ≤ I_{VREF} ≤ 0µA	●	1.965	2.00	2.045	V
V_{REF} Line Regulation	4.5V ≤ V_{IN} ≤ 40V			0.006		%/V
SENSE Current Limit Threshold		●	98	108	118	mV
SENSE Input Bias Current	Current Out of Pin			40		µA
SS Pull-Up Current	Current Out of Pin		8	10	13	µA
Error Amplifier						
ISP/ISN Full-Scale Current Sense Threshold	FB = 0V, ISP = 48V	●	96	100	103	mV
ISP/ISN Full-Scale Current Sense Threshold at CTRL = 0V	CTRL = 0V, FB = 0V, ISP = 48V		–12	–9.5	–7	mV
CTRL Pin Range for Current Sense Threshold Adjustment		●	0		1.1	V
CTRL Input Bias Current	Current Out of Pin			50	100	nA
LED Current Sense Amplifier Input Common Mode Range (V_{ISN})		●	2.9		75	V
ISP/ISN Short-Circuit Threshold	ISN = 0V		115	150	200	mV
ISP/ISN Short-Circuit Fault Sensing Common Mode Range (V_{ISN})		●	0		3	V
ISP/ISN Input Bias Current (Combined)	PWM = 5V (Active), ISP = ISN = 48V PWM = 0V (Standby), ISP = ISN = 48V			55 0	 0.1	µA µA
LED Current Sense Amplifier g_m	$V_{(ISP-ISN)}$ = 100mV			120		µS
VC Output Impedance	1V < VC < 2V			15000		kΩ
VC Standby Input Bias Current	PWM = 0V		–20		20	nA
FB Regulation Voltage (V_{FB})	 ISP = ISN	 ●	1.232 1.220	1.250 1.250	1.265 1.270	V V
FB Amplifier g_m	FB = V_{FB}, ISP = ISN			480		µS
FB Pin Input Bias Current	Current Out of Pin			40	100	nA
FB Open LED Threshold	$\overline{OPENLED}$ Falling (LT3755 and LT3755-2)		V_{FB} – 65mV	V_{FB} – 50mV	V_{FB} – 40mV	V
FB Overvoltage Threshold	PWMOUT Falling		V_{FB} + 50mV	V_{FB} + 60mV	V_{FB} + 75mV	V
VC Current Mode Gain – ($\Delta V_{VC}/\Delta V_{SENSE}$)				4		V/V
Oscillator						
Switching Frequency	R_T = 100k R_T = 10k	●	90 925	100 1000	125 1050	kHz kHz
Minimum Off-Time				170		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, $\overline{SHDN}$/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Linear Regulator						
$INTV_{CC}$ Regulation Voltage			7	7.15	7.3	V
Dropout (V_{IN} – $INTV_{CC}$)	I_{INTVCC} = –10mA, V_{IN} = 7V			350		mV
$INTV_{CC}$ Undervoltage Lockout			3.9	4.1	4.3	V
$INTV_{CC}$ Current Limit			29	34	40	mA
$INTV_{CC}$ Current in Shutdown	$\overline{SHDN}$/UVLO = 0V, $INTV_{CC}$ = 7V			8	12	µA
Logic Inputs/Outputs						
PWM Input High Voltage		●	1.5			V
PWM Input Low Voltage		●			0.4	V
PWM Pin Resistance to GND			45	60		kΩ
PWMOUT Output Low (V_{OL})				0	50	mV
PWMOUT Output High (V_{OH})			$INTV_{CC}$ – 0.05			V
$\overline{SHDN}$/UVLO Threshold Voltage Falling	E-, I-Grades H-Grade	● ●	1.185 1.175	1.220	1.245 1.245	V V
$\overline{SHDN}$/UVLO Rising Hysteresis				20		mV
$\overline{SHDN}$/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
$\overline{SHDN}$/UVLO Pin Bias Current Low	$\overline{SHDN}$/UVLO = 1.15V		1.7	2.05	2.5	µA
$\overline{SHDN}$/UVLO Pin Bias Current High	$\overline{SHDN}$/UVLO = 1.30V			10	100	nA
$\overline{OPENLED}$ Output Low (V_{OL})	$I_{\overline{OPENLED}}$ = 0.5mA (LT3755 and LT3755-2)				200	mV
SYNC Pin Resistance to GND	LT3755-1 Only			30		kΩ
SYNC Input High	LT3755-1 Only		1.5			V
SYNC Input Low	LT3755-1 Only				0.4	V
Gate Driver						
t_r GATE Driver Output Rise Time	C_L = 3300pF			35		ns
t_f GATE Driver Output Fall Time	C_L = 3300pF			35		ns
GATE Output Low (V_{OL})					0.05	V
GATE Output High (V_{OH})			$INTV_{CC}$ – 0.05			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3755E, LT3755E-1 and LT3755E-2 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3755I, LT3755I-1 and LT3755I-2 are guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LT3755H-2 is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: For V_{IN} below 6V, the $\overline{SHDN}$/UVLO pin must not exceed V_{IN} for proper operation.

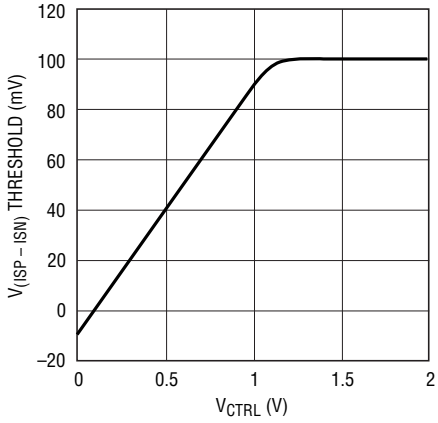
Note 4: GATE and PWMOUT pins are driven either to GND or $INTV_{CC}$ by internal switches. Do not connect these pins externally to a power supply.

Note 5: The LT3755 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

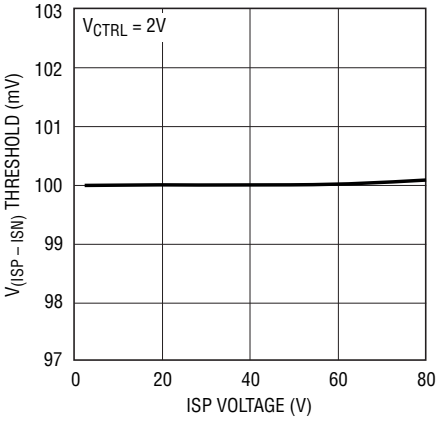
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

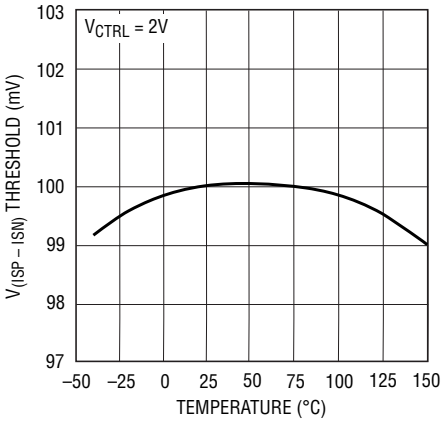
$V_{(ISP – ISN)}$ Threshold vs V_{CTRL}



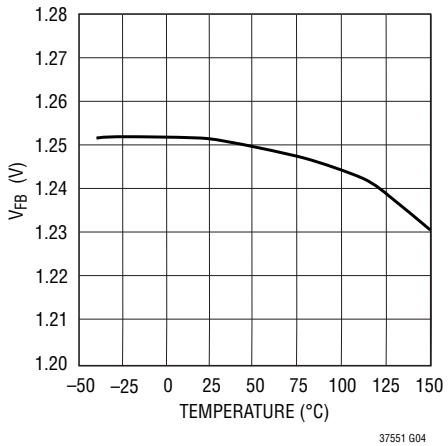
$V_{(ISP – ISN)}$ Threshold vs V_{ISP}



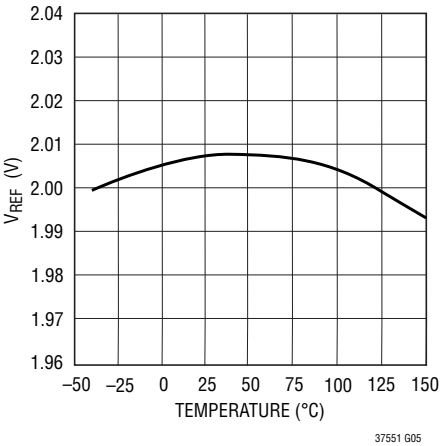
$V_{(ISP – ISN)}$ Threshold vs Temperature



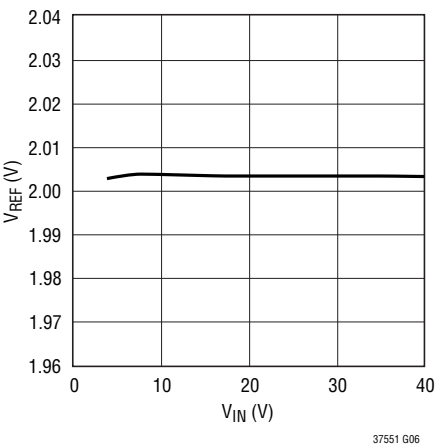
FB Regulation Voltage vs Temperature



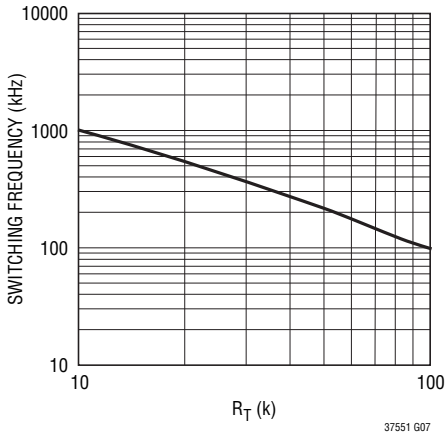
V_{REF} Voltage vs Temperature



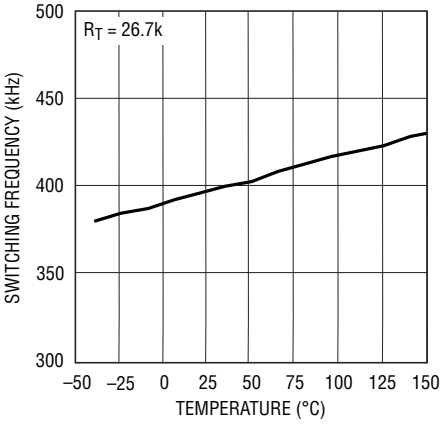
V_{REF} Voltage vs V_{IN}



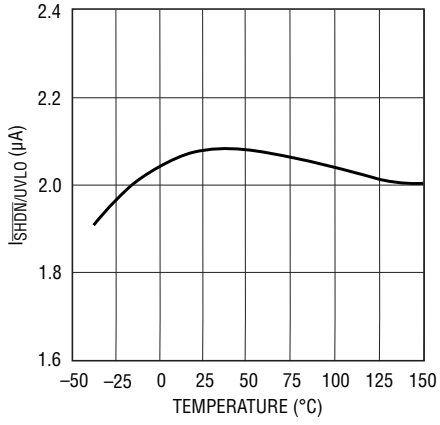
Switching Frequency vs R_T



Switching Frequency vs Temperature



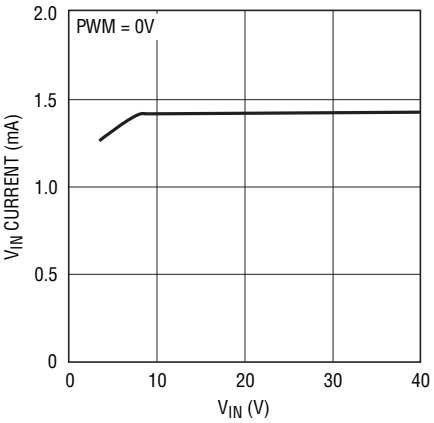
$\overline{SHDN}$/UVLO Hysteresis Current vs Temperature



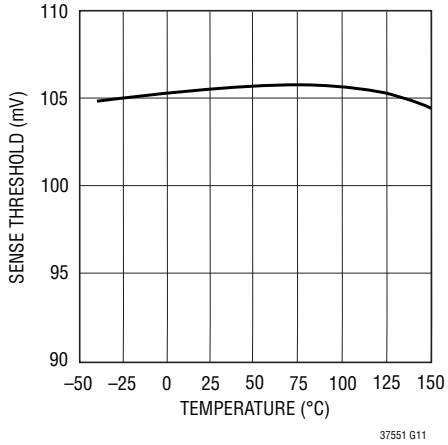
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

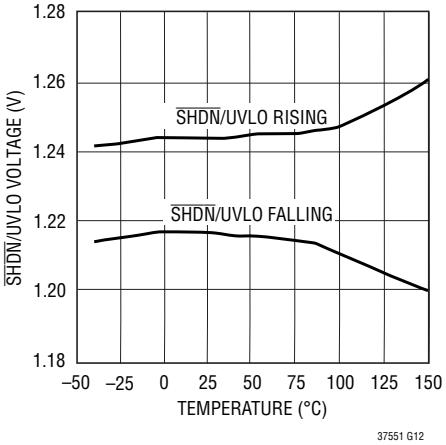
Quiescent Current vs V_{IN}



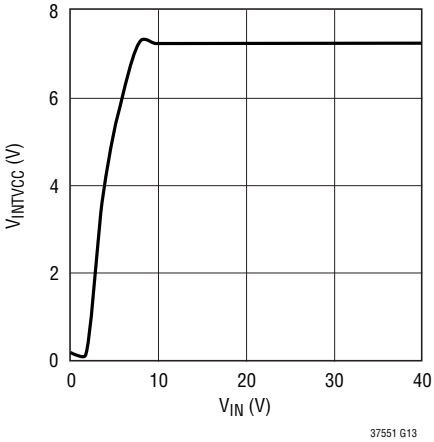
SENSE Current Limit Threshold vs Temperature



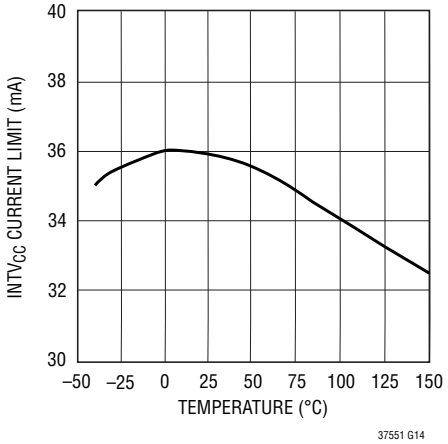
$\overline{SHDN}$/UVLO Threshold vs Temperature



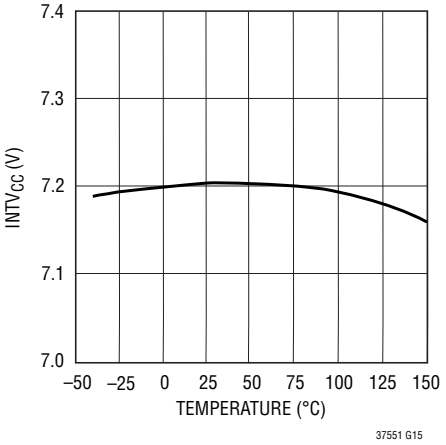
$INTV_{CC}$ Voltage vs V_{IN}



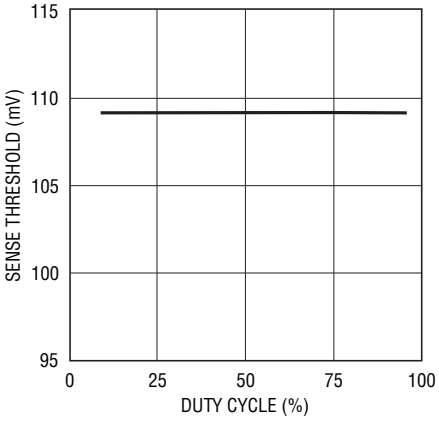
$INTV_{CC}$ Current Limit vs Temperature



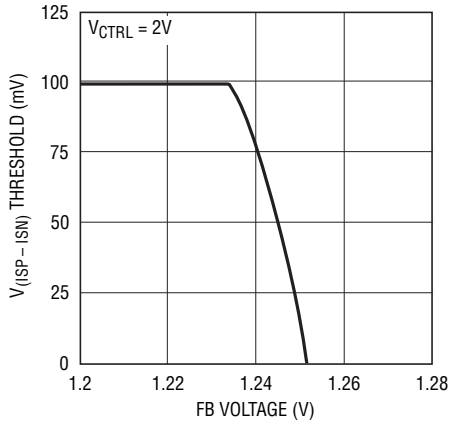
$INTV_{CC}$ Voltage vs Temperature



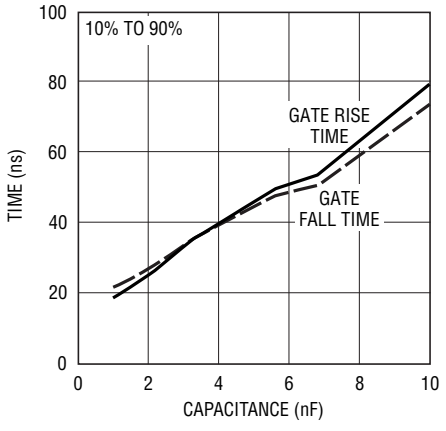
SENSE Current Limit Threshold vs Duty Cycle



$V_{(ISP-ISN)}$ Threshold vs FB Voltage

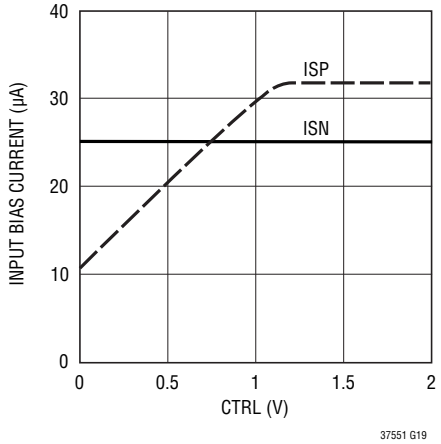


Gate Rise/Fall Time vs Capacitance

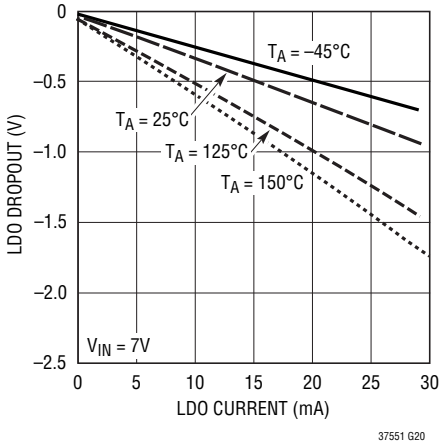


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

ISP/ISN Input Bias Current vs CTRL Voltage



$INTV_{CC}$ Dropout Voltage vs Current, Temperature



PIN FUNCTIONS (MSOP/QFN)

PWMOUT (Pin 1/Pin 11): Buffered Version of PWM Signal for Driving LED Load Disconnect NMOS or Level Shift. This pin also serves in a protection function for the FB overvoltage condition—will toggle if the FB input is greater than the FB regulation voltage (V_{FB}) plus 60mV (typical). The PWMOUT pin is driven from $INTV_{CC}$. Use of a FET with gate cut-off voltage higher than 1V is recommended.

FB (Pin 2/Pin 12): Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation or for LED protection/open LED detection. The internal transconductance amplifier with output VC will regulate FB to 1.25V (nominal) through the DC/DC converter. If the FB input is regulating the loop, the $\overline{OPENLED}$ pull-down is asserted. This action may signal an open LED fault. If FB is driven above the FB threshold (by an external power supply spike, for example), the $\overline{OPENLED}$ pull-down will be de-asserted and the PWMOUT pin will be driven low to protect the LEDs from an overcurrent event. Do not leave the FB pin open. If not used, connect to GND.

ISN (Pin 3/Pin 13): Connection Point for the Negative Terminal of the Current Feedback Resistor. If ISN is greater than 2.9V, the LED current can be programmed by I_{LED} = 100mV/R_{LED} when V_{CTRL} > 1.2V or I_{LED} = (V_{CTRL} – 100mV)/(10 • R_{LED}) when $V_{CTRL} \leq$ 1V. Input bias current is typically 25µA. Below 3V, ISN is an input to the short-circuit protection feature that forces GATE to 0V if ISP exceeds ISN by more than 150mV (typ).

ISP (Pin 4/Pin 14): Connection Point for the Positive Terminal of the Current Feedback Resistor. Input bias current is dependent upon CTRL pin voltage as shown in the TPC. ISP is an input to the short-circuit protection feature when ISN is less than 3V.

VC (Pin 5/Pin 15): Transconductance Error Amplifier Output Pin Used to Stabilize the Voltage Loop with an RC Network. This pin is high impedance when PWM is low, a feature that stores the demand current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response.

PIN FUNCTIONS (MSOP/QFN)

CTRL (Pin 6/Pin 16): Current Sense Threshold Adjustment Pin. Regulating threshold $V_{(ISP-ISN)}$ is 1/10th V_{CTRL} plus an offset for 0V < V_{CTRL} < 1V. For V_{CTRL} > 1.2V the current sense threshold is constant at the full-scale value of 100mV. For 1V < V_{CTRL} < 1.2V, the dependence of current sense threshold upon V_{CTRL} transitions from a linear function to a constant value, reaching 98% of full-scale value by V_{CTRL} = 1.1V. Do not leave this pin open.

V_{REF} (Pin 7/Pin 1): Voltage Reference Output Pin, Typically 2V. This pin drives a resistor divider for the CTRL pin, either for analog dimming or for temperature limit/compensation of LED load. Can supply up to 100µA.

PWM (Pin 8/Pin 2): A signal low turns off switcher, idles oscillator and disconnects VC pin from all internal loads. PWMOUT pin follows PWM pin. PWM has an internal pull-down resistor. If not used, connect to $INTV_{CC}$.

$\overline{OPENLED}$ (Pin 9/Pin 3, LT3755 and LT3755-2): An open-collector pull-down on $\overline{OPENLED}$ asserts if the FB input is greater than the FB regulation threshold minus 50mV (typical). To function, the pin requires an external pull-up current less than 1mA. When the PWM input is low and the DC/DC converter is idle, the $\overline{OPENLED}$ condition is latched to the last valid state when the PWM input was high. When PWM input goes high again, the $\overline{OPENLED}$ pin will be updated. This pin may be used to report an open LED fault.

SYNC (Pin 9/Pin 3, LT3755-1 Only): The SYNC pin is used to synchronize the internal oscillator to an external logic level signal. The R_T resistor should be chosen to program an internal switching frequency 20% slower than the SYNC pulse frequency. Gate turn-on occurs a fixed delay after the rising edge of SYNC. For best PWM performance, the PWM rising edge should occur at least 200ns before the SYNC rising edge. Use a 50% duty cycle waveform to drive this pin. This pin replaces $\overline{OPENLED}$ on LT3755-1 option parts. If not used, tie this pin to GND.

SS (Pin 10/Pin 4): Soft-Start Pin. This pin modulates oscillator frequency and compensation pin voltage (VC) clamp. The soft-start interval is set with an external capacitor. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to GND by an undervoltage condition (detected by $\overline{SHDN}$/UVLO pin) or thermal limit.

RT (Pin 11/Pin 5): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND (for resistor values, see the Typical Performance curve or Table 1). Do not leave the RT pin open.

$\overline{SHDN}$/UVLO (Pin 12/Pin 6): Shutdown and Undervoltage Detect Pin. An accurate 1.22V falling threshold with externally programmable hysteresis detects when power is OK to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2.1µA pull-down current. Above the threshold (but below 6V), $\overline{SHDN}$/UVLO input bias current is sub-µA. Below the falling threshold, a 2.1µA pull-down current is enabled so the user can define the hysteresis with the external resistor selection. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

$INTV_{CC}$ (Pin 13/Pin 7): Regulated Supply for Internal Loads, GATE Driver and PWMOUT Driver. Supplied from V_{IN} and regulates to 7.15V (typical). $INTV_{CC}$ must be bypassed with a 4.7µF capacitor placed close to the pin. Connect $INTV_{CC}$ directly to V_{IN} if V_{IN} is always less than or equal to 8V.

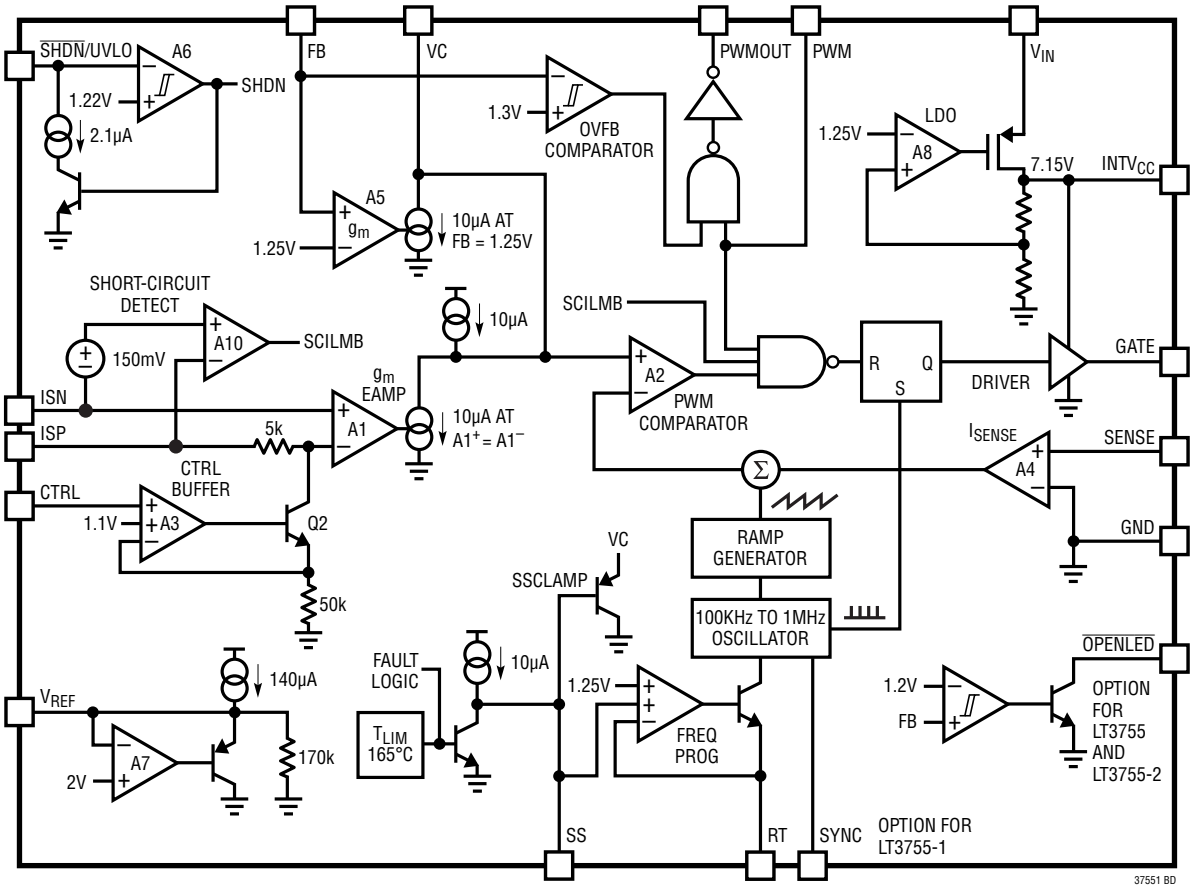
V_{IN} (Pin 14/Pin 8): Input Supply Pin. Must be locally bypassed with a 0.22µF (or larger) capacitor placed close to the IC.

SENSE (Pin 15/Pin 9): The current sense input for the control loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor, R_{SENSE}, in the source of the NFET. The negative terminal of the current sense resistor should be Kelvin connected to the GND plane of the IC.

GATE (Pin 16/Pin 10): N-channel FET Gate Driver Output. Switches between $INTV_{CC}$ and GND. Driven to GND during shutdown, fault or idle states.

Exposed Pad (Pin 17/Pin 17): Ground. This pin also serves as current sense input for control loop, sensing negative terminal of current sense resistor. Solder the Exposed Pad directly to ground plane.

BLOCK DIAGRAM



OPERATION

The LT3755 is a constant-frequency, current mode controller with a low side NMOS gate driver. The GATE pin and PWMOUT pin drivers and other chip loads are powered from $INTV_{CC}$, which is an internally regulated supply. In the discussion that follows it will be helpful to refer to the Block Diagram of the IC. In normal operation with the PWM pin low, the GATE and PWMOUT pins are driven to GND, the VC pin is high impedance to store the previous switching state on the external compensation capacitor, and the ISP and ISN pin bias currents are reduced to leakage levels. When the PWM pin transitions high, the PWMOUT pin transitions high after a short delay. At the same time, the internal oscillator wakes up and generates a pulse to set the PWM latch, turning on the external power MOSFET switch (GATE goes high). A voltage input proportional to the switch current, sensed by an external current sense resistor between the SENSE and GND input pins, is added to a stabilizing slope compensation ramp and the resulting "switch current sense" signal is fed into the positive terminal of the PWM comparator. The current in the external inductor increases steadily during the time the switch is on. When the switch current sense voltage exceeds the output of the error amplifier, labeled "VC", the latch is reset and the switch is turned off. During the switch-off phase, the inductor current decreases. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator.

Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current or voltage in the load. The VC signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin. In this manner, the error amplifier sets the correct peak switch current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. The switch current is monitored during the on-phase and the voltage across the SENSE pin is not allowed to exceed the current limit threshold of 108mV (typical). If the SENSE pin exceeds the current limit threshold, the SR latch is reset regardless of the output state of the PWM comparator. Likewise, at an ISP/ISN common mode voltage less than 3V, the difference between ISP and ISN is monitored to determine if the output is in a short-circuit condition. If the difference between ISP and ISN is greater than 150mV (typical), the SR latch will be reset regardless of the PWM comparator. These functions are intended to protect the power switch as well as various external components in the power path of the DC/DC converter.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the VC pin is set by the amplified difference of the internal reference of 1.25V (nominal) and the FB pin. If FB is lower than the reference voltage, the switch current will increase; if FB is higher than the reference voltage, the switch demand current will decrease. The LED current sense feedback interacts with the FB voltage feedback so that FB will not exceed the internal reference and the voltage between ISP and ISN will not exceed the threshold set by the CTRL pin. For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions the appropriate loop is dominant. To deactivate the voltage loop entirely, FB can be connected to GND. To deactivate the LED current loop entirely, the ISP and ISN should be tied together and the CTRL input tied to V_{REF}.

Two LED specific functions featured on the LT3755 are controlled by the voltage feedback pin. First, when the FB pin exceeds a voltage 50mV lower (–4%) than the FB regulation voltage, the pull-down driver on the $\overline{\text{OPENLED}}$ pin is activated (LT3755 and LT3755-2 only). This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. When the FB pin exceeds the FB regulation voltage by 60mV (5% typical), the PWMOUT pin is driven low, ignoring the state of the PWM input. In the case where the PWMOUT pin drives a disconnect NFET, this action isolates the LED load from GND preventing excessive current from damaging the LEDs. If the FB input exceeds both the open LED and the overvoltage thresholds, then an externally driven overvoltage event has caused the FB pin to be too high and the $\overline{\text{OPENLED}}$ pull-down will be de-asserted. The LT3755-2 will re-assert the $\overline{\text{OPENLED}}$ signal when FB falls below the overvoltage threshold and remains above the OPENLED threshold. The LT3755 is prevented from re-asserting $\overline{\text{OPENLED}}$ until FB drops below both thresholds.

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$INTV_{CC}$ Regulator Bypassing and Operation

The $INTV_{CC}$ pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R ceramic capacitor for best performance. A 4.7µF capacitor will be adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the $INTV_{CC}$ pin and also to the IC ground.

An internal current limit on the $INTV_{CC}$ output protects the LT3755 from excessive on-chip power dissipation. The minimum value of this current should be considered when choosing the switching NMOS and the operating frequency.

I_{INTVCC} can be calculated from the following equation:

$$I_{INTVCC} = Q_G \bullet f_{OSC}$$

Careful choice of a lower Q_G FET will allow higher switching frequencies, leading to smaller magnetics. The $INTV_{CC}$ pin has its own undervoltage disable (UVLO) set to 4.1V (typical) to protect the external FETs from excessive power dissipation caused by not being fully enhanced. If the $INTV_{CC}$ pin drops below the UVLO threshold, the GATE and PWMOUT pins will be forced to 0V and the soft-start pin will be reset.

If the input voltage, V_{IN}, will not exceed 8V, then the $INTV_{CC}$ pin could be connected to the input supply. Be aware that a small current (less than 12µA) will load the $INTV_{CC}$ in shutdown. This action allows the LT3755 to operate from V_{IN} as low as 4.5V. If V_{IN} is normally above, but occasionally drops below the $INTV_{CC}$ regulation voltage, then the minimum operating V_{IN} will be close to 6V. This value is determined by the dropout voltage of the linear regulator and the $INTV_{CC}$ undervoltage lockout threshold mentioned above.

Programming the Turn-On and Turn-Off Thresholds with the $\overline{SHDN}$/UVLO Pin

The falling UVLO value can be accurately set by the resistor divider. A small 2.1µA pull-down current is active when $\overline{SHDN}$/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis.

The following equations should be used to determine the values of the resistors:

$$V_{IN,FALLING} = 1.22 \bullet \frac{R1+R2}{R2}$$

$$V_{IN,RISING} = 2.1\mu A \bullet R1 + V_{IN,FALLING}$$

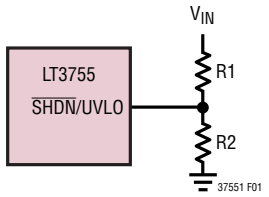

Figure 1. Resistor Connection to Set V_{IN} Undervoltage Shutdown Threshold

LED Current Programming

The LED current is programmed by placing an appropriate value current sense resistor, R_{LED}, in series with the LED string. The voltage drop across R_{LED} is (Kelvin) sensed by the ISP and ISN pins. Typically, sensing of the current should be done at the top of the LED string. If this option is not available, then the current may be sensed at the bottom of the string, but take caution that the minimum ISN value does not fall below 3V, which is the lower limit of the LED current regulation function. The CTRL pin should be tied to a voltage higher than 1.2V to get the full-scale 100mV (typical) threshold across the sense resistor. The CTRL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the CTRL pin voltage is less than 1V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 100mV}{R_{LED} \bullet 10}$$

When the CTRL pin voltage is between 1V and 1.2V the LED current varies with CTRL, but departs from the equation above by an increasing amount as CTRL voltage increases. Ultimately, above CTRL = 1.2V the LED current no longer varies with CTRL. At CTRL = 1.1V, the actual value of I_{LED} is ~98% of the equation's estimate.

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When V_{CTRL} is higher than 1.2V, the LED current is regulated to:

$$I_{LED} = \frac{100mV}{R_{LED}}$$

The LED current programming feature can increase total dimming range by a factor of 10. The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor. Some level of ripple signal is acceptable: the compensation capacitor on the VC pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. Ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause misoperation, but may lead to noticeable offset between the average value and the user-programmed value.

Programming Output Voltage (Constant Voltage Regulation) or Open LED/Overvoltage Threshold

For a boost application, the output voltage can be set by selecting the values of R3 and R4 (see Figure 2) according to the following equation:

$$V_{OUT} = 1.25 \bullet \frac{R3 + R4}{R4}$$

For a boost type LED driver, set the resistor from the output to the FB pin such that the expected V_{FB} during normal operation will not exceed 1.1V. For an LED driver of buck or a buck-boost configuration, the output voltage is typically level-shifted to a signal with respect to GND as illustrated in Figure 3. The output can be expressed as:

$$V_{OUT} = V_{BE} + 1.25 \bullet \frac{R3}{R4}$$

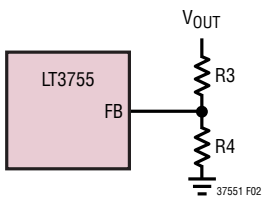

Figure 2. Feedback Resistor Connection for Boost or SEPIC LED Driver

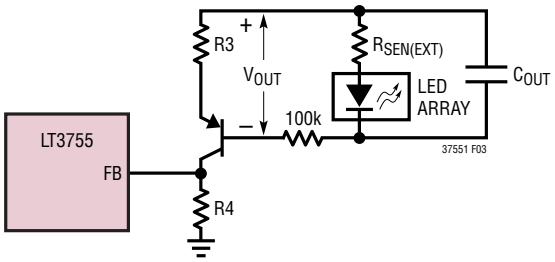

Figure 3. Feedback Resistor Connection for Buck Mode or Buck-Boost Mode LED Driver

ISP/ISN Short-Circuit Protection Feature (for SEPIC)

The ISP and ISN pins have a protection feature independent of the LED current sense feature that operates at ISN below 3V. The purpose of this feature is to provide continuous current sensing when ISN is below the LED current sense common mode range (during start-up or an output short-circuit fault) to prevent the development of excessive switching currents that could damage the power components in a SEPIC converter. The action threshold (150mV, typ) is above the default LED current sense threshold, so that no interference will occur over the ISN voltage range where these two functions overlap. This feature acts in the same manner as SENSE current limit — it prevents GATE from going high (switch turn-on) until the ISP/ISN difference falls below the threshold. If the load has appreciable series inductance, use of a Schottky clamp from GND to ISN is recommended for the SEPIC to prevent excessive current flowing from the ISN pin in a fault.

Dimming Control

There are two methods to control the current source for dimming using the LT3755. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the current source between

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zero and full current to achieve a precisely programmed average current. To make PWM dimming more accurate, the switch demand current is stored on the VC node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch may be used in the LED current path to prevent the ISP node from discharging during the PWM signal low phase. The minimum PWM on or off time is affected by choice of operating frequency and external component selection. The data sheet application titled "Buck Mode 500mA LED Driver for 20kHz PWM Dimming" demonstrates regulated current pulses as short as 1µs are achievable. The best overall combination of PWM and analog dimming capability is available if the minimum PWM pulse is at least six switching cycles.

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate R_T resistor value see Table 1. An external resistor from the RT pin to GND is required—do not leave this pin open.

Table 1. Switching Frequency vs R_T Value

f_{OSC} (kHz)	R_T (kΩ)
1000	10.0
900	11.8
800	13.0
700	15.4
600	17.8
500	21.0
400	26.7
300	35.7
200	53.6
100	100

Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The fixed minimum on-time and minimum off-time (see Figure 4) and the switching frequency define the minimum and maximum duty cycle of the switch, respectively. The following equations express the minimum/maximum duty cycle:

Min Duty Cycle = (minimum on-time) • switching frequency

Max Duty Cycle = 1 – (minimum off-time) • switching frequency

When calculating the operating limits, the typical values for on/off-time in the data sheet should be increased by at least 60ns to allow margin for PWM control latitude, GATE rise/fall times and SW node rise/fall times.

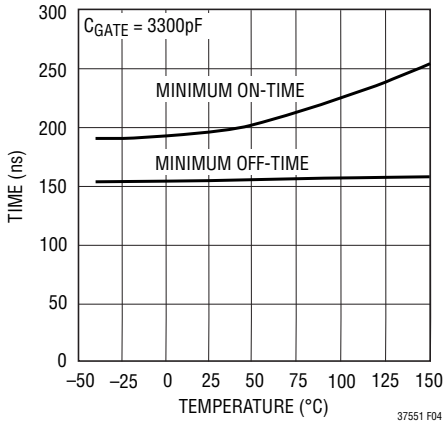

Figure 4. Typical Minimum On and Off Pulse Width vs Temperature

Thermal Considerations

The LT3755 is rated to a maximum input voltage of 40V. Careful attention must be paid to the internal power dissipation of the IC at higher input voltages to ensure that a junction temperature of 125°C (150°C for H-Grade) is not exceeded. This junction limit is especially important

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when operating at high ambient temperatures. The majority of the power dissipation in the IC comes from the supply current needed to drive the gate capacitance of the external power MOSFET. This gate drive current can be calculated as:

$$I_{GATE} = f_{SW} \bullet Q_G$$

A low Q_G power MOSFET should always be used when operating at high input voltages, and the switching frequency should also be chosen carefully to ensure that the IC does not exceed a safe junction temperature. The internal junction temperature of the IC can be estimated by:

$$T_J = T_A + [V_{IN} (I_Q + f_{SW} \bullet Q_G) \bullet \theta_{JA}]$$

where T_A is the ambient temperature, I_Q is the quiescent current of the part (maximum 1.7mA) and θ_{JA} is the package thermal impedance (68°C/W for the 3mm × 3mm QFN package). For example, an application with $T_{A(MAX)}$ = 85°C, $V_{IN(MAX)}$ = 40V, f_{SW} = 400kHz, and having a FET with Q_G = 20nC, the maximum IC junction temperature will be approximately:

$$T_J = 85°C + [40V (1.7mA + 400kHz \bullet 20nC) \bullet 68°C/W] = 111°C$$

The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should then be connected to an internal copper ground plane with thermal vias placed directly under the package to spread out the heat dissipated by the IC.

If LT3755 junction temperature reaches 165°C, the GATE and PWMOUT pins will be driven to GND and the soft-start (SS) pin will be discharged to GND. Switching will be enabled after device temperature is reduced 10°C. This function is intended to protect the device during momentary thermal overload conditions.

Frequency Synchronization (LT3755-1 Only)

The LT3755-1 switching frequency can be synchronized to an external clock using the SYNC pin. For proper operation, the R_T resistor should be chosen for a switching frequency 20% lower than the external clock frequency. The SYNC pin is disabled during the soft-start period.

Observation of the following guidelines about the SYNC waveform will ensure proper operation of this feature. Driving SYNC with a 50% duty cycle waveform is always a good choice, otherwise, maintain the duty cycle between 20% and 60%. When using both PWM and SYNC features, the PWM signal rising edge should occur at least 200ns before the SYNC rising edge (V_{IH}) for optimal PWM performance. If the SYNC pin is not used, it should be connected to GND.

Open LED Detection (LT3755 and LT3755-2)

The LT3755 and LT3755-2 provide an open-drain status pin, $\overline{\text{OPENLED}}$, that pulls low when the FB pin is within ~50mV of its 1.25V regulated voltage. If the open LED clamp voltage is programmed correctly using the FB pin, then the FB pin should never exceed 1.1V when LEDs are connected, therefore, the only way for the FB pin to be within 50mV of the regulation voltage is for an open LED event to have occurred. The key difference between the LT3755 and LT3755-2 is the behavior of the $\overline{\text{OPENLED}}$ pin when the FB pin crosses and re-crosses the FB overvoltage threshold (1.31V typ). The LT3755-2 asserts/de-asserts $\overline{\text{OPENLED}}$ freely when crossing the 1.31V threshold. The LT3755, by comparison, de-asserts $\overline{\text{OPENLED}}$ when FB exceeds 1.31V and is prevented from re-asserting $\overline{\text{OPENLED}}$ until the FB pin falls below the 1.2V (typ) open LED threshold and clears the fault. The LT3755-2 has the more general purpose behavior and is recommended for applications using $\overline{\text{OPENLED}}$.

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter. Assuming that a 100mV input voltage ripple is acceptable, the required capacitor value for a boost converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) \bullet \frac{V_{OUT}}{V_{IN}} \bullet t_{SW}(\mu s) \bullet \left(\frac{\mu F}{A \bullet \mu s} \right)$$

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Therefore, a 10µF capacitor is an appropriate selection for a 400kHz boost regulator with 12V input, 48V output and 1A load.

With the same V_{IN} voltage ripple of 100mV, the input capacitor for a buck converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) \bullet t_{SW}(\mu s) \bullet 4.7 \bullet \left(\frac{\mu F}{A \bullet \mu s}\right)$$

A 10µF input capacitor is an appropriate selection for a 400kHz buck mode converter with a 1A load.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. In this buck converter case it is important to place the capacitor as close as possible to the Schottky diode and to the GND return of the switch (i.e., the sense resistor). It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. The RMS input current for a buck mode LED driver is:

$$I_{IN(RMS)} = I_{LED} \bullet \sqrt{(1-D) \bullet D}$$

where D is the switch duty cycle.

Table 2. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
TDK	www.tdk.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of X7R type ceramic capacitors is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately higher capacitor values.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{2V}{10\mu A}$$

A typical value for the soft-start capacitor is 0.01µF. The soft-start pin reduces the oscillator frequency and the maximum current in the switch. The soft-start capacitor is discharged when $\overline{SHDN}$/UVLO falls below its threshold, during an overtemperature event or during an $INTV_{CC}$ undervoltage event. During start-up with $\overline{SHDN}$/UVLO, charging of the soft-start capacitor is enabled after the first PWM high period.

Power MOSFET Selection

For applications operating at high input or output voltages, the power NMOS FET switch is typically chosen for drain voltage V_{DS} rating and low gate charge Q_G. Consideration of switch on-resistance, $R_{DS(ON)}$, is usually secondary because switching losses dominate power loss. The $INTV_{CC}$ regulator on the LT3755 has a fixed current limit to protect the IC from excessive power dissipation at high V_{IN}, so the FET should be chosen so that the product of Q_G at 7V and switching frequency does not exceed the $INTV_{CC}$ current limit. For driving LEDs be careful to choose a switch with a V_{DS} rating that exceeds the threshold set by the FB pin in case of an open-load fault. Several MOSFET vendors are listed in Table 3. The MOSFETs used in the application circuits in this data sheet have been found to work well with the LT3755. Consult factory applications for other recommended MOSFETs.

Table 3. MOSFET Manufacturers

VENDOR	WEB
Vishay Siliconix	www.vishay.com
Fairchild	www.fairchildsemi.com
International Rectifier	www.irf.com

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Schottky Rectifier Selection

The power Schottky diode conducts current during the interval when the switch is turned off. Select a diode rated for the maximum SW voltage. If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current. Table 4 has some recommended component vendors.

Table 4. Schottky Rectifier Manufacturers

VENDOR	WEB
On Semiconductor	www.onsemi.com
Diodes, Inc.	www.diodes.com
Central Semiconductor	www.centralsemi.com

Sense Resistor Selection

The resistor, R_{SENSE}, between the source of the external NMOS FET and GND should be selected to provide adequate switch current to drive the application without exceeding the 108mV (typical) current limit threshold on the SENSE pin of LT3755. For buck mode applications, select a resistor that gives a switch current at least 30% greater than the required LED current. For buck mode, select a resistor according to:

$$R_{SENSE,BUCK} \leq \frac{0.07V}{I_{LED}}$$

For buck-boost, select a resistor according to:

$$R_{SENSE,BUCK\text{-}BOOST} \leq \frac{V_{IN} \bullet 0.07V}{(V_{IN} + V_{LED})I_{LED}}$$

For boost, select a resistor according to:

$$R_{SENSE,BOOST} \leq \frac{V_{IN} \bullet 0.07V}{V_{LED} \bullet I_{LED}}$$

These equations provide an estimate of the sense resistor value based on reasonable assumptions about inductor current ripple during steady state switching. Lower values of sense resistor may be required in applications where inductor ripple current is higher. Examples include applications with current limited operation at high duty cycle, and those with discontinuous conduction mode (DCM) switching. It is always prudent to verify the peak inductor current in the application to ensure the sense resistor selection provides margin to the SENSE current limit threshold.

The placement of R_{SENSE} should be close to the source of the NMOS FET and GND of the LT3755. The SENSE input to LT3755 should be a Kelvin connection to the positive terminal of R_{SENSE}.

Inductor Selection

The inductor used with the LT3755 should have a saturation current rating appropriate to the maximum switch current selected with the R_{SENSE} resistor. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode ramp on SENSE during the switch on-time of approximately 20mV magnitude. The following equations are useful to estimate the inductor value for continuous conduction mode operation:

$$L_{BUCK} = \frac{R_{SENSE} \bullet V_{LED}(V_{IN} - V_{LED})}{V_{IN} \bullet 0.02V \bullet f_{OSC}}$$

$$L_{BUCK\text{-}BOOST} = \frac{R_{SENSE} \bullet V_{LED} \bullet V_{IN}}{(V_{LED} + V_{IN}) \bullet 0.02V \bullet f_{OSC}}$$

$$L_{BOOST} = \frac{R_{SENSE} \bullet V_{IN}(V_{LED} - V_{IN})}{V_{LED} \bullet 0.02V \bullet f_{OSC}}$$

Table 5 provides some recommended inductor vendors.

Table 5. Inductor Manufacturers

VENDOR	WEB
Sumida	www.sumida.com
Würth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Loop Compensation

The LT3755 uses an internal transconductance error amplifier whose VC output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability.

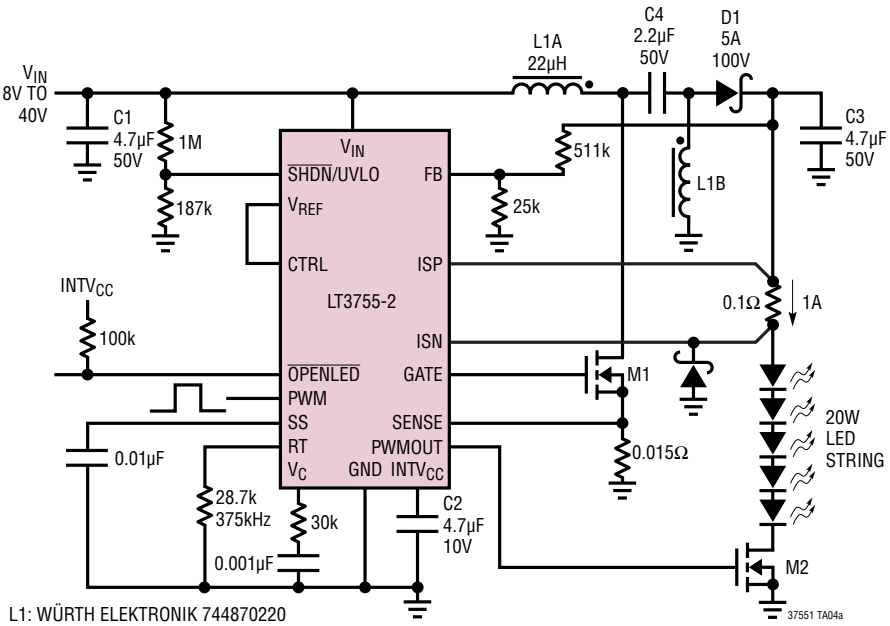
APPLICATIONS INFORMATION

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop response and stability. For typical LED applications, a 2.2nF compensation capacitor at VC is adequate, and a series resistor should always be used to increase the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Board Layout

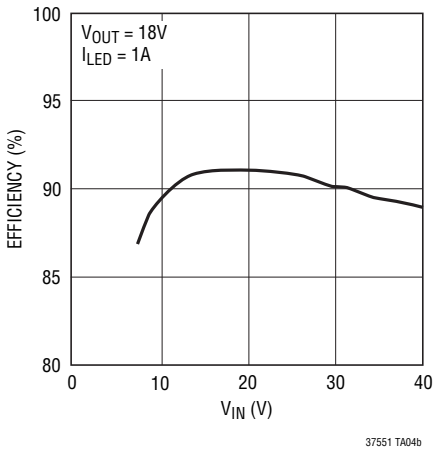
The high speed operation of the LT3755 demands careful attention to board layout and component placement. The exposed pad of the package is the only GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching node between the inductor, switch drain and anode of the Schottky rectifier. Use a ground plane under the switching node to eliminate interplane coupling to sensitive signals. The lengths of the high dI/dt traces: 1) from the switch node through the switch and sense resistor to GND, and 2) from the switch node through the Schottky rectifier and filter capacitor to GND should be minimized. The ground points of these two switching current traces should come to a common point then connect to the ground plane under the LT3755. Likewise, the ground terminal of the bypass capacitor for the $INTV_{CC}$ regulator should be placed near the GND of the switching path. Typically this requirement will result in the external switch being closest to the IC, along with the $INTV_{CC}$ bypass capacitor. The ground for the compensation network and other DC control signals should be star connected to the underside of the IC. Do not extensively route high impedance signals such as FB and VC, as they may pick up switching noise. In particular, avoid routing FB and PWMOUT in parallel for more than a few millimeters on the board. Minimize resistance in series with the SENSE input to avoid changes (most likely reduction) to the switch current limit threshold.

20W SEPIC LED Driver



L1: WÜRTH ELEKTRONIK 744870220
M1: VISHAY SILICONIX SI7454DP
D1: DIODES INC. - PDS5100
M2: VISHAY SILICONIX SI2318DS

Efficiency vs V_{IN}



APPLICATIONS INFORMATION

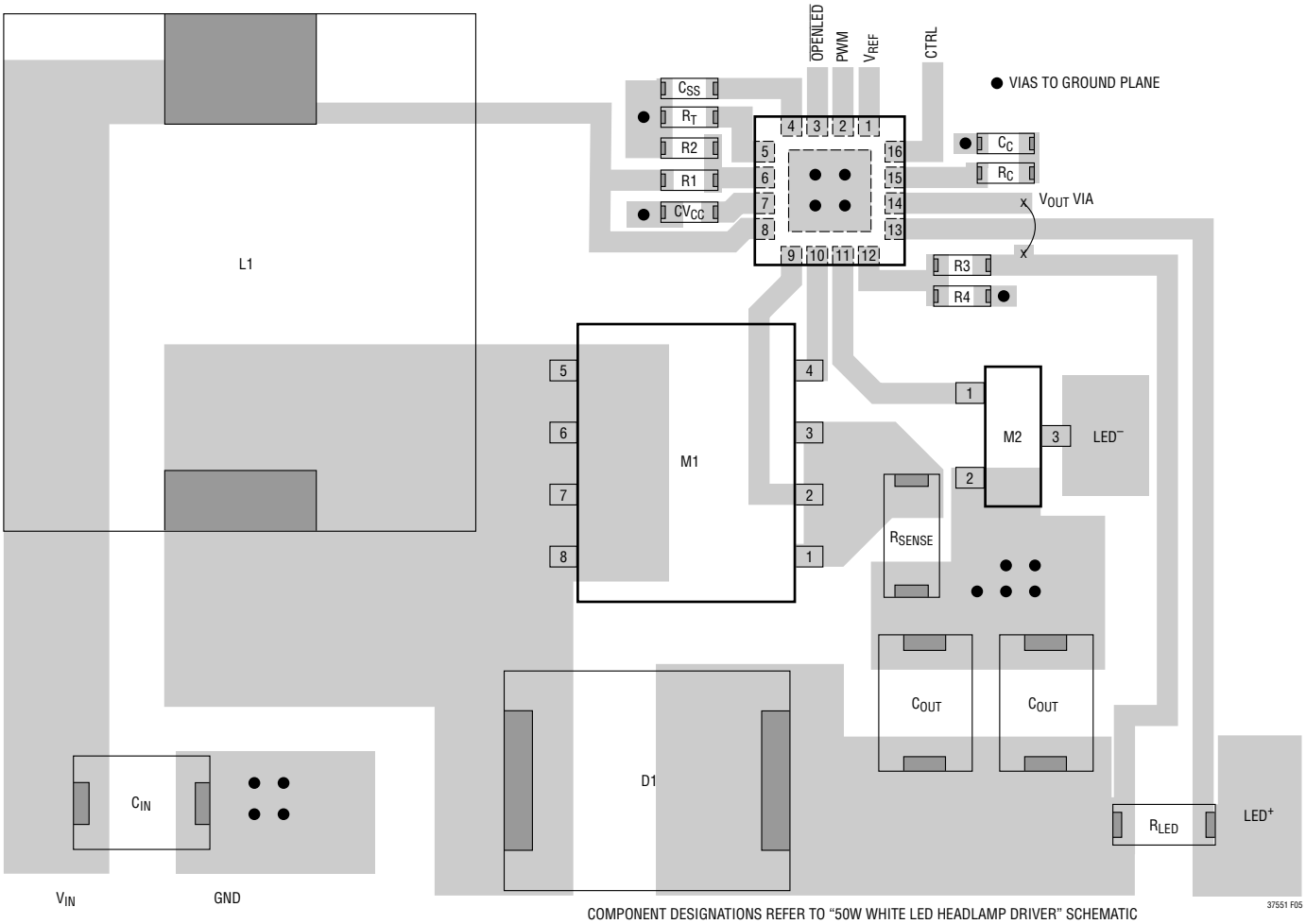
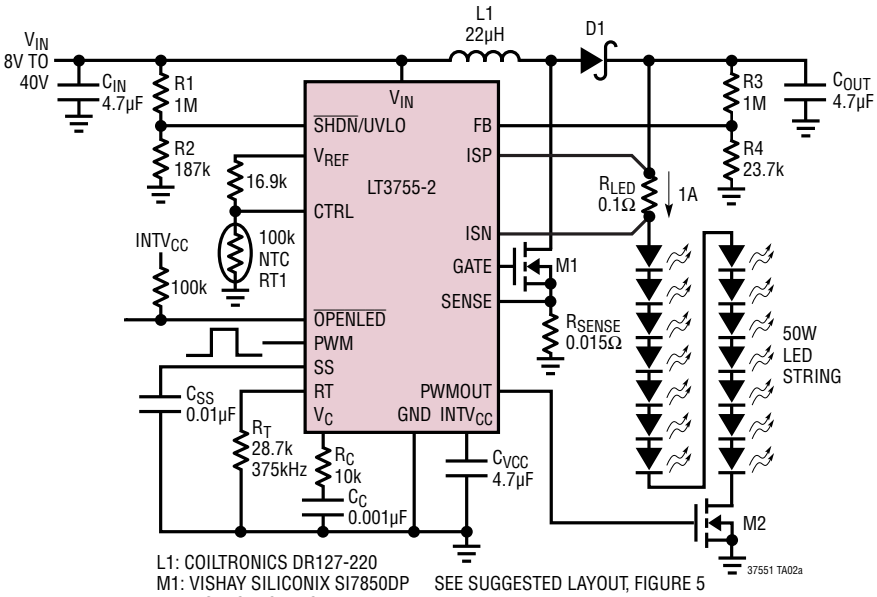


Figure 5. Boost Converter Suggested Layout

TYPICAL APPLICATIONS

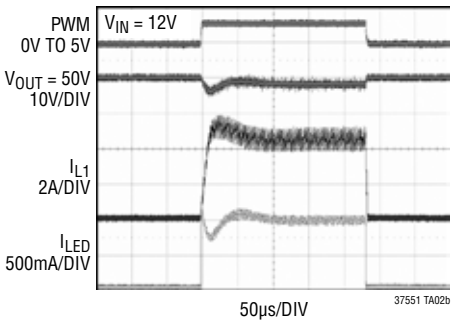
50W White LED Headlamp Driver



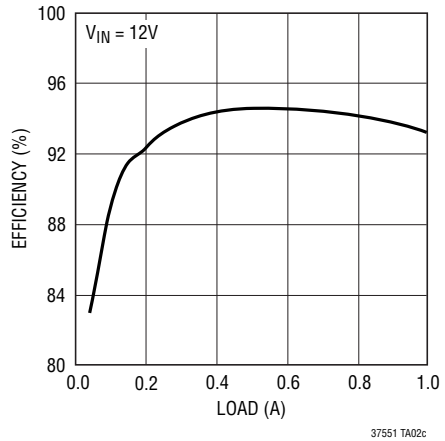
L1: COILTRONICS DR127-220
M1: VISHAY SILICONIX SI7850DP
D1: DIODES INC. PDS5100
M2: VISHAY SILICONIX SI2308DS
RT1: MURATA NCP18WM1045

SEE SUGGESTED LAYOUT, FIGURE 5

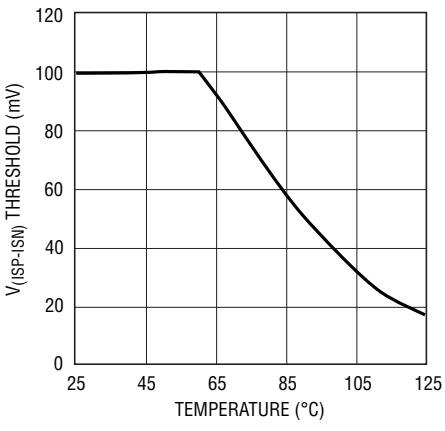
Waveforms for 50W LED Driver with PWM Disconnect NFET



Efficiency vs Load

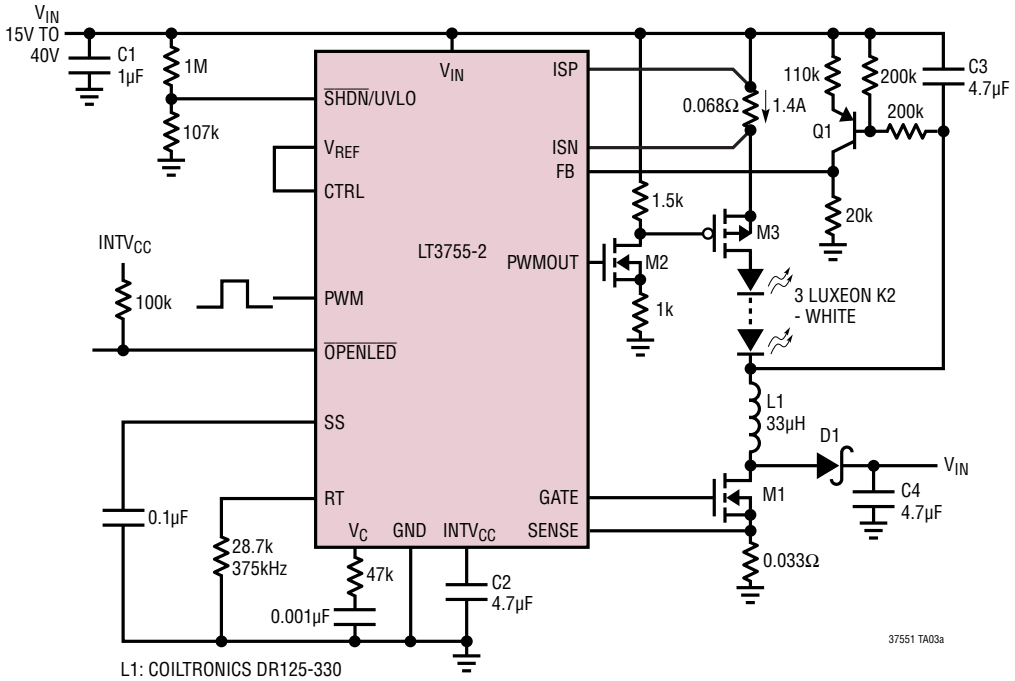


V(ISP-ISN) Threshold vs Temperature for NTC Resistor Divider



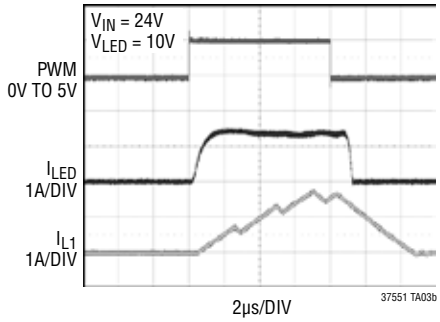
TYPICAL APPLICATIONS

Buck Mode 1.4A LED Driver

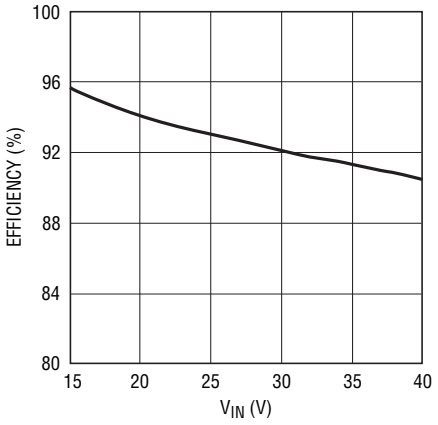


L1: COILTRONICS DR125-330
M1: VISHAY SILICONIX SI7850DP
D1: ON SEMICONDUCTOR MBRS360
M2: ZETEX ZXMN4A06G
M3: ZETEX ZXM62P03E6
Q1: ZETEX FMMT558

1000:1 PWM Dimming at 120Hz with Buck Mode

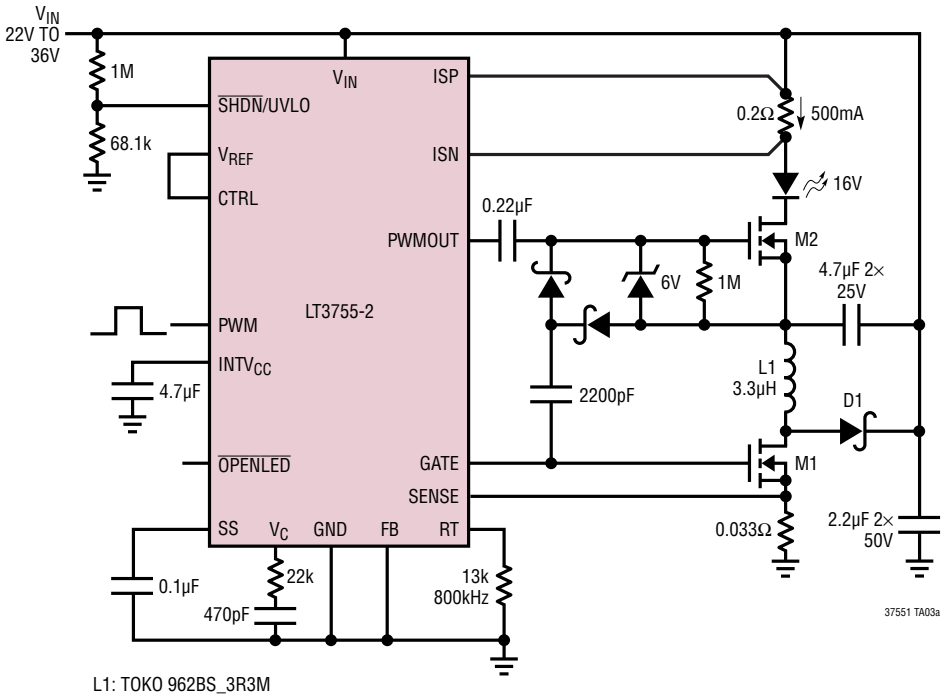


Efficiency vs V_{IN}



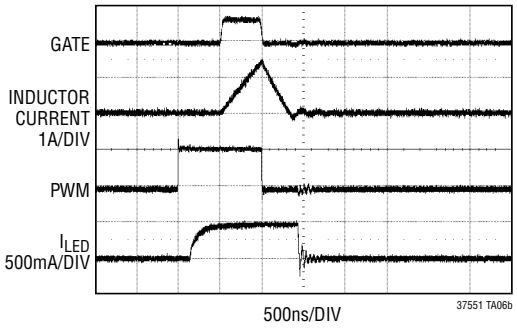
TYPICAL APPLICATIONS

Buck Mode 500mA LED Driver for 20kHz PWM Dimming

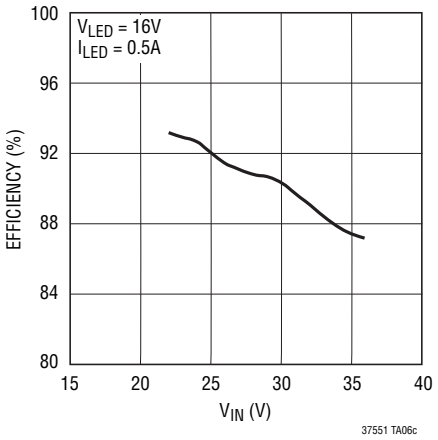


L1: TOKO 962BS_3R3M
M1: VISHAY SILICONIX SI7850DP
M2: VISHAY SILICONIX SI2306DS
D1: DIODES, INC SBM540

Minimum PWM Pulse Switching Waveform

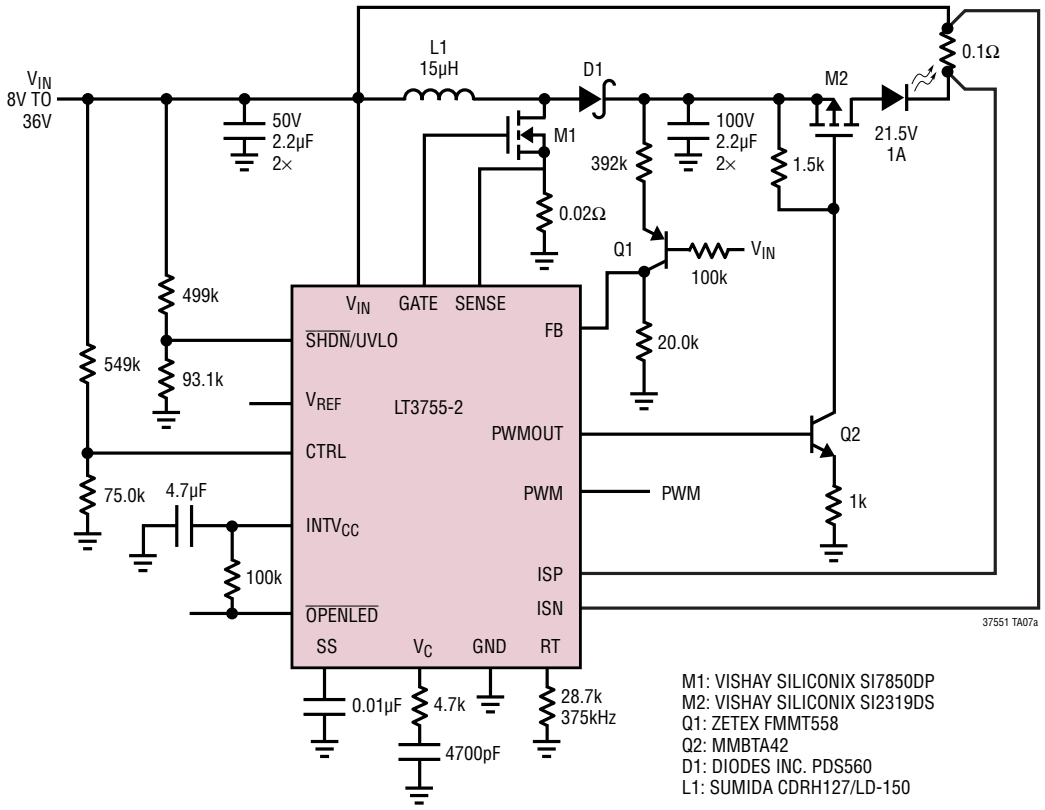


Efficiency vs V_{IN}



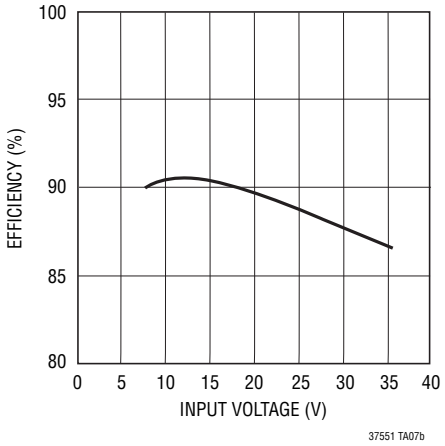
TYPICAL APPLICATIONS

21W Buck-Boost Mode with 250:1 PWM Dimming and Open LED Protection

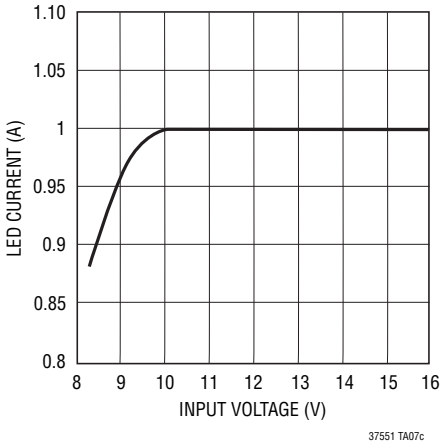


M1: VISHAY SILICONIX SI7850DP
M2: VISHAY SILICONIX SI2319DS
Q1: ZETEX FMMT558
Q2: MMBTA42
D1: DIODES INC. PDS560
L1: SUMIDA CDRH127/LD-150

Buck-Boost Mode Efficiency vs Input Voltage

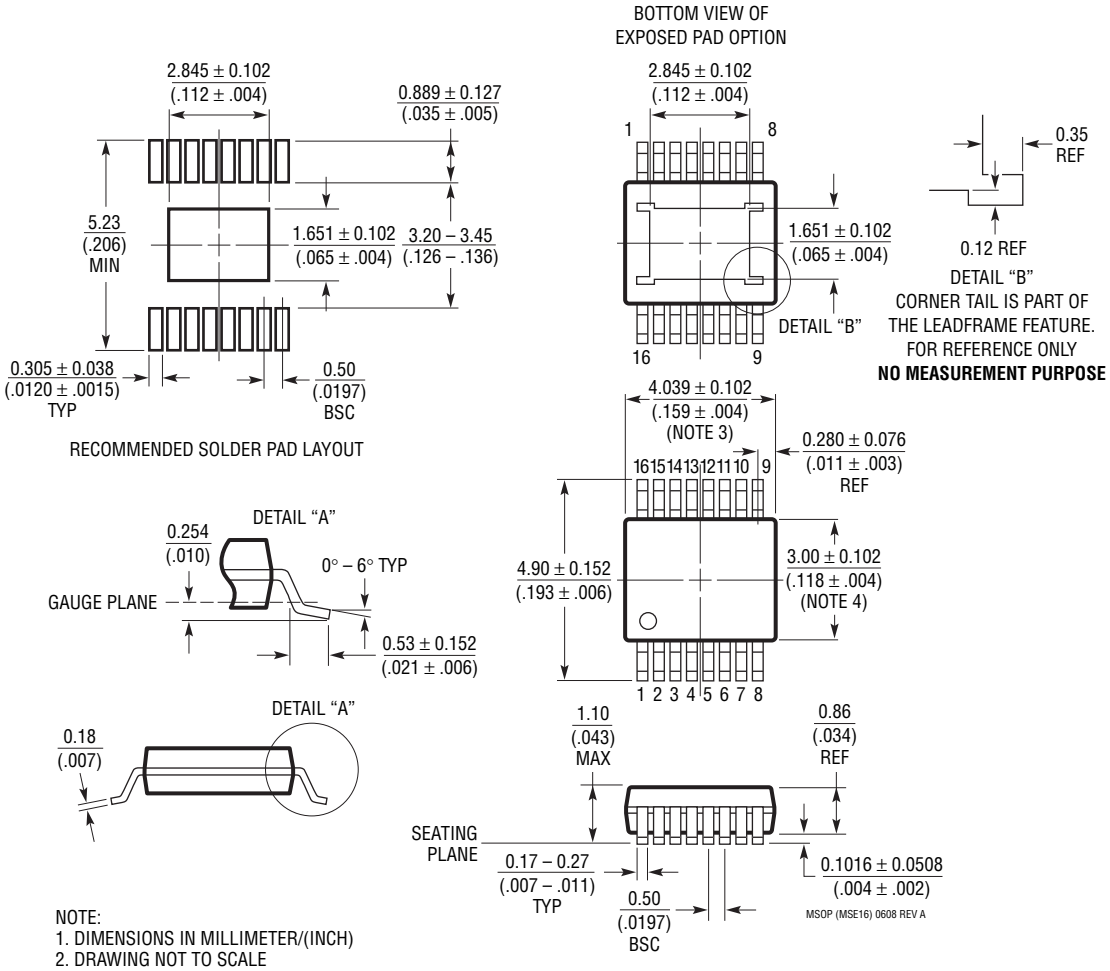


Buck-Boost Mode LED Current vs Low Input Voltage



PACKAGE DESCRIPTION

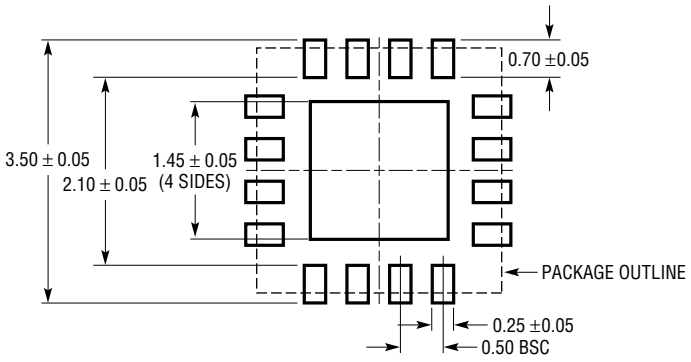
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



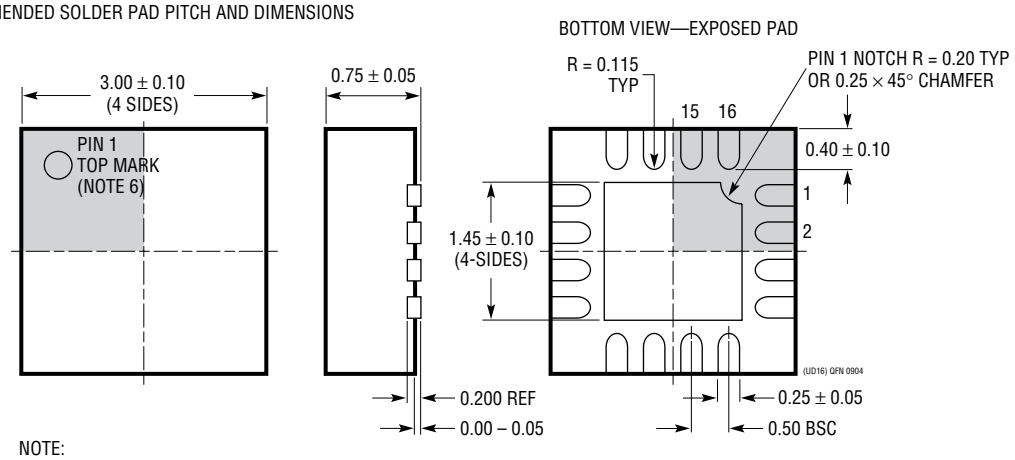
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

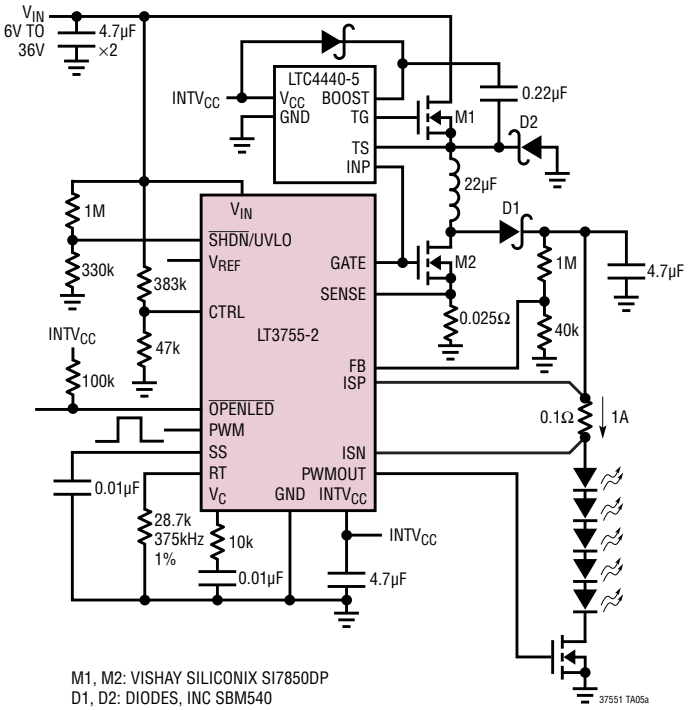
REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	03/10	Revised Entire Data Sheet to Include H-Grade	1-26

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

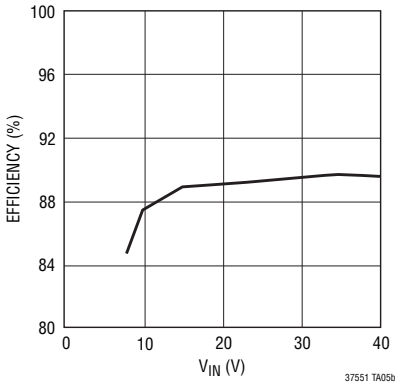
TYPICAL APPLICATION

Buck-Boost LED Driver for Automotive



M1, M2: VISHAY SILICONIX SI7850DP
D1, D2: DIODES, INC SBM540

Efficiency vs V_{IN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3474	36V, 1A (I_{LED}), 2MHz, Step-Down LED Driver	V_{IN}: 4V to 36V, $V_{OUT(MAX)}$ = 13.5V, True Color PWM Dimming = 400:1, I_{SD} < 1µA, TSSOP16E Package
LT3475	Dual 1.5A (I_{LED}), 36V, 2MHz Step-Down LED Driver	V_{IN}: 4V to 36V, $V_{OUT(MAX)}$ = 13.5V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, TSSOP20E Package
LT3476	Quad Output 1.5A, 36V, 2MHz High Current LED Driver with 1000:1 Dimming	V_{IN}: 2.8V to 16V, $V_{OUT(MAX)}$ = 36V, True Color PWM Dimming = 1000:1, I_{SD} < 10µA, 5mm × 7mm QFN Package
LT3477	3A, 42V, 3MHz Boost, Buck-Boost, Buck LED Driver	V_{IN}: 2.5V to 25V, $V_{OUT(MAX)}$ = 40V, Dimming = Analog/PWM, I_{SD} < 1µA, QFN and TSSOP20E Packages
LT3478/LT3478-1	4.5A, 42V, 2.5MHz High Current LED Driver with 3000:1 Dimming	V_{IN}: 2.8V to 36V, $V_{OUT(MAX)}$ = 42V, True Color PWM Dimming = 3000:1, I_{SD} < 3µA, TSSOP16E Package
LT3486	Dual 1.3A, 2MHz High Current LED Driver	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 36V, True Color PWM Dimming = 1000:1, I_{SD} < 1µA, 5mm × 3mm DFN and TSSOP16E Packages
LT3496	Triple 0.75A, 2.1MHz, 45V LED Driver	V_{IN}: 3V to 30V, $V_{OUT(MAX)}$ = 45V, Dimming = 3000:1, I_{SD} < 1µA, 4mm × 5mm QFN and TSSOP16E Packages
LT3517	1.3A, 2.5MHz, 45V LED Driver	V_{IN}: 3V to 30V, $V_{OUT(MAX)}$ = 45V, Dimming = 3000:1, I_{SD} < 1µA, 4mm × 4mm QFN and TSSOP16E Packages
LT3518	2.3A, 2.5MHz, 45V LED Driver	V_{IN}: 3V to 30V, $V_{OUT(MAX)}$ = 45V, Dimming = 3000:1, I_{SD} < 1µA, 4mm × 4mm QFN and TSSOP16E Packages
LT3756/LT3756-1/ LT3756-2	100V_{IN}, 100V_{OUT} LED Controller	V_{IN}: 6V to 100V, $V_{OUT(MAX)}$ = 100V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, 3mm × 3mm QFN-16 and MS16E Packages
LTC®3783	High Current LED Controller	V_{IN}: 3V to 36V, $V_{OUT(MAX)}$ = Ext FET, True Color PWM Dimming = 3000:1, I_{SD} < 20µA, 5mm × 4mm QFN10 and TSSOP16E Packages

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