

500MHz, 2200V/ μ s Gain of 2, Single Supply Triple Video Amplifier with Input Bias Control

FEATURES

- **–3dB Small-Signal Bandwidth: 500MHz**
- **–3dB 2V_{P-P} Large-Signal Bandwidth: 400MHz**
- **Slew Rate: 2200V/ μ s**
- **Fixed Gain of 2, No External Resistors Required**
- **AC Coupling with Programmable DC Input Bias**
- **Output Swings to 0.8V of Supply Rails**
- **Full Video Swing with 5V Single Supply**
- Diff Gain: 0.02%
- Diff Phase: 0.05°
- Enable/Shutdown Pin
- High Output Current: ± 100 mA
- Supply Range: 3V to 7.5V
- Operating Temperature Range: –40°C to 85°C
- Available in 16-Lead SSOP and 5mm $\times$ 3mm DFN Packages

APPLICATIONS

- LCD Video Projectors
- RGB HD Video Amplifiers
- Coaxial Cable Drivers
- Low Supply ADC Drivers

DESCRIPTION

The LT[®]6557 is a high speed triple video amplifier with an internal fixed gain of 2 and a programmable DC input bias voltage. This amplifier features a 400MHz 2V_{P-P} signal bandwidth, 2200V/ μ s slew rate and a unique ability to drive heavy output loads to 0.8V of the supply rails, making the LT6557 ideal for a single 5V supply, wideband video application. With just one resistor, the inputs of all three amplifiers can be programmed to a common voltage level, simplifying and reducing the need for external circuitry in the AC-coupled applications. Without the programmable resistor, the input bias circuit becomes inactive, allowing the use of an external clamp circuit or direct coupled input.

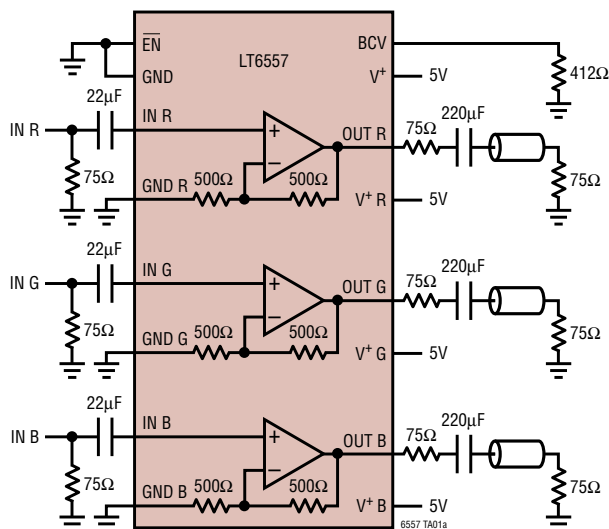
The LT6557 has separate power supply and ground pins for each amplifier to improve channel separation and to ease power supply bypassing. The LT6557 provides uncompromised performance in many high speed applications where a low voltage, single supply is required.

The LT6557 is available in 16-lead SSOP and 5mm $\times$ 3mm DFN packages.

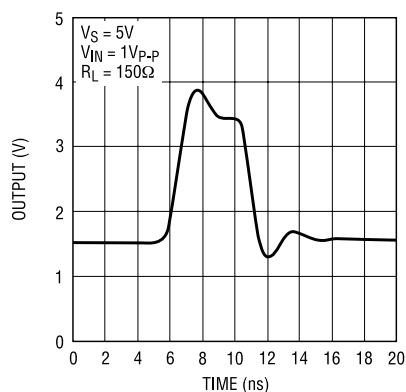
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TYPICAL APPLICATION

AC-Coupled Triple Video Driver



Fast Large-Signal Transient Response



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_S^+ to GND)	7.5V	Junction Temperature	
Input Current.....	$\pm 10\text{mA}$	SSOP	150°C
Output Current (Note 2)	$\pm 70\text{mA}$	DFN.....	125°C
Output Short-Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	
Operating Temperature Range (Note 3) ...	-40°C to 85°C	SSOP	-65°C to 150°C
Specified Temperature Range (Note 4)	-40°C to 85°C	DFN.....	-65°C to 125°C
		Lead Temperature (Soldering, 10 sec)	
		SSOP	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW GN PACKAGE 16-LEAD PLASTIC SSOP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 110^\circ\text{C/W}$		TOP VIEW DHC PACKAGE 16-LEAD (5mm x 3mm) PLASTIC DFN $T_{JMAX} = 125^\circ\text{C}$, $\theta_{JA} = 40^\circ\text{C/W}$ EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB	
ORDER PART NUMBER	GN PART MARKING	ORDER PART NUMBER	DHC PART MARKING*
LT6557CGN	6557	LT6557CDHC	6557
LT6557IGN	6557I	LT6557IDHC	6557
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/			

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, $R_L = 150\Omega$ to $V_S/2$, $V_{EN} = 0.4\text{V}$, $R_{BCV} = \text{open}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{IN} = 1.25\text{V}$		12 15	40 50	mV
I_{IN}	Input Current	$V_{IN} = 1.25\text{V}$		35 45	70 100	μA
R_{IN}	Input Resistance	$V_{IN} = 0.75\text{V}$ to 1.75V , BCV (Pin 6) Open	90 50	200 150		k Ω k Ω
C_{IN}	Input Capacitance	$f = 1\text{MHz}$		1.5		pF

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, $R_L = 150\Omega$ to $V_S/2$, $V_{EN} = 0.4\text{V}$, $R_{BCV} = \text{open}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$A_V \text{ ERR}$	Gain Error	$V_{IN} = 0.75\text{V to } 1.75\text{V}$	●	± 0.5 ± 0.5	± 2.5 ± 3.0	% %
$A_V \text{ MATCH}$	Gain Match Between Channels	$V_{IN} = 0.75\text{V to } 1.75\text{V}$	●	± 0.4 ± 0.4	± 2.75 ± 3.25	% %
$V_{IN(DC)}$	Input Voltage Bias	$R_{BCV} = 348\Omega$	●	1.0 0.8	1.25 1.10	1.5 1.7 V V
PSRR	Power Supply Rejection Ratio	$V_S = 4\text{V to } 6\text{V}$, $V_{IN} = 1.25\text{V}$	●	42 38	50 47	dB dB
V_{OL}	Output Voltage Swing Low		●	0.8 0.9	0.9 1.0	V V
V_{OH}	Output Voltage Swing High		●	4.1 4.0	4.2 4.1	V V
I_S	Supply Current per Amplifier	$V_{EN} = 0.4\text{V}$, $R_L = \infty$, Includes I_S of V^+ (Pin 15)	●	22.5 25.0	25 29	mA mA
	Total Supply Current (Disabled)	$V_{EN} = \text{Open}$, $R_L = \infty$	●	10 10	450 1000	μA μA
I_{EN}	Enable Pin Current	$V_{EN} = 0.4\text{V}$	●	-250 -300	-125 -150	μA μA
I_{SC}	Short-Circuit Current		●	± 70 ± 40	± 100 ± 90	mA mA
SR	Slew Rate	$V_{OUT} = 1.25\text{V to } 3.75\text{V}$ (Note 5)		1400	2200	V/ μs
-3dB BW	-3dB Bandwidth	$V_{OUT} = 2V_{P-P}$		400		MHz
		$V_{OUT} = 0.2V_{P-P}$		500		MHz
0.1dB BW	Gain Flatness $\pm 0.1\text{dB}$ Bandwidth	$V_{OUT} = 2V_{P-P}$		120		MHz
FPBW	Full Power Bandwidth	$V_{OUT} = 2V_{P-P}$ (Note 6)		220	350	MHz
XTalk	All Hostile Crosstalk	$f = 10\text{MHz}$, $V_{OUT} = 2V_{P-P}$ $f = 100\text{MHz}$, $V_{OUT} = 2V_{P-P}$		-80 -55		dB dB
t_S	Settling Time	To 1%, $V_{OUT} = 1.5\text{V to } 3.5\text{V}$		4		ns
		To 0.1%		7		ns
t_r , t_f	Rise Time, Fall Time	10% to 90%, $V_{OUT} = 1.5\text{V to } 3.5\text{V}$		875		ps
ΔG	Differential Gain	NTSC Signal		0.02		%
$\Delta \Phi$	Differential Phase	NTSC Signal		0.05		Deg
HD2	2nd Harmonic Distortion	$f = 10\text{MHz}$, $V_{OUT} = 2V_{P-P}$		-68		dBc
HD3	3rd Harmonic Distortion	$f = 10\text{MHz}$, $V_{OUT} = 2V_{P-P}$		-75		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating.

Note 3: The LT6557C is guaranteed functional over the temperature range of -40°C and 85°C .

Note 4: The LT6557C is guaranteed to meet specified performance from 0°C to 70°C . The LT6557C is designed, characterized and expected to

meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6557I is guaranteed to meet specified performance from -40°C to 85°C .

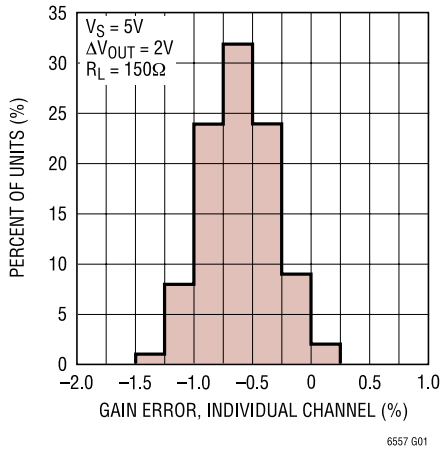
Note 5: Slew rate is 100% production tested on the R channel and measured on the rising edge of the output signal. The slew rate of the falling edge and of the G and B channels is guaranteed through design and characterization.

Note 6: Large-signal bandwidth is calculated from slew rate:

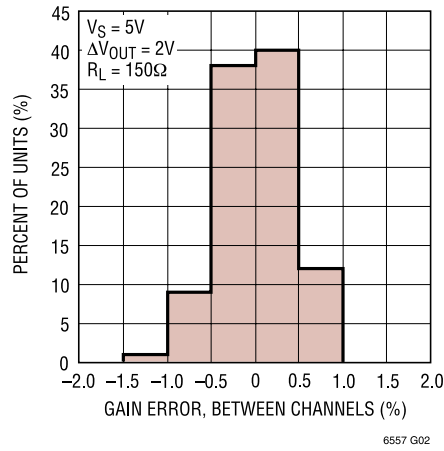
$$\text{FPBW} = \text{SR}/(\pi \cdot V_{P-P})$$

TYPICAL PERFORMANCE CHARACTERISTICS

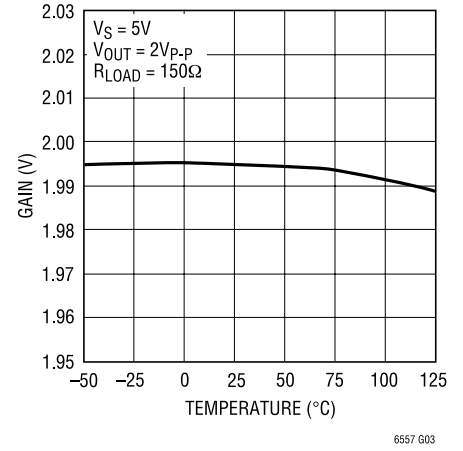
Gain Error Distribution



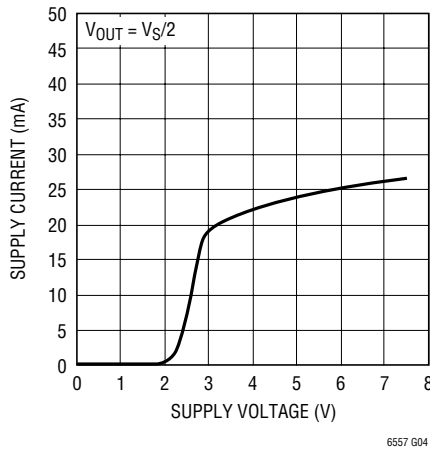
Gain Error Matching Distribution



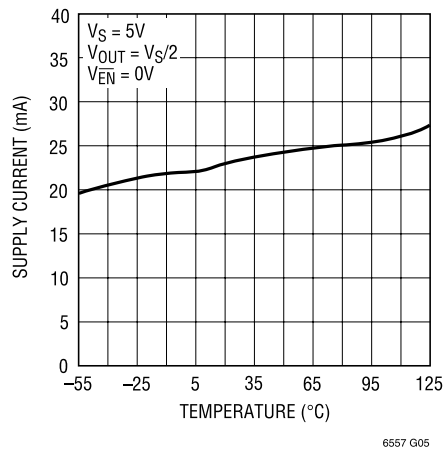
Voltage Gain vs Temperature



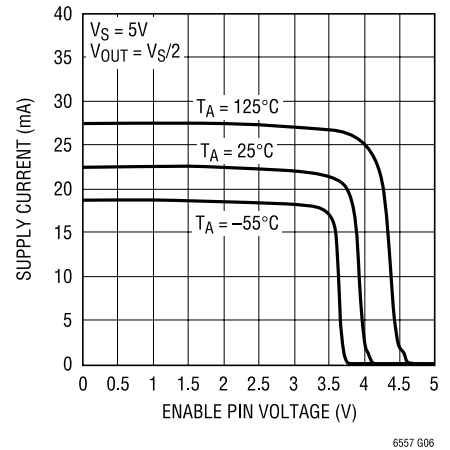
Supply Current per Amplifier vs Supply Voltage



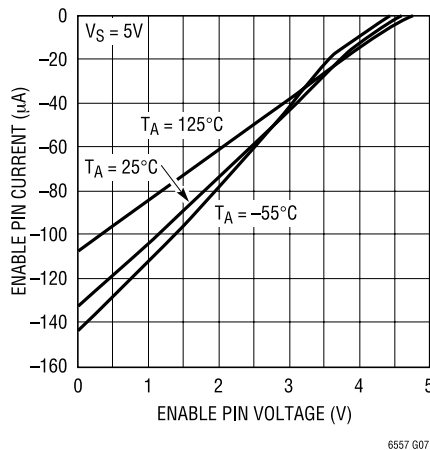
Supply Current per Amplifier vs Temperature



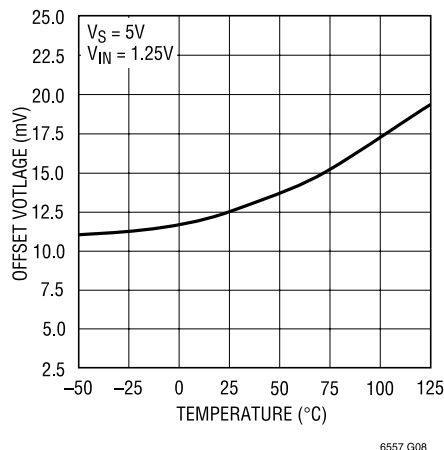
Supply Current per Amplifier vs EN Voltage



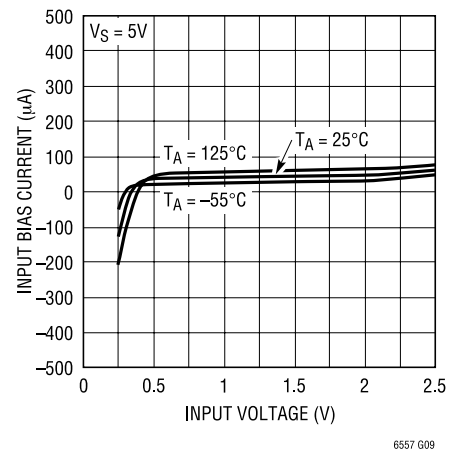
EN Pin Current vs EN Pin Voltage



Input Referred Offset Voltage vs Temperature

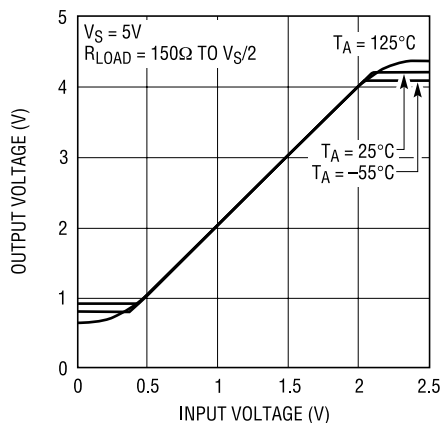


Input Bias Current vs Input Voltage



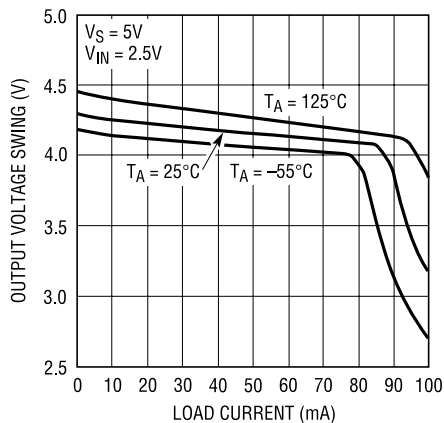
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Input Voltage



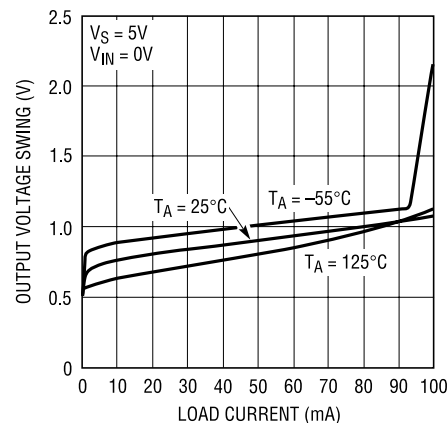
6557 G10

Output Voltage Swing vs Load Current (Output High)



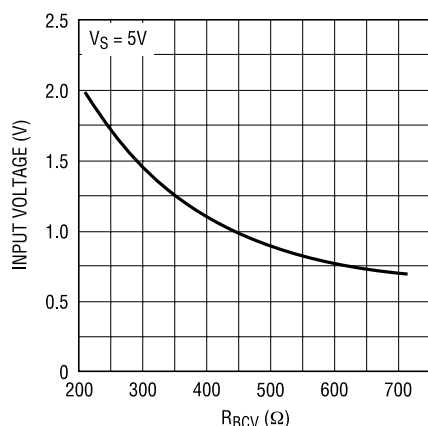
6557 G11

Output Voltage Swing vs Load Current (Output Low)



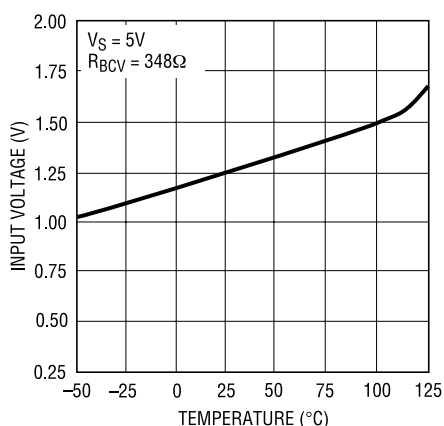
6557 G12

Input Bias Voltage vs Resistance at BCV Pin



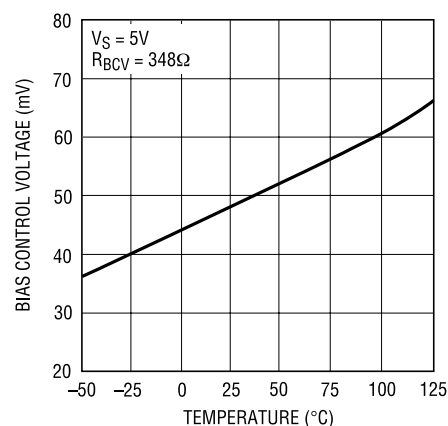
6557 G13

Input Bias Voltage vs Temperature



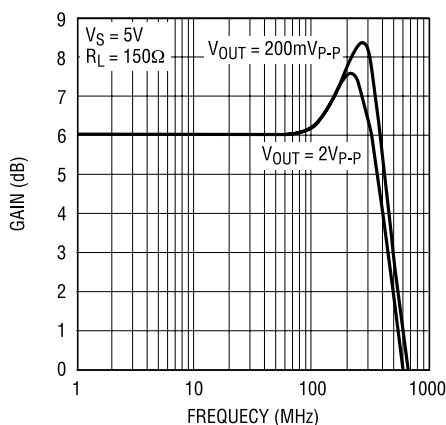
6557 G14

Bias Control Voltage vs Temperature



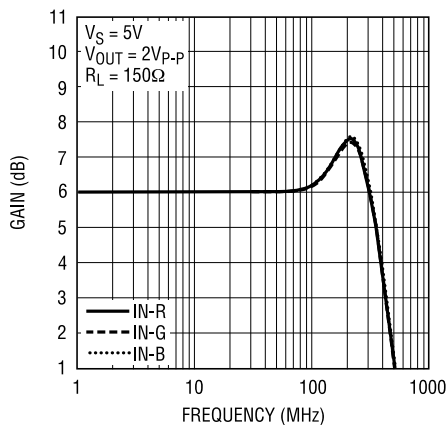
6557 G15

Frequency Response



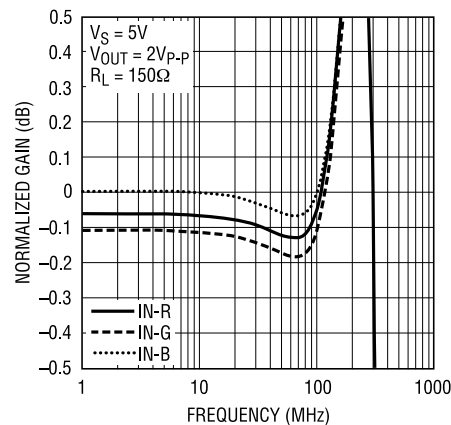
6557 G16

Frequency Response of Three Amplifiers



6557 G17

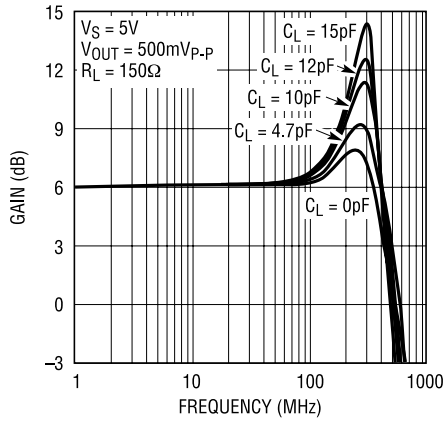
Gain Flatness vs Frequency



6557 G18

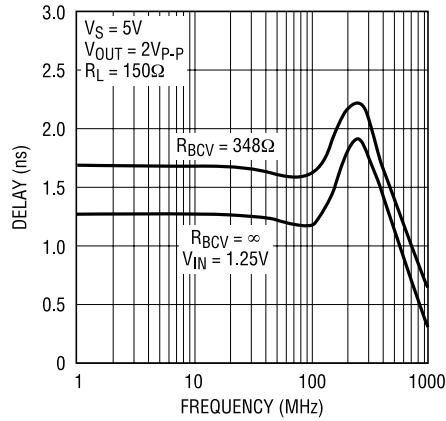
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response with Capacitive Loads



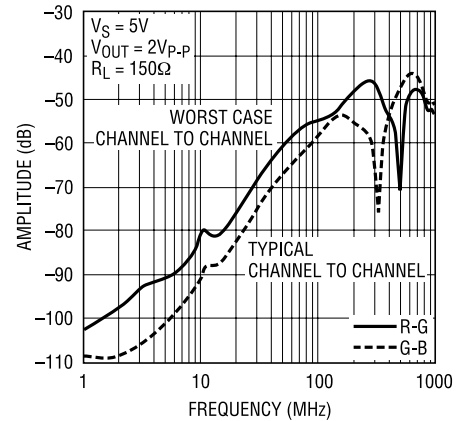
6557 G25

Large-Signal Group Delay



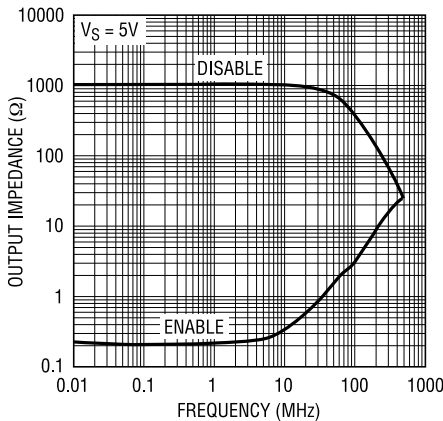
6557 G26

Crosstalk Between Amplifiers vs Frequency



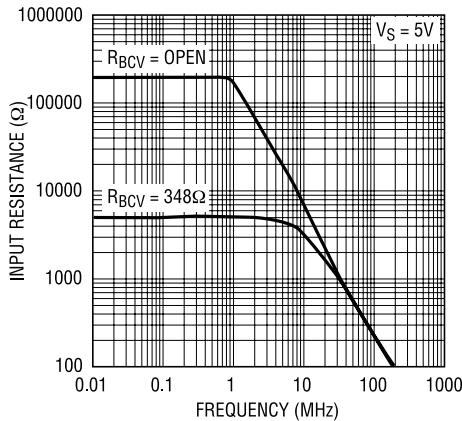
6557 G19

Output Impedance vs Frequency



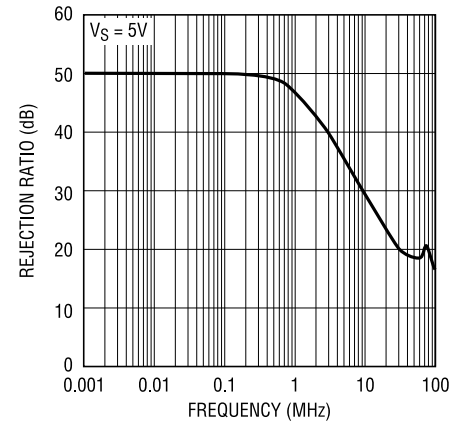
6557 G20

Input Impedance vs Frequency



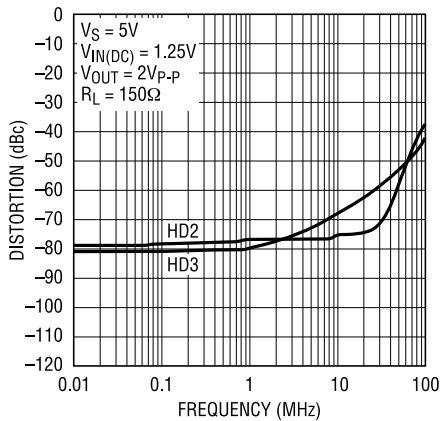
6557 G21

PSRR vs Frequency



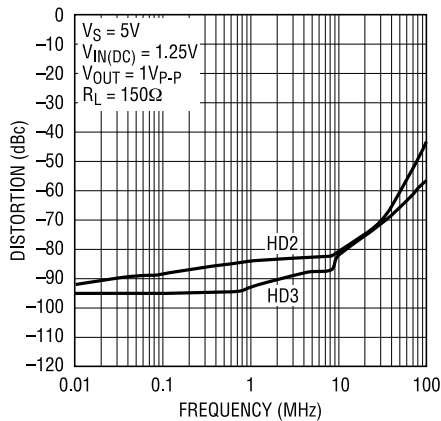
6557 G22

Distortion vs Frequency



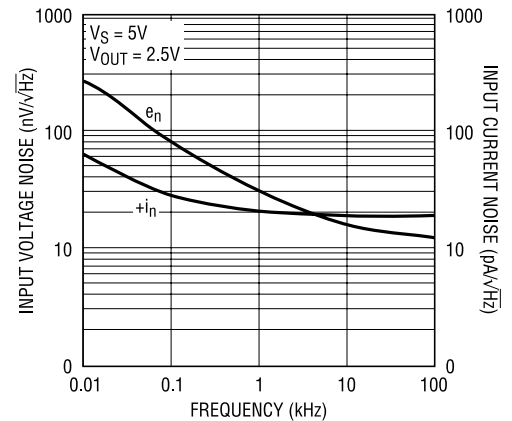
6557 G23

Distortion vs Frequency



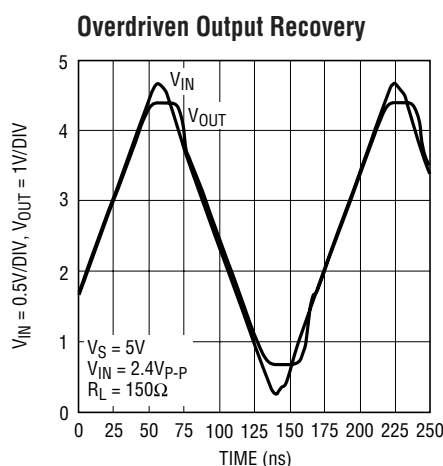
6557 G24

Input Referred Noise Spectral Density

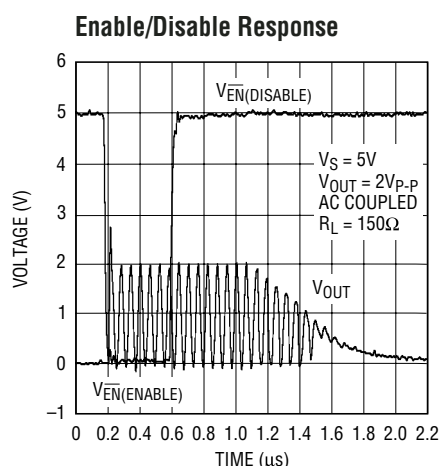


6557 G27

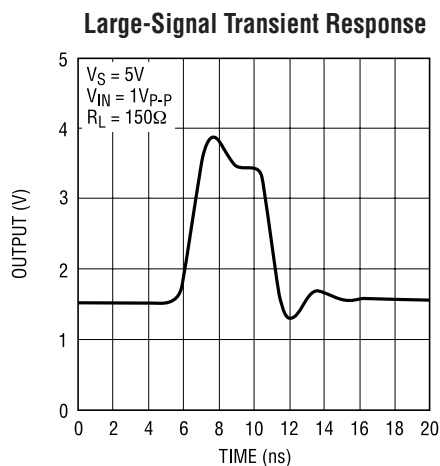
TYPICAL PERFORMANCE CHARACTERISTICS



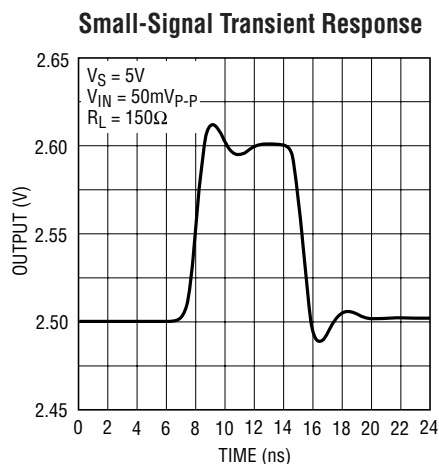
6557 G28



6557 G29



6557 G30



6557 G31

PIN FUNCTIONS

EN (Pin 1): Enable Control Pin. The part is enabled when this pin is pulled low. An internal pull-up resistor of 40k will turn the part off if this pin is unconnected.

GND (Pin 2): Ground Reference for Enable Pin (Pin 1) and Bias Control Voltage Pin (Pin 16). This pin must be connected externally to ground.

IN R (Pin 3): Red Channel Input. This pin has a nominal impedance of 200k Ω with input bias circuit inactive, Pin 16 open.

GND R (Pin 4): Ground of Red Channel Amplifier. This pin is not internally connected to other ground pins and must be connected externally to ground.

IN G (Pin 5): Green Channel Input. This pin has a nominal impedance of 200k Ω with input bias circuit inactive, Pin 16 open.

GND G (Pin 6): Ground of Green Channel Amplifier. This pin is not internally connected to other ground pins and must be connected externally to ground.

IN B (Pin 7): Blue Channel Input. This pin has a nominal impedance of 200k Ω with input bias circuit inactive, Pin 16 open.

GND B (Pin 8): Ground of Blue Channel Amplifier. This pin is not internally connected to other ground pins and must be connected externally to ground.

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PIN FUNCTIONS

V⁺ B (Pin 9): Positive Supply Voltage of Blue Channel Amplifier. This pin is not internally connected to other supply voltage pins and must be externally connected to the supply voltage bus with proper bypassing for best performance, see Power Supply Considerations.

OUT B (Pin 10): Blue Channel Output.

V⁺ G (Pin 11): Positive Supply Voltage of Green Channel Amplifier. This pin is not internally connected to other supply voltage pins and must be externally connected to the supply voltage bus with proper bypassing for best performance, see Power Supply Considerations.

OUT G (Pin 12): Green Channel Output.

V⁺ R (Pin 13): Positive Supply Voltage of Red Channel Amplifier. This pin is not internally connected to other supply voltage pins and must be externally connected to

the supply voltage bus with proper bypassing for best performance, see Power Supply Considerations.

OUT R (Pin 14): Red Channel Output.

V⁺ (Pin 15): Positive Supply Voltage of Control Circuitry. This pin is not internally connected to other supply voltage pins and must be externally connected to supply voltage bus with proper bypassing for best performance, see Power Supply Considerations.

BCV (Pin 16): Bias Control Voltage. A resistor connected between Pin 16 and Pin 2 (GND) will generate a DC voltage bias at the inputs of the three amplifiers for AC coupling application, see Programmable Input Bias.

Exposed Pad (Pin 17, DFN Package): Ground. This pad must be soldered to PCB and is internally connected to GND (Pin 2).

APPLICATIONS INFORMATION

Power Supply Considerations

The LT6557 is optimized to provide full video signal swing output when operated from a standard 5V single supply. Due to the supply current involved in ultrahigh slew rate amplifiers like the LT6557, selection of the lowest workable supply voltage is recommended to minimize heat generation and simplify thermal management. Temperature rise at the internal devices (T_J) must be kept below 150°C (SSOP package) or 125°C (DFN package), and can be estimated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$T_J = T_A + P_D \cdot 40^\circ\text{C/W for DFN package}$$

or

$$T_J = T_A + P_D \cdot 110^\circ\text{C/W for SSOP package}$$

$$\text{where } P_D = (I_S + 0.5 \cdot I_O) \cdot V_{S(\text{TOTAL})}$$

The latter equation assumes (conservatively) that the output swing is small relative to the supply and RMS load current (I_O) is bidirectional (as with AC coupling).

The grounds are separately pinned for each amplifier to minimize crosstalk.

Operation from split supplies can be accomplished by connecting the LT6557 ground pins to the negative rail. Since the amplifier gain is referenced to its ground pins, the actual signals are referenced to the negative rail, in this case, and DC coupled applications need to take this into consideration. With dual supplies, recommended voltages range from nominal $\pm 2.5\text{V}$ to $\pm 3.3\text{V}$.

The ultrahigh frequency (UHF) operating range of the LT6557 requires that careful printed circuit layout practices be followed to obtain maximum performance. Trace lengths between power pins and bypass capacitors should be minimized (< 0.1 inch) and one or more dedicated ground planes should be employed to minimize parasitic inductance. Poor layout or breadboarding methods can seriously impact amplifier stability, frequency response and crosstalk performance. A 2.2 μF and a 10 μF bypass capacitor is recommended for the LT6557 supply bus, plus a 10nF high frequency bypass capacitor at each individual power pin.

APPLICATIONS INFORMATION

Programmable Input Bias

The LT6557 contains circuitry that provides a user-programmed bias voltage to the inputs of all three amplifier sections. The internal biasing feature is designed to minimize external component count in AC-coupled applications, but may be defeated if external biasing is desired. Figure 1 shows the simplified equivalent circuit feeding the noninverting input of each amplifier. A programming resistor from Pin 16 to GND (Pin 2) establishes the nominal

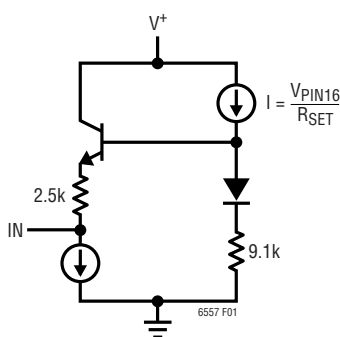


Figure 1. Simplified Programmable Input Bias Circuit Diagram

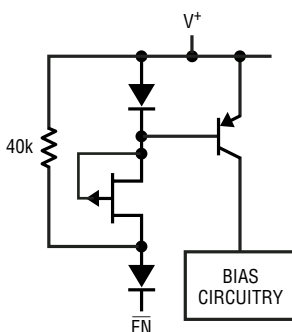
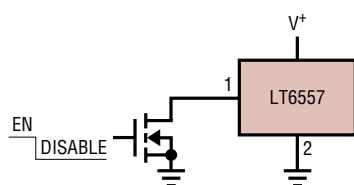
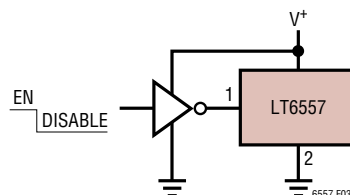


Figure 2. Simplified Shutdown Circuit Diagram



(3a) Open Drain or Open Collector



(3b) CMOS Gate with Shared Supply

Figure 3. Suitable Shutdown Pin Drive Circuits

no-signal amplifier input bias condition according to the following relationship:

$$V_{\text{BIAS(IN)}} = \frac{V_{\text{PIN16}} \cdot 9.1\text{k}}{R_{\text{SET}}}$$

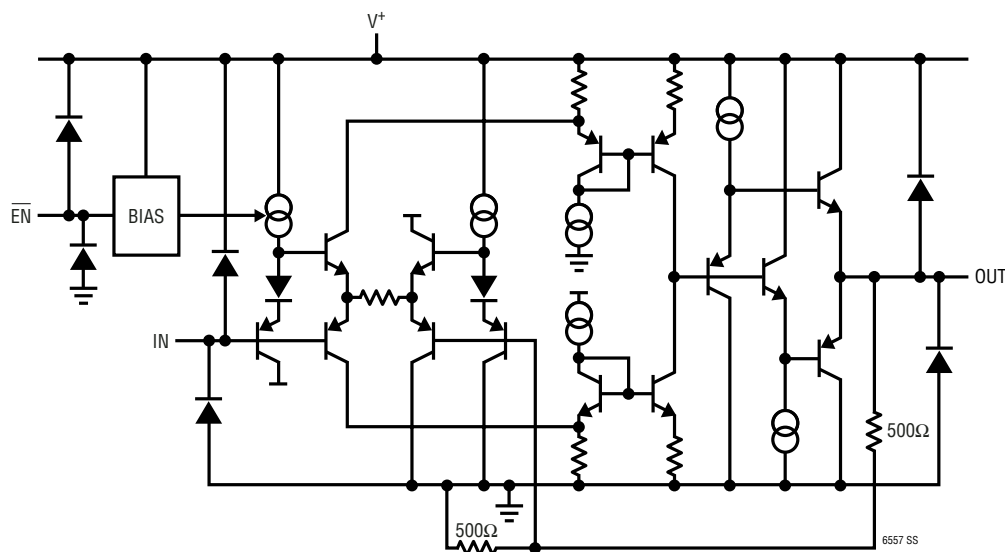
where $V_{\text{PIN16}} = 0.048\text{V}$ typical.

For single 5V supply operation, a 400Ω programming resistor is generally optimal. In applications that demand maximum amplifier linearity, or if external biasing is preferred (in DC-coupled applications, for example), the internal biasing circuitry may be disabled by leaving Pin 16 open. With Pin 16 open, input loading is approximately $200\text{k}\Omega$.

Shutdown Control

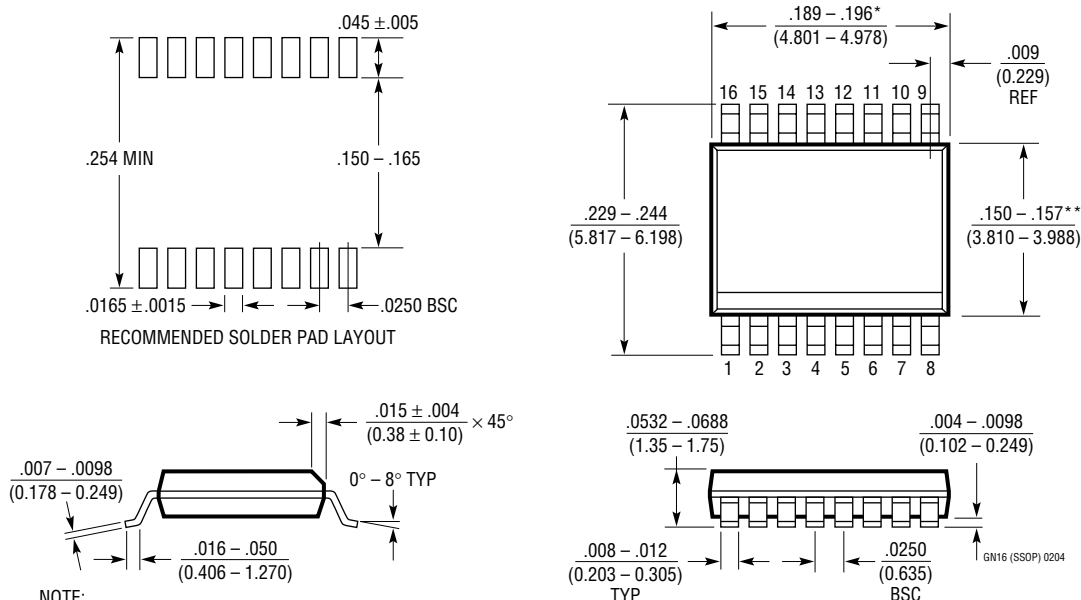
The LT6557 may be placed into a shutdown mode, where all three amplifier sections are deactivated and power supply draw is reduced to approximately $10\mu\text{A}$. When the $\overline{\text{EN}}$ pin is left open, an internal $40\text{k}\Omega$ pull-up resistor brings the pin to V^+ and the part enters the shutdown mode. Pulling the pin more than approximately 1.5V below V^+ will enable the LT6557 (see Figure 2 for equivalent circuit). The pull-down current required to activate the part is typically $125\mu\text{A}$. In most applications, the $\overline{\text{EN}}$ pin is simply connected to ground (for continuous operation) or driven directly by a CMOS-level logic gate (see Figure 3 for examples). Response time is typically 50ns for enabling, and $1\mu\text{s}$ for shutdown. In shutdown mode, the feedback resistors remain connected between the output pins and the individual ground (or V^- connected) pins.

SIMPLIFIED SCHEMATIC



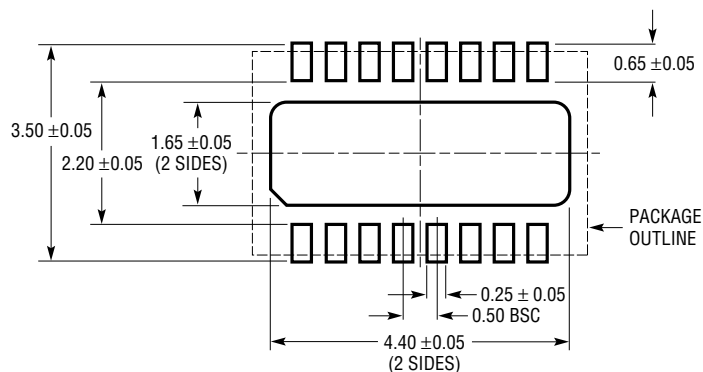
PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1641)

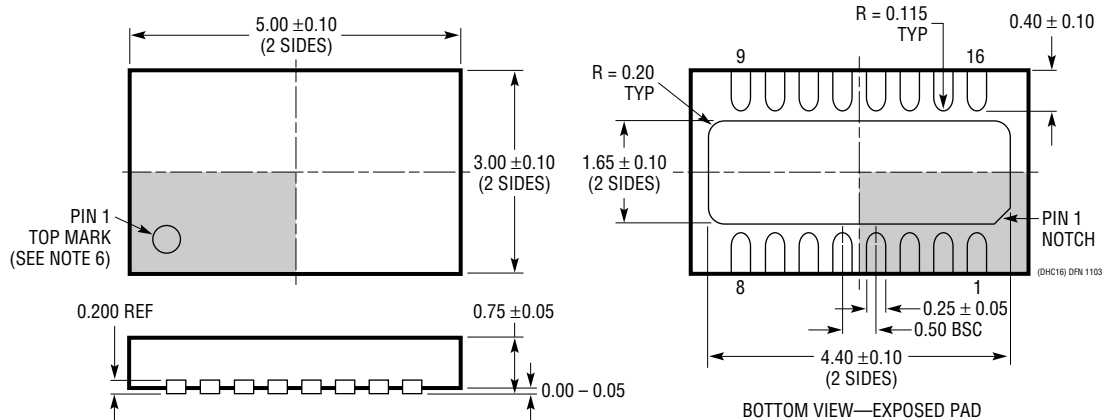


PACKAGE DESCRIPTION

DHC Package 16-Lead Plastic DFN (5mm × 3mm) (Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

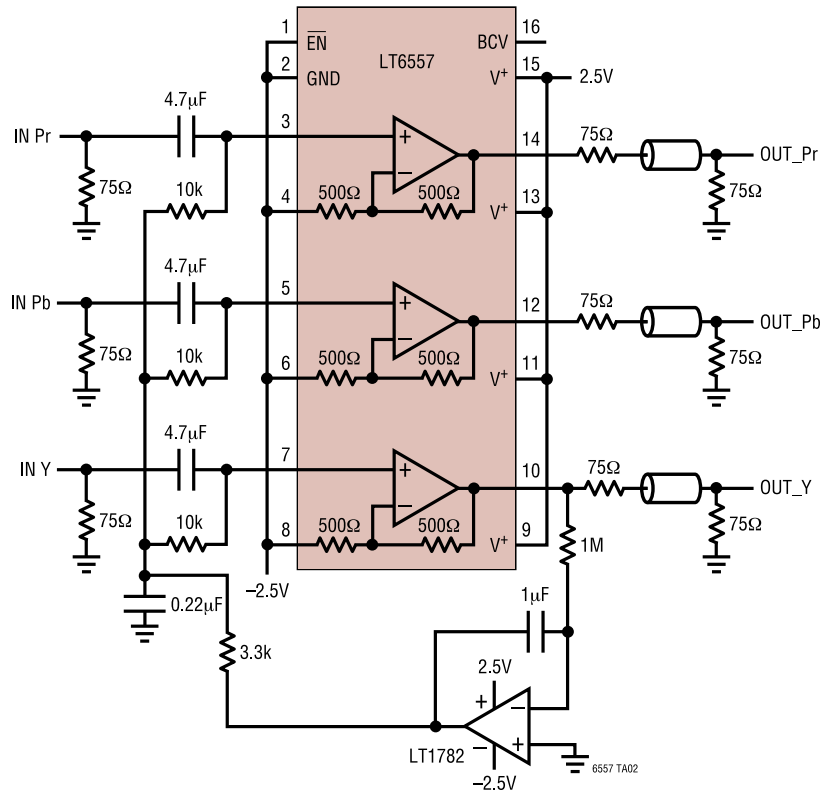


NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Split Supply Operation with DC Bias Servo



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1399	300MHz Triple Current Feedback Amplifier	0.1dB Gain Flatness to 150MHz, Shutdown
LT1675	250MHz Triple RGB Multiplexer	100MHz Pixel Switching, 1100V/μs Slew Rate, 16-Lead SSOP
LT6550/LT6551	3.3V Triple and Quad Video Buffers	110MHz Gain of 2 Buffers in MS Package
LT6553	650MHz Gain of 2 Triple Video Amplifier	Optimized for Driving 75Ω Cables
LT6554	650MHz Gain of 1 Triple Video Amplifier	Performance Similar to the LT6553 with $A_V = 1$, 16-Lead SSOP
LT6555	650MHz Gain of 2 Triple Video Multiplexer	Optimized for Driving 75Ω Cables
LT6556	750MHz Gain of 1 Triple Video Multiplexer	High Slew Rate 2100V/μs
LT6558	550MHz, 2200V/μs Gain of 1 Triple Video Amplifier	Single Supply with Input Bias Control