# Complete SO-8, 12-Bit, 400ksps ADC with Shutdown

## FEATURES

- **Complete 12-Bit ADC in SO-8**
- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 400ksps**
- Power Dissipation: 75mW (Typ)
- 72dB S/(N + D) and –80dB THD at Nyquist
- No Missing Codes over Temperature
- Nap Mode with Instant Wake-Up: 6mW
- Sleep Mode: 30μW
- High Impedance Analog Input
- Input Range (1mV/LSB): 0V to 4.096V or ±2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors (SPI and MICROWIRE™ Compatible)

## APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Digital Radio
- Spectrum Analysis
- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments

## DESCRIPTION

The LTC®1400 is a complete 400ksps, 12-bit A/D converter which draws only 75mW from 5V or ±5V supplies. This easy-to-use device comes complete with a 200ns sample-and-hold and a precision reference. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The LTC1400 has two power saving modes: Nap and Sleep. In Nap mode, it consumes only 6mW of power and can wake up and convert immediately. In the Sleep mode, it consumes 30μW of power typically. Upon power-up from Sleep mode, a reference ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The LTC1400 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL, ±1LSB DNL and 45ppm/°C drift over temperature. Guaranteed AC performance includes 70dB S/(N + D) and –76dB THD at an input frequency of 100kHz, over temperature.

The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs.

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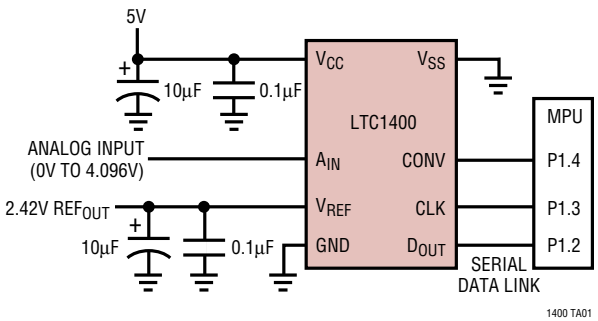
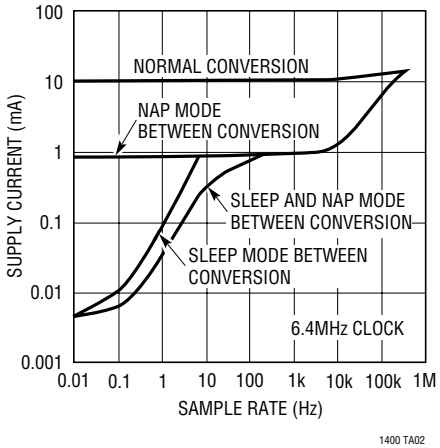
## TYPICAL APPLICATION

**Single 5V Supply, 400kHz, 12-Bit Sampling A/D Converter**




**Power Consumption vs Sample Rate**

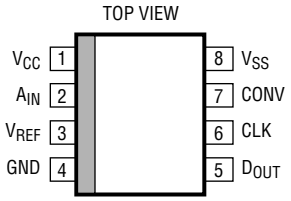


## ABSOLUTE MAXIMUM RATINGS

**(Note 1, 2)**

Supply Voltage ($V_{CC}$) ..... 7V
Negative Supply Voltage ($V_{SS}$) ..... –6V to GND
Total Supply Voltage ($V_{CC}$ to $V_{SS}$)
  Bipolar Operation Only ..... 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... –0.3V to ($V_{CC}$ + 0.3V)
  Bipolar Operation ..... ($V_{SS}$ – 0.3V) to ($V_{CC}$ + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 12V
  Bipolar Operation ..... ($V_{SS}$ – 0.3V) to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to ($V_{CC}$ + 0.3V)
  Bipolar Operation ..... ($V_{SS}$ – 0.3V) to ($V_{CC}$ + 0.3V)
Power Dissipation ..... 500mW
Operation Temperature Range
  LTC1400C ..... 0°C to 70°C
  LTC1400I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W

| ORDER PART NUMBER | S8 PART MARKING |
|---|---|
| LTC1400CS8<br>LTC1400IS8 | 1400<br>1400I |

**Order Options** Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## POWER REQUIREMENTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage (Note 6) | Unipolar<br>Bipolar | | 4.75<br>4.75 | | 5.25<br>5.25 | V<br>V |
| $V_{SS}$ | Negative Supply Voltage (Note 6) | Bipolar Only | | –2.45 | | –5.25 | V |
| $I_{CC}$ | Positive Supply Current | $f_{SAMPLE}$ = 400ksps<br>Nap Mode<br>Sleep Mode | ●<br>●<br>● | | 15<br>1.0<br>5.0 | 30<br>3.0<br>20.0 | mA<br>mA<br>µA |
| $I_{SS}$ | Negative Supply Current | $f_{SAMPLE}$ = 400ksps, $V_{SS}$ = –5V<br>Nap Mode<br>Sleep Mode | ●<br>●<br>● | | 0.3<br>0.2<br>1 | 0.6<br>0.5<br>5 | mA<br>mA<br>µA |
| $P_D$ | Power Dissipation | $f_{SAMPLE}$ = 400ksps<br>Nap Mode<br>Sleep Mode | ●<br>●<br>● | | 75<br>6<br>30 | 160<br>20<br>125 | mW<br>mW<br>µW |

## ANALOG INPUT

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Analog Input Range (Note 7) | 4.75V ≤ $V_{CC}$ ≤ 5.25V (Unipolar)<br>4.75V ≤ $V_{CC}$ ≤ 5.25V, –5.25V ≤ $V_{SS}$ ≤ –2.45V (Bipolar) | ●<br>● | | 0 to 4.096<br>±2.048 | | V<br>V |
| $I_{IN}$ | Analog Input Leakage Current | During Conversions (Hold Mode) | ● | | | ±1 | µA |
| $C_{IN}$ | Analog Input Capacitance | Between Conversions (Sample Mode)<br>During Conversions (Hold Mode) | | | 45<br>5 | | pF<br>pF |

## CONVERTER CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. With internal reference (Notes 5, 8)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution (No Missing Codes) | | ● | 12 | | | Bits |
| Integral Linearity Error | (Note 9) | ● | | | ±1 | LSB |
| Differential Linearity Error | | ● | | | ±1 | LSB |
| Offset Error | (Note 10)<br> | <br>● | | | ±6<br>±8 | LSB<br>LSB |
| Full-Scale Error | | | | | ±15 | LSB |
| Full-Scale Tempco | $I_{OUT(REF)}$ = 0 | ● | | ±10 | ±45 | ppm/°C |

## DYNAMIC ACCURACY

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_{SS}$ = –5V, $f_{SAMPLE}$ = 400kHz unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| S/(N + D) | Signal-to-Noise Plus Distortion Ratio | 100kHz Input Signal Commercial<br>Industrial | ●<br>● | 70<br>69 | 72 | | dB<br>dB |
| | | 200kHz Input Signal | | | 72 | | dB |
| THD | Total Harmonic Distortion Up to 5th Harmonic | 100kHz Input Signal<br>200kHz Input Signal | ● | | –82<br>–80 | –76 | dB<br>dB |
| | Peak Harmonic or Spurious Noise | 100kHz Input Signal<br>200kHz Input Signal | ● | | –84<br>–82 | –76 | dB<br>dB |
| IMD | Intermodulation Distortion | $f_{IN1}$ = 99.51kHz, $f_{IN2}$ = 102.44kHz<br>$f_{IN1}$ = 199.12kHz, $f_{IN2}$ = 202.05kHz | | | –82<br>–70 | | dB<br>dB |
| | Full Power Bandwidth | | | | 4 | | MHz |
| | Full Linear Bandwidth (S/(N + D) ≥ 68dB) | | | | 900 | | kHz |

## INTERNAL REFERENCE CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{REF}$ Output Voltage | $I_{OUT}$ = 0 | | 2.400 | 2.420 | 2.440 | V |
| $V_{REF}$ Output Tempco | $I_{OUT}$ = 0 | ● | | ±10 | ±45 | ppm/°C |
| $V_{REF}$ Load Regulation | 4.75V ≤ $V_{CC}$ ≤ 5.25V<br>–5.25V ≤ $V_{SS}$ ≤ 0V | | | 0.01<br>0.01 | | LSB/V<br>LSB/V |
| $V_{REF}$ Load Regulation | 0 ≤ $\|I_{OUT}\|$ ≤ 1mA | | | 2 | | LSB/mA |
| $V_{REF}$ Wake-Up Time from Sleep Mode (Note 7) | $C_{VREF}$ = 10µF | | | 4 | | ms |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = 5.25V | ● | 2.0 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = 4.75V | ● | | | 0.8 | V |
| $I_{IN}$ | Digital Input Current | $V_{IN}$ = 0V to $V_{CC}$ | ● | | | ±10 | µA |
| $C_{IN}$ | Digital Input Capacitance | | | | 5 | | pF |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = –10µA<br>$V_{CC}$ = 4.75V, $I_O$ = –200µA | <br>● | <br>4.0 | 4.7 | | V<br>V |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 160µA<br>$V_{CC}$ = 4.75V, $I_O$ = 1.6mA | <br>● | | 0.05<br>0.10 | <br>0.4 | V<br>V |
| $I_{OZ}$ | Hi-Z Output Leakage $D_{OUT}$ | $V_{OUT}$ = 0V to $V_{CC}$ | ● | | | ±10 | µA |
| $C_{OZ}$ | Hi-Z Output Capacitance $D_{OUT}$ (Note 7) | | | | 15 | | pF |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | –10 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = $V_{CC}$ | | | 10 | | mA |

## TIMING CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{SAMPLE(MAX)}$ | Maximum Sampling Frequency | (Note 6) | ● | 400 | | | kHz |
| $t_{CONV}$ | Conversion Time | $f_{CLK}$ = 6.4MHz | ● | | | 2.1 | µs |
| $t_{ACQ}$ | Acquisition Time (Unipolar Mode)<br>(Bipolar Mode $V_{SS}$ = –5V) | (Note 7) | ●<br>● | | 230<br>200 | 300<br>270 | ns<br>ns |
| $f_{CLK}$ | CLK Frequency | | ● | 0.1 | | 6.4 | MHz |
| $t_{CLK}$ | CLK Pulse Width | (Notes 7, 12) | ● | 50 | | | ns |
| $t_{WK(NAP)}$ | Time to Wake Up from Nap Mode | (Note 7) | | | 350 | | ns |
| $t_1$ | CLK Pulse Width to Return to Active Mode | | ● | 50 | | | ns |
| $t_2$ | CONV↑ to CLK↑ Setup Time | | ● | 80 | | | ns |
| $t_3$ | CONV↑ After Leading CLK↑ | | ● | 0 | | | ns |
| $t_4$ | CONV Pulse Width | (Note 11) | ● | 50 | | | ns |
| $t_5$ | Time from CLK↑ to Sample Mode | (Note 7) | | | 80 | | ns |
| $t_6$ | Aperture Delay of Sample-and-Hold | Jitter < 50ps (Note 7) | ● | | 45 | 65 | ns |
| $t_7$ | Minimum Delay Between Conversion (Unipolar Mode)<br>(Bipolar Mode $V_{SS}$ = –5V) | | ●<br>● | | 265<br>235 | 385<br>355 | ns<br>ns |
| $t_8$ | Delay Time, CLK↑ to $D_{OUT}$ Valid | $C_{LOAD}$ = 20pF | ● | | 40 | 80 | ns |
| $t_9$ | Delay Time, CLK↑ to $D_{OUT}$ Hi-Z | $C_{LOAD}$ = 20pF | ● | | 40 | 80 | ns |
| $t_{10}$ | Time from Previous Data Remains Valid After CLK↑ | $C_{LOAD}$ = 20pF | ● | 14 | 25 | | ns |
| $t_{11}$ | Minimum Time between Nap/Sleep Request to Wake Up Request | (Notes 7, 12) | ● | 50 | | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** When these pin voltages are taken below $V_{SS}$ (ground for unipolar mode) or above $V_{CC}$, they will be clamped by internal diodes. This product can handle input currents greater than 40mA below $V_{SS}$ (ground for unipolar mode) or above $V_{CC}$ without latch-up.

**Note 4:** When these pin voltages are taken below $V_{SS}$ (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 40mA below $V_{SS}$ (ground for unipolar mode) without latch-up. These pins are not clamped to $V_{CC}$.

**Note 5:** $V_{CC}$ = 5V, $f_{SAMPLE}$ = 400kHz, $t_r$ = $t_f$ = 5ns unless otherwise specified.

**Note 6:** Recommended operating conditions.

**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

**Note 9:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

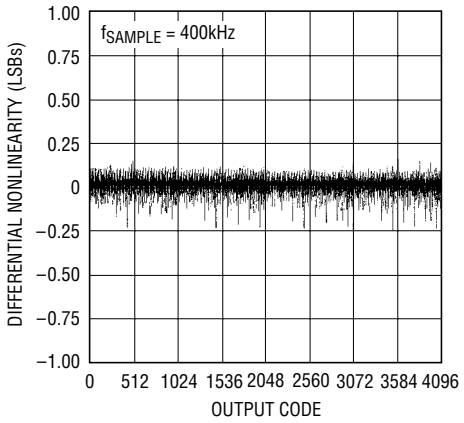
**Note 10:** Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

**Note 11:** The rising edge of CONV starts a conversion. If CONV returns low at a bit decision point during the conversion, it can create small errors. For best performance ensure that CONV returns low either within 120ns after conversion starts (i.e., before the first bit decision) or after the 14 clock cycle. (Figure 13 Timing Diagram).

**Note 12:** If this timing specification is not met, the device may not respond to a request for a conversion. To recover from this condition a NAP request is required.

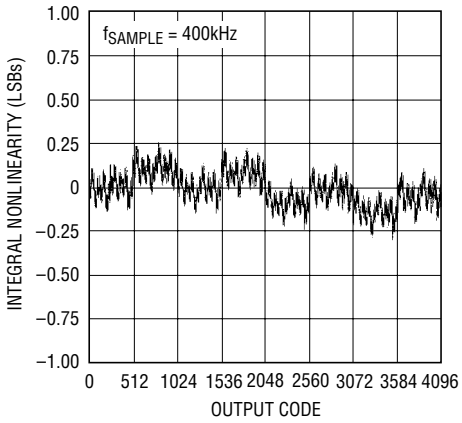
# TYPICAL PERFORMANCE CHARACTERISTICS

### Differential Nonlinearity vs Output Code



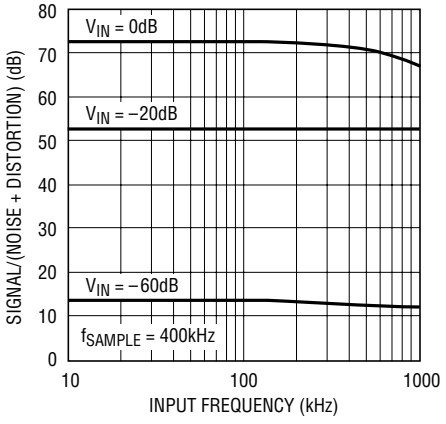

1400 TPC01

### Integral Nonlinearity vs Output Code



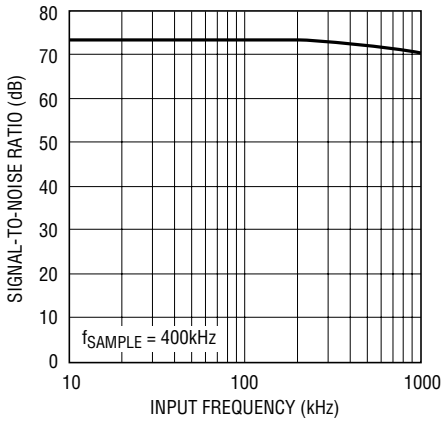

1400 TPC02

### S/(N + D) vs Input Frequency and Amplitude



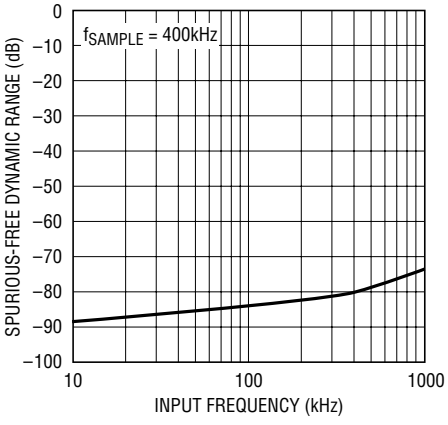

1400 TPC06

### Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



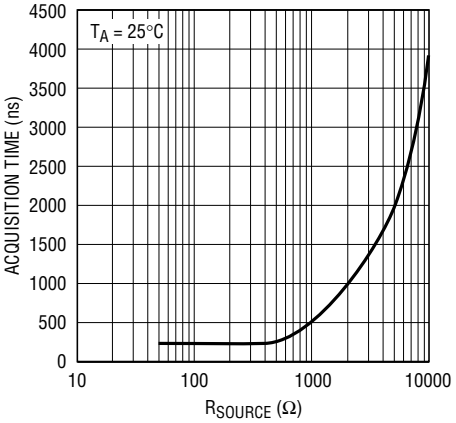

1400 TPC07

### Peak Harmonic or Spurious Noise vs Input Frequency



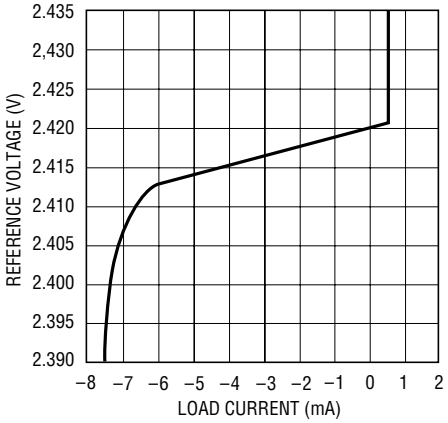

1400 TPC08

### Acquisition Time vs Source Impedance



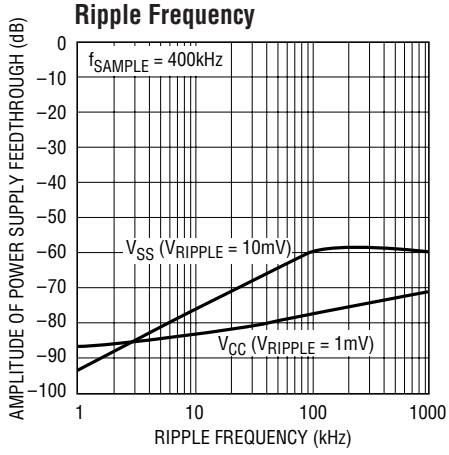

1400 TPC05

### Reference Voltage vs Load Current



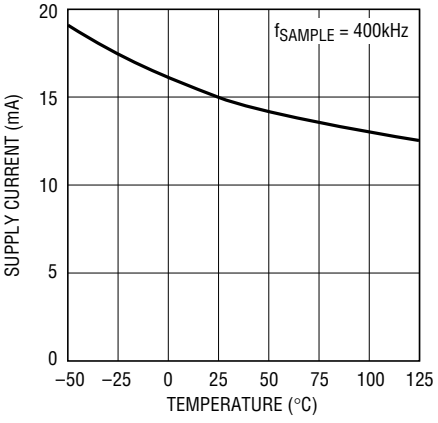

1400 TPC03

### Power Supply Feedthrough vs Ripple Frequency




1400 TPC07.5

### Supply Current vs Temperature




1400 TPC04

## PIN FUNCTIONS

**$V_{CC}$ (Pin 1):** Positive Supply, 5V. Bypass to GND (10μF tantalum in parallel with 0.1μF ceramic).

**$A_{IN}$ (Pin 2):** Analog Input. 0V to 4.096V (Unipolar), ±2.048V (Bipolar).

**$V_{REF}$ (Pin 3):** 2.42V Reference Output. Bypass to GND (10μF tantalum in parallel with 0.1μF ceramic).

**GND (Pin 4):** Ground. GND should be tied directly to an analog ground plane.

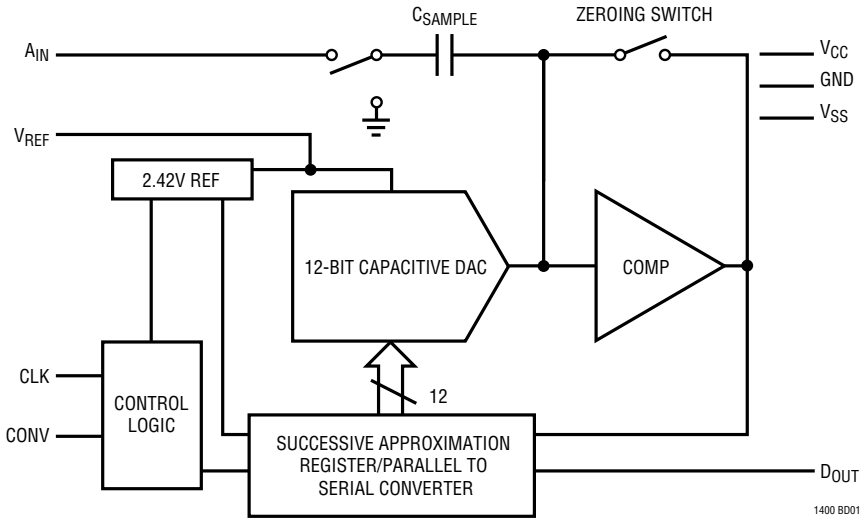
**$D_{OUT}$ (Pin 5):** The A/D conversion result is shifted out from this pin.

**CLK (Pin 6):** Clock. This clock synchronizes the serial data transfer. A minimum CLK pulse of 50ns will cause the ADC to wake up from Nap or Sleep mode.

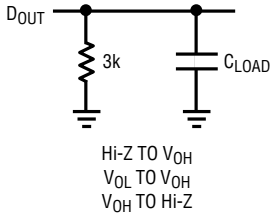
**CONV (Pin 7):** Conversion Start Signal. This active high signal starts a conversion on its rising edge. Keeping CLK low and pulsing CONV two/four times will put the ADC into Nap/Sleep mode.

**$V_{SS}$ (Pin 8):** Negative Supply. –5V for bipolar operation. Bypass to GND with 0.1μF ceramic. $V_{SS}$ should be tied to GND for unipolar operation.

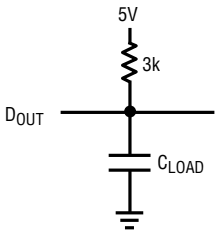
## FUNCTIONAL BLOCK DIAGRAM




## TEST CIRCUITS




Hi-Z TO $V_{OH}$
$V_{OL}$ TO $V_{OH}$
$V_{OH}$ TO Hi-Z




Hi-Z TO $V_{OL}$
$V_{OH}$ TO $V_{OL}$
$V_{OL}$ TO Hi-Z

1400 TC01

# APPLICATIONS INFORMATION

## Conversion Details

The LTC1400 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output based on a precision internal reference. The control logic provides easy interface to microprocessors and DSPs through 3-wire connections.

A rising edge on the CONV input starts a conversion. At the start of a conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the $A_{IN}$ input connects to the sample-and-hold capacitor during the acquired phase and the comparator offset is nulled by the feedback switch. In this acquire phase, it typically takes 200ns for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switches connect $C_{SAMPLE}$ to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the $A_{IN}$ input charge. The SAR contents (a 12-bit data word) which represent the input voltage, are output through the serial pin $D_{OUT}$.

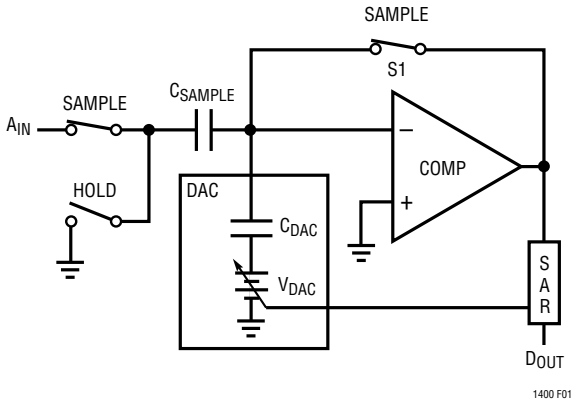



**Figure 1. $A_{IN}$ Input**

## Dynamic Performance

The LTC1400 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2a shows a typical LTC1400 FFT plot.

## Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from DC to half the sampling frequency. Figure 2a shows a typical spectral content with a 400kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 200kHz as shown in Figure 2b.

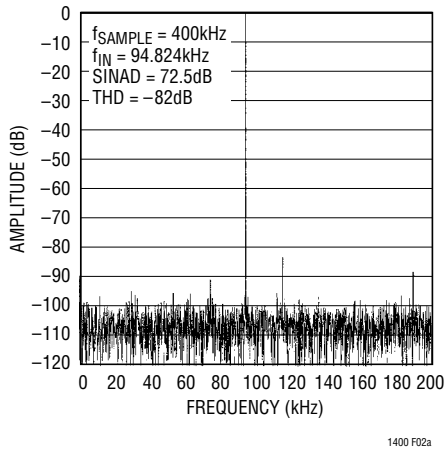



**Figure 2a. LTC1400 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency in Bipolar Mode**

## Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the effective resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = \frac{S/(N+D) - 1.76}{6.02}$$

## APPLICATIONS INFORMATION

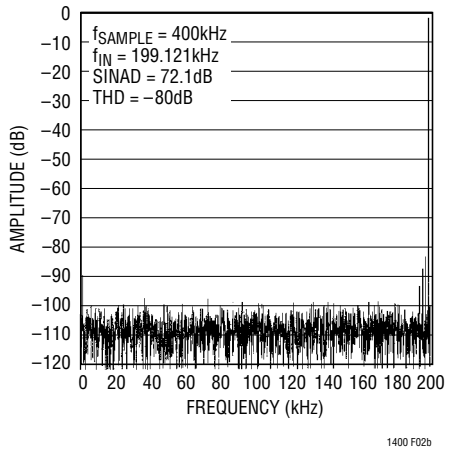



**Figure 2b. LTC1400 Nonaveraged, 4096 Point FFT Plot with 200kHz Input Frequency in Bipolar Mode**

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 400kHz, the LTC1400 maintains very good ENOBs up to the Nyquist input frequency of 200kHz (refer to Figure 3).

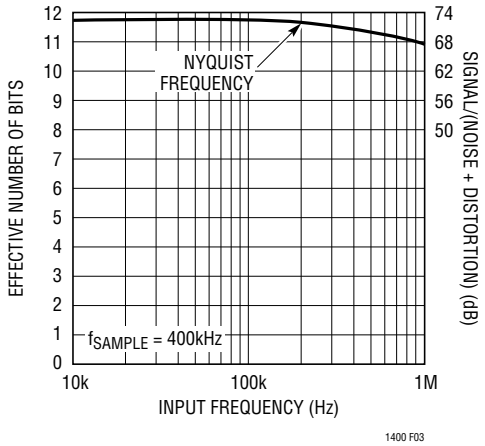



**Figure 3. Effective Bits and Signal-to-Noise + Distortion vs Input Frequency in Bipolar Mode**

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1400 has good distortion performance up to the Nyquist frequency and beyond.

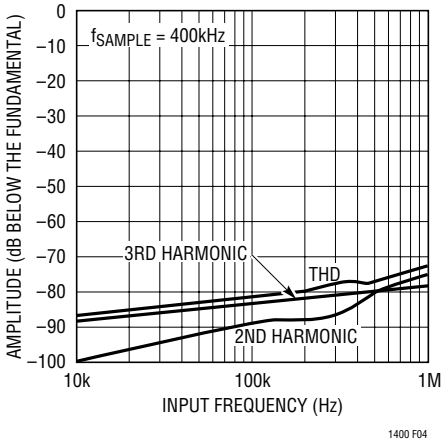



**Figure 4. Distortion vs Input Frequency in Bipolar Mode**

### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms includes (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula.

$$IMD(fa \pm fb) = 20\log\frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

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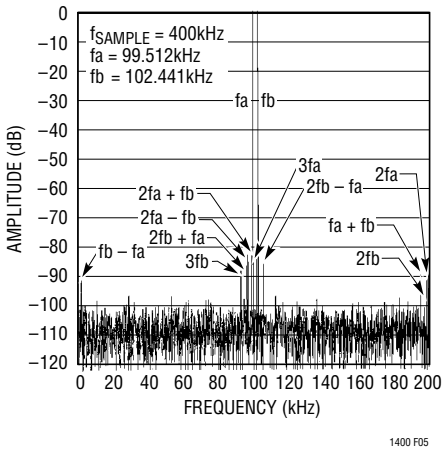


**Figure 5. Intermodulation Distortion Plot in Bipolar Mode**

Figure 5 shows the IMD performance at a 100kHz input.

### Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

### Full Power and Full Linear Bandwidth

The full power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1400 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

### Driving the Analog Input

The analog input of the LTC1400 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of a conversion. During conversion, the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 200ns to small load current transient will allow maximum speed operation. If a slower op amp is used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's $A_{IN}$ input include the LT®1360 and the LT1363 op amps.

LTC1400 comes with a built-in unipolar/bipolar detection circuit. If $V_{SS}$ potential is forced below GND, the internal circuitry will automatically switch to bipolar mode.

The following list is a summary of the op amps that are suitable for driving the LTC1400, more detailed information is available in the Linear Technology databooks or the Linear Technology Website.

**LT1215/LT1216:** Dual and quad 23MHz, 50V/μs single supply op amps. Single 5V to ±15V supplies, 6.6mA specifications, 90ns settling to 0.5LSB.

**LT1223:** 100MHz video current feedback amplifier. ±5V to ±15V supplies, 6mA supply current. Low distortion up to and above 400kHz. Low noise. Good for AC applications.

**LT1227:** 140MHz video current feedback amplifier. ±5V to ±15V supplies, 10mA supply current. Lowest distortion at frequencies above 400kHz. Low noise. Best for AC applications.

**LT1229/LT1230:** Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, 6mA supply current each amplifier. Low noise. Good AC specs.

**LT1360:** 37MHz voltage feedback amplifier. ±5V to ±15V supplies. 3.8mA supply current. Good AC and DC specs. 70ns settling to 0.5LSB.

**LT1363:** 50MHz, 450V/μs op amps. ±5V to ±15V supplies. 6.3mA supply current. Good AC and DC specs. 60ns settling to 0.5LSB.

**LT1364/LT1365:** Dual and quad 50MHz, 450V/μs op amps. ±5V to ±15V supplies, 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

### Internal Reference

The LTC1400 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory

## APPLICATIONS INFORMATION

trimmed to 2.42V. It is internally connected to the DAC and is available at Pin 3 to provide up to 1mA of current to an external load. For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic). The $V_{REF}$ pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The $V_{REF}$ pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should not be driven to more than 5V.

Figure 6 shows an LT1360 op amp driving the reference pin. Figure 7 shows a typical reference, the LT1019A-5 connected to the LTC1400. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-5) and a ±4.231V full scale. If $V_{REF}$ is forced lower than 2.42V, the REFRDY bit in the serial data output will be forced to low.

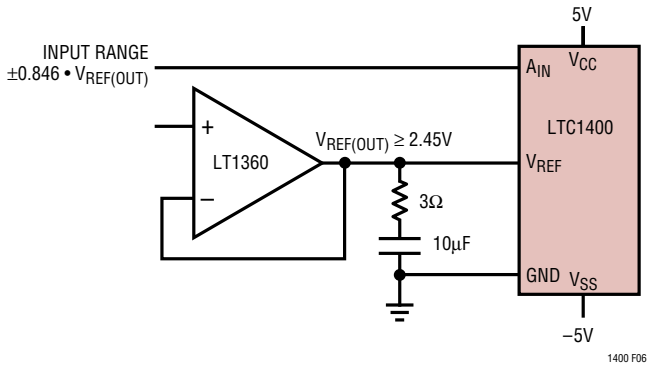


**Figure 6. Driving the $V_{REF}$ with the LT1360 Op Amp**

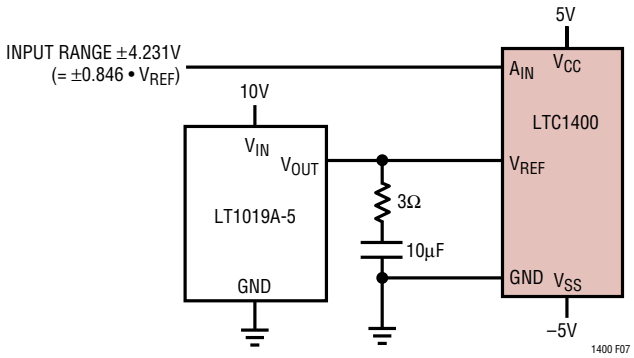


**Figure 7. Supplying a 5V Reference Voltage to the LTC1400 with the LT1019A-5**

### Unipolar/Bipolar Operation and Adjustment

Figure 8 shows the ideal input/output characteristics for the LTC1400. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, … FS – 1.5LSB). The output code is straight binary with 1LSB = 4.096V/4096 = 1mV. Figure 9 shows the input/output transfer characteristics for the bipolar mode in two's complement format.

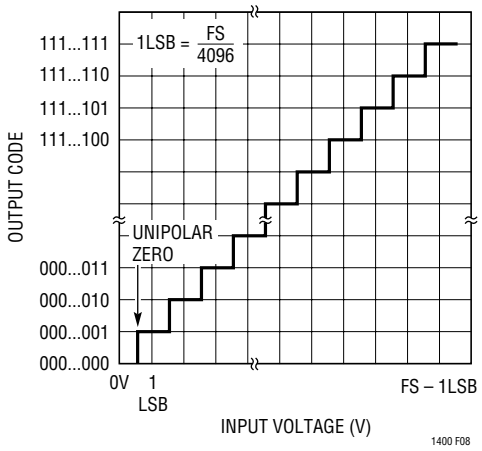


**Figure 8. LTC1400 Unipolar Transfer Characteristics**

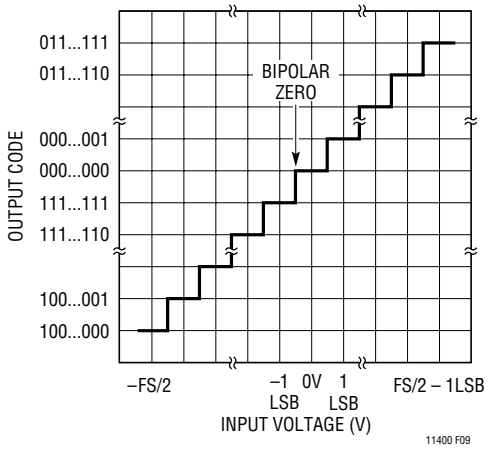


**Figure 9. LTC1400 Bipolar Transfer Characteristics**

### Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Figure 10a shows the extra components required for full-scale

## APPLICATIONS INFORMATION

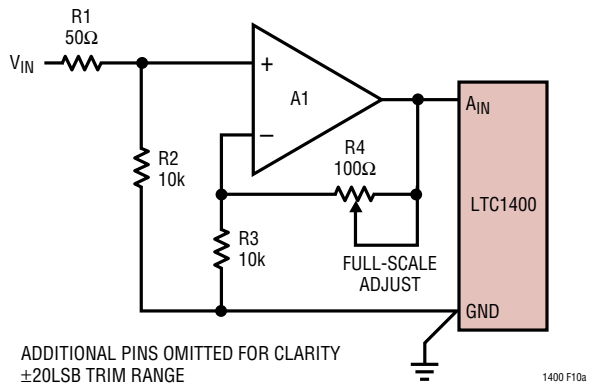


**Figure 10a. LTC1400 Full-Scale Adjust Circuit**

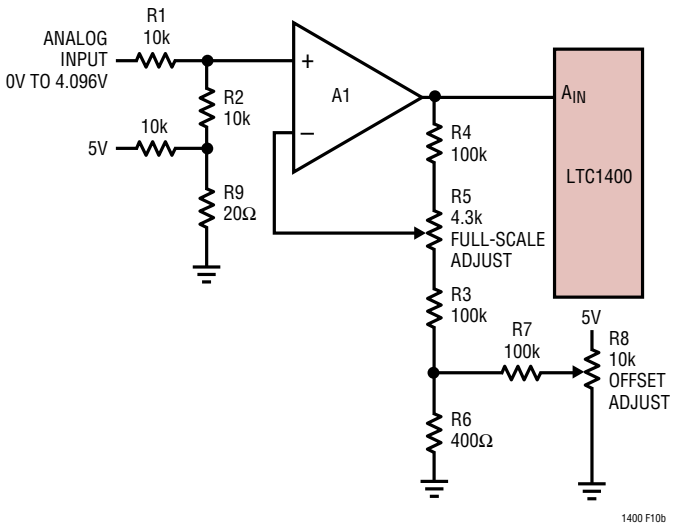


**Figure 10b. LTC1400 Offset and Full-Scale Adjust Circuit**

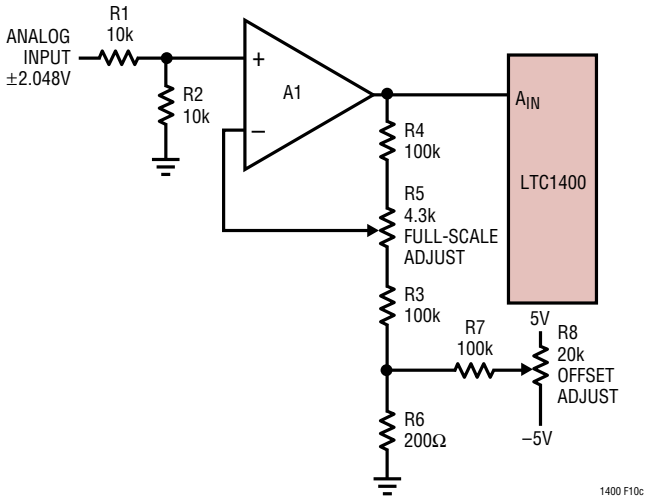


**Figure 10c. LTC1400 Bipolar Offset and Full-Scale Adjust Circuit**

error adjustment. Figure 10b shows offset and full-scale adjustment. Offset error must be adjusted before full-scale error. Zero offset is achieved by applying 0.5mV (i.e., 0.5LSB) at the input and adjusting the offset trim until the LTC1400 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 4.0945V (FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1400 output code flickers between 1111 1111 1110 and 1111 1111 1111.

### Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Bipolar offset error adjustment is achieved by applying an input voltage of –0.5mV (–0.5LSB) to the input in Figure 10c and adjusting the op amp until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

### Board Layout and Bypassing

To obtain the best performance from the LTC1400, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by GND.

High quality tantalum and ceramic bypass capacitors should be used at the $V_{CC}$ and $V_{REF}$ pins as shown in the Typical Application on the first page of this data sheet. For the bipolar mode, a 0.1μF ceramic provides adequate bypassing for the $V_{SS}$ pin. For optimum performance, a 10μF surface mount AVX capacitor with a 0.1μF ceramic is recommended for the $V_{CC}$ and $V_{REF}$ pins. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible. In unipolar mode operation, $V_{SS}$ should be isolated from any noise source before shorting to the GND pin.

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Input signal leads to $A_{IN}$ and signal return leads from GND (Pin 4) should be kept as short as possible to minimize noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible.

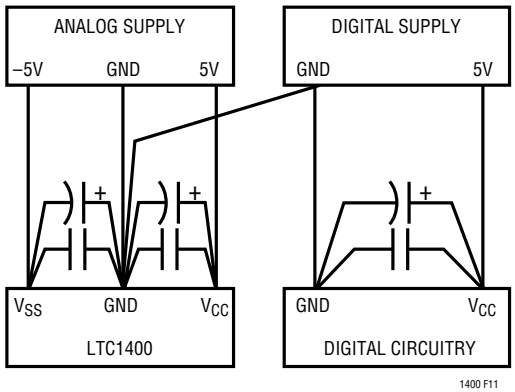


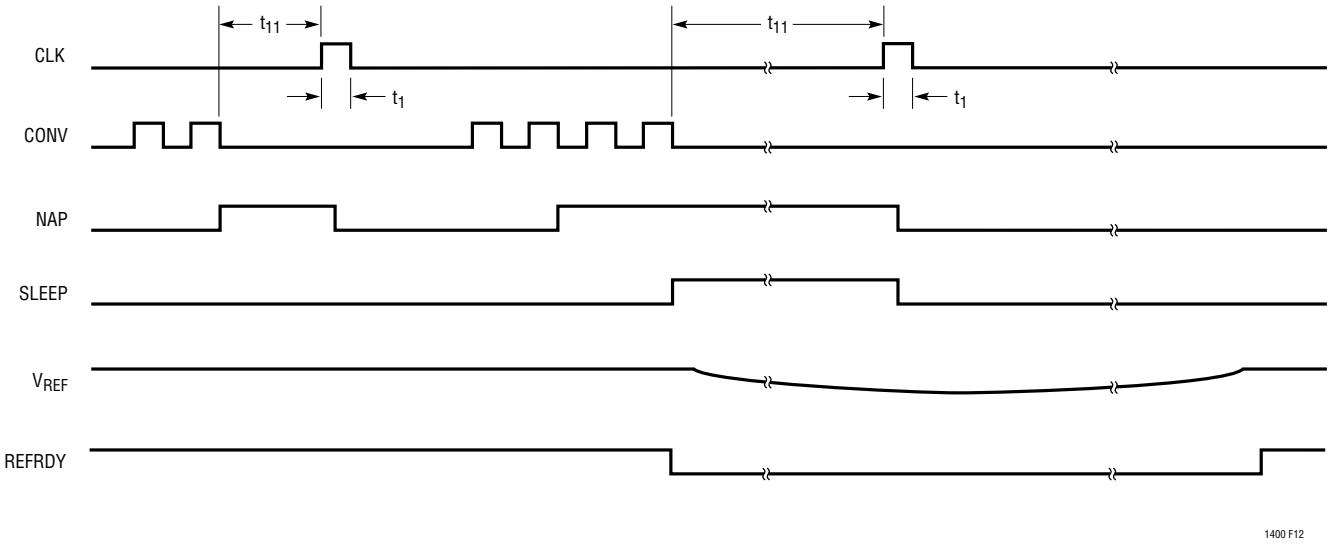

**Figure 11. Power Supply Connection**

Figure 11 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1400 GND pin. The ground return from the LTC1400 Pin 4 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

### Power-Down Mode

Upon power-up, the LTC1400 is initialized to the active state and is ready for conversion. However, the chip can be easily placed into the Nap or Sleep mode by exercising the right combination of CLK and CONV signal. In the Nap mode all power is off except the internal reference, which is still active and provides 2.42V output voltage to the other circuitry. In this mode, the ADC draws only 6mW of power instead of 75mW (for minimum power, the logic inputs must be within 500mV of the supply rails). The wake-up time from the Nap mode to the active mode is 350ns.




NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS. REFRDY APPEARS AS A BIT IN THE $D_{OUT}$ WORD.

**Figure 12. Nap Mode and Sleep Mode Waveforms**

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In the Sleep mode, power consumption is reduced to a minimum by cutting off the supply to all internal circuitry including the reference. Figure 12 shows the ways to power down the LTC1400. The chip can enter the Nap mode by keeping the CLK signal low and pulsing the CONV signal twice. For Sleep mode operation, CONV signal should be pulsed four times while CLK is kept low.

The LTC1400 can be returned to active mode easily. The rising edge of CLK will wake-up the LTC1400. During the transition from Sleep mode to active mode, the $V_{REF}$ voltage ramp-up time is a function of the loading conditions. With a 10µF bypass capacitor, the wake-up time from Sleep mode is typically 4ms. A REFRDY signal will be activated once the reference has settled and is ready for an A/D conversion. This REFRDY bit is output to the $D_{OUT}$ pin before the rest of the A/D converted code.

### Digital Interface

The digital interface requires only three digital lines. CLK and CONV are both inputs, and the $D_{OUT}$ output provides the conversion result in serial form.

Figure 13 shows the digital timing diagram of the LTC1400 during the A/D conversion. The CONV rising edge starts the conversion. Once initiated, it can not be restarted until the conversion is completed. If the time from CONV signal to CLK rising edge is less than $t_2$, the digital output will be delayed by one clock cycle.

The digital output data is updated on the rising edge of the CLK line. $D_{OUT}$ data should be captured by the receiving system on the rising CLK edge. Data remains valid for a minimum time of $t_{10}$ after the rising CLK edge to allow capture to occur.

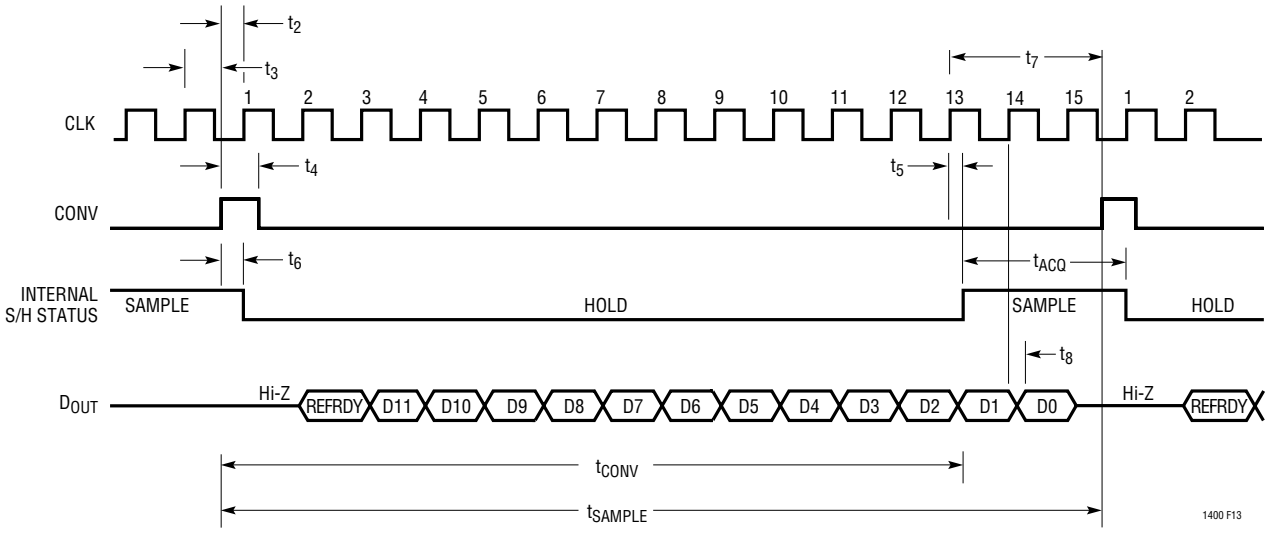



**Figure 13. ADC Digital Timing Diagram**

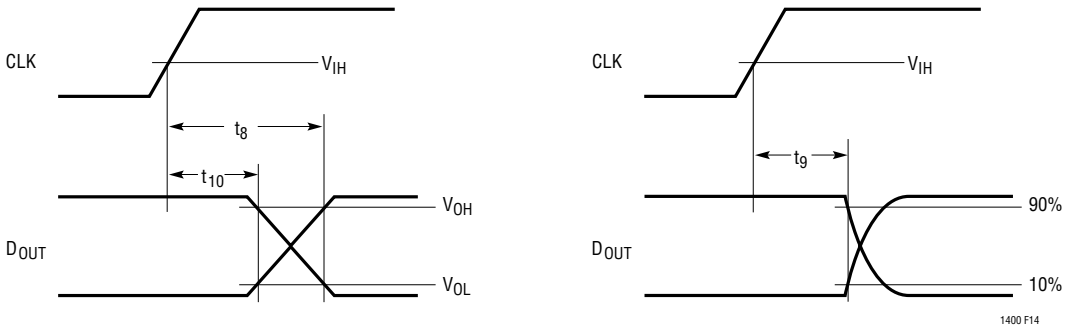
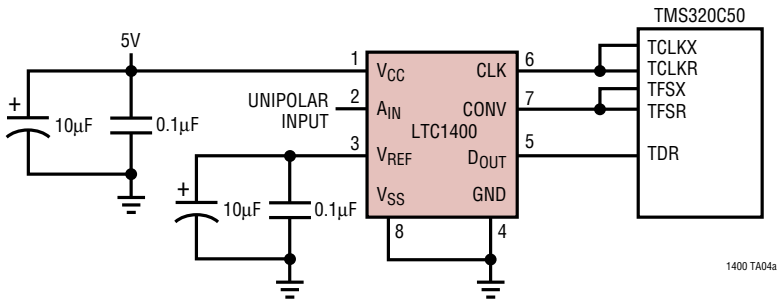


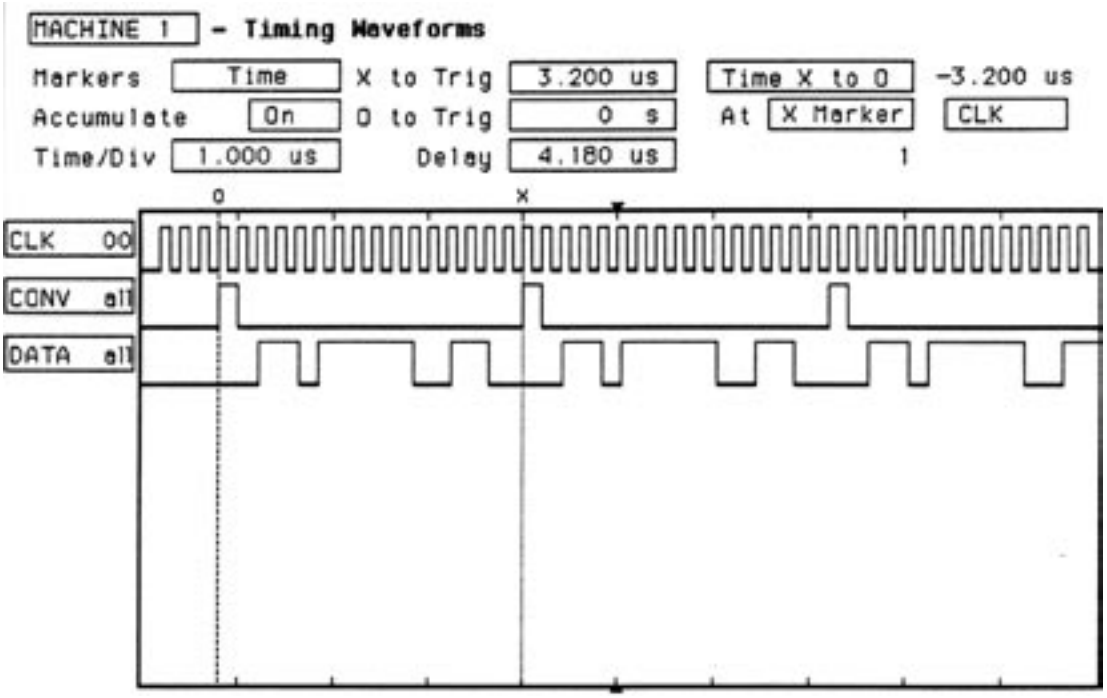

**Figure 14. CLK to $D_{OUT}$ Delay**

## TYPICAL APPLICATIONS

**Hardware Interface to TMS320C50's TDM Serial Port (Frame Sync is Generated from TFSX)**




**Logic Analyzer Waveforms Show 3.2µs Throughput Rate (Input Voltage = 3.046V, Output Code = 1011 1110 0110 = $3046_{10}$)**




**Data from LTC1400 Loaded into TMS320C50's TRCV Register**

| X | RDY | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

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**Data Stored in TMS320C50's Memory (in Right Justified Format)**

| 0 | 0 | 0 | RDY | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

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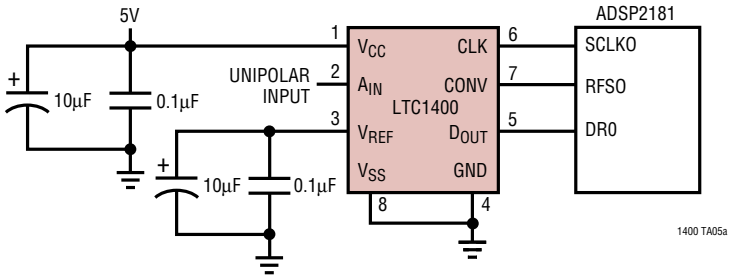
# TYPICAL APPLICATIONS

**TMS320C50 Code for Circuit**

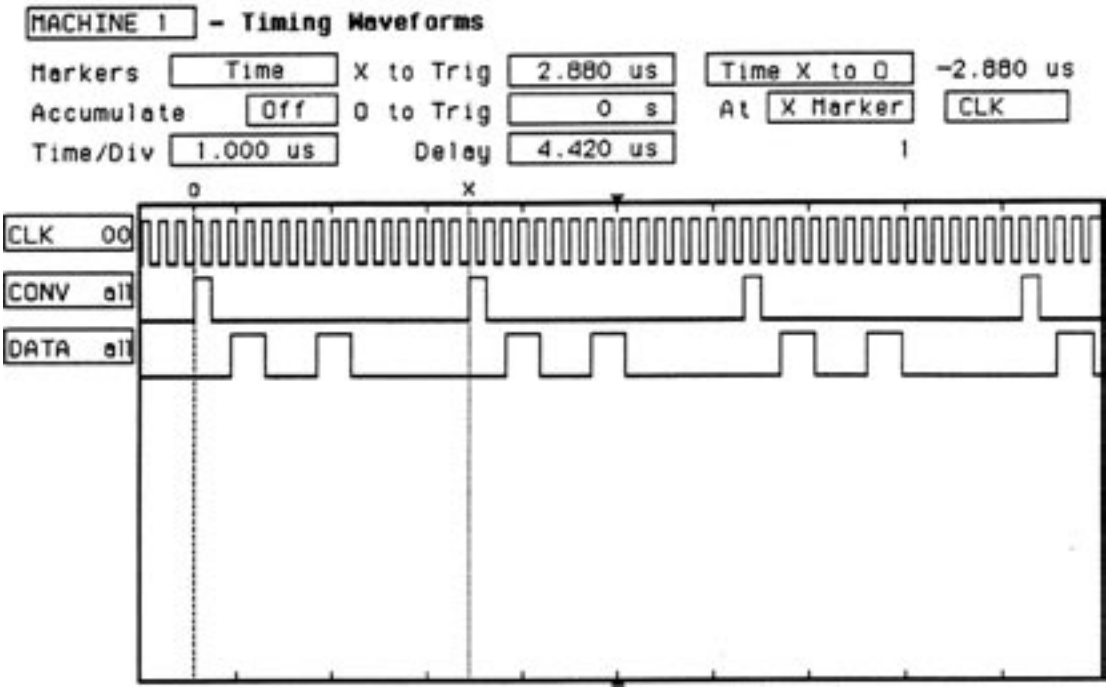
```
THIS PROGRAM DEMONSTRATES LTC1400 INTERFACE TO TMS320C50
FRAME SYNC PULSE IS GENERATED FROM TFSX

*Initialization*
    .mmregs                     ; Defines global symbolic names
;- - Initialized data memory to zero
        .ds     0F00h           ; Initialize data to zero
DATA0   .word   0               ; Begin sample data location
DATA1   .word   0               ; .
DATA2   .word   0               ; Location of data
DATA3   .word   0               ; .
DATA4   .word   0               ; .
DATA5   .word   0               ; End sample data location
;- - Set up the ISR vector
        .ps     080Ah           ; Serial ports interrupts
rint :  B       RECEIVE         ; 0A;
xint :  B       TRANSMIT        ; 0C;
trnt :  B       TREC            ; 0E;
txnt :  B       TTRANX          ; 10;
;- - Setup the reset vector
    .ps 0A00h
    .entry
START:

*TMS32C050 Initialization*
    SETC  INTM          ; Temporarily disable all interrupts
    LDP   #0            ; Set data page pointer to zero
    OPL   #0834h, PMST  ; Set up the PMST status and control register
    LACC  #0
    SAMM CWSR           ; Set software wait state to 0
    SAMM PDWSR          ;

*Configure Serial Port*
    SPLK  #0038h, TSPC  ; Set TDM Serial Port
                        ; TDM = 0 Stand Alone mode
                        ; DLB = 0 Not loop back
                        ; FO = 0 16  Bits
                        ; FSM = 1 Burst Mode
                        ; MCM = 1 CLKX is generated internally
                        ; TXM = 1 FSX as output pin
                        ; Put serial port into reset
                        ; (XRST = RRST =0)
    SPLK  #00F8h, TSPC  ; Take Serial Port out of reset
                        ; (XRST = RRST = 1)
    SPLK  #0FFFFh, IFR  ; Clear all the pending interrupts

*Start Serial Communication*
    SACL  TDXR          ; Generate frame sync pulse
    SPLK  #040h, IMR    ; Turn on TRNT receiver interrupt
    CLRC  INTM          ; Enable interrupt
    CLRC  SXM           ; For Unipolar input, set for right shift
                        ; with no sign extension
    MAR   *AR7          ; Load the auxiliary register pointer with seven
    LAR   AR7, #0F00h   ; Load the auxiliary register seven with #0F00h
                        ; as the begin address for data storage
WAIT:   NOP             ; Wait for a receive interrupt
        NOP             ;
        NOP             ;
    SACL  TDXR          ; !! regenerate the frame sync pulse
    B     WAIT          ;
; - - - - - - - end of main program - - - - - - - - - - ;

*Receiver Interrupt Service Routine*
TREC:
    LAMM TRCV           ; Load the data received from LTC1400
    SFR                 ; Shift right two times
    SFR                 ;
    AND   #1FFFh, 0     ; ANDed with #1FFFh
                        ; For converting the data to right
                        ; justified format
                        ;
    SACL  *+, 0         ; Write to data memory pointed by AR7 and
                        ; increase the memory address by one
    LACC  AR7           ;
    SUB   #0F05h,0      ; Compare to end sample address #0F05h
    BCND  END_TRCV, GEQ ; If the end sample address has exceeded jump
                          to END_TRCV
                        ;
    SPLK  #040h, IMR    ; Else Re-enable the TRNT receive interrupt
    RETE                ; Return to main program and enable interrupt

*After Obtained the Data from LTC1400, Program Jump to END_TRCV*
END_TRCV:
    SPLK  #002h, IMR    ; Enable INT2 for program to halt
    CLRC  INTM
SUCCESS:
    B     SUCCESS

*Fill the Unused Interrupt with RETE, to avoid program get "lost"*
TTRANX:
    RETE
RECEIVE:
    RETE
TRANSMIT:
    RETE
INT2:
    B halt              ; Halts the running CPU
```

## TYPICAL APPLICATIONS

**LTC1400 Interface to ADSP2181's SPORT0 (Frame Sync is Generated from RFS0)**




**Logic Analyzer Waveforms Show 2.88µs Throughput Rate (Input Voltage = 2.240V, Output Code = 1000 1100 0000 = $2240_{10}$)**




**Data from LTC1400 (Normal Mode)**

| X | RDY | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

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**Data Stored in ADSP2181's Memory (Normal Mode, SLEN = D)**

| 0 | 0 | 0 | RDY | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1400 TA05d

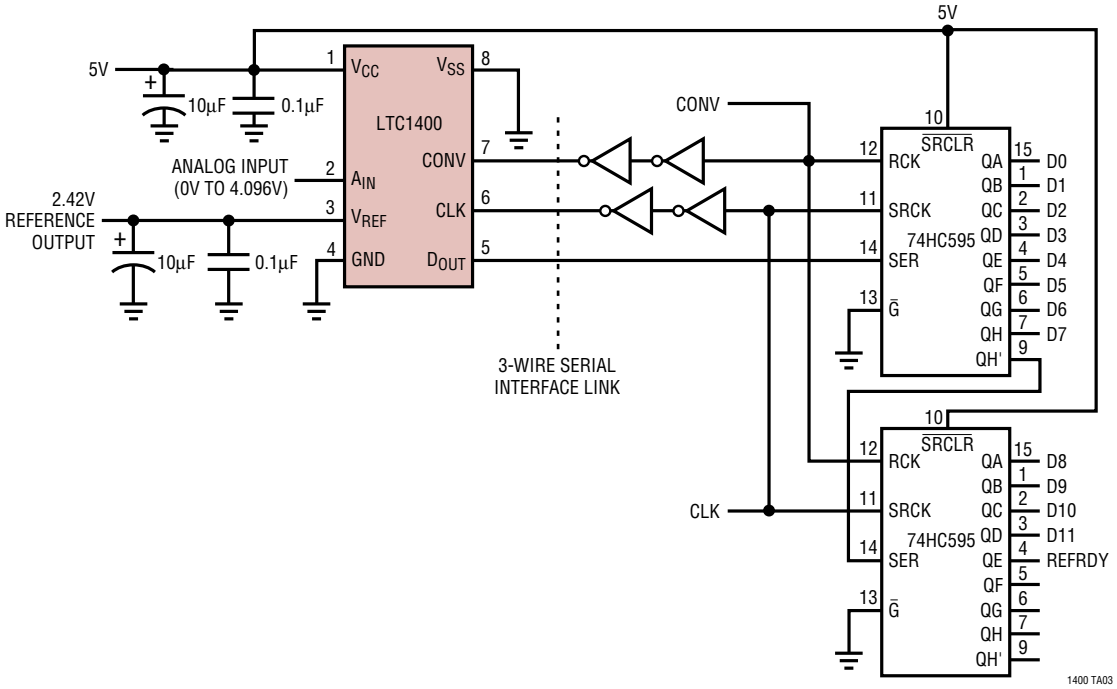
# TYPICAL APPLICATIONS

**ADSP2181 Code for Circuit**

```
THIS PROGRAM DEMONSTRATES LTC1400 INTERFACE TO ADSP-2181
FRAME SYNC PULSE IS GENERATED FROM RFS0

/*Section 1: Initialization*/
.module/ram/abs = 0 adspltc;    /*define the program module*/
   jump start;              /*jump over interrupt vectors*/
   nop; nop; nop;
   rti; rti; rti; rti;      /*code vectors here upon IRQ2 int*/
   rti; rti; rti; rti;      /*code vectors here upon IRQL1 int*/
   rti; rti; rti; rti;      /*code vectors here upon IRQL0 int*/
   rti; rti; rti; rti;      /*code vectors here upon SPORT0 TX int*/
   ax0 = rx0;               /*Section 5*/
   dm (0x2000) = ax0;       /*begin of SPORT0 receive interrupt*/
   rti;                     /* */
                            /* */
                            /*end of SPORT0 receive interrupt*/
   rti; rti; rti; rti;      /*code vectors here upon /IRQE int*/
   rti; rti; rti; rti;      /*code vectors here upon BDMA interrupt*/
   rti; rti; rti; rti;      /*code vectors here upon SPORT1 TX (IRQ1) int*/
   rti; rti; rti; rti;      /*code vectors here upon SPORT1 RX (IRQ0) int*/
   rti; rti; rti; rti;      /*code vectors here upon TIMER int*/
   rti; rti; rti; rti;      /*code vectors here upon POWER DOWN int*/

/*Section 2: Configure SPORT0*/
start:
/*to configure SPORT0 control reg*/
                            /*SPORT0 address = 0X3FF6*/
                            /*RFS is used for frame sync generation*/
                            /*RFS0 is internal, TFS is not use*/
                            /*bit 0-3 = Slen*/
                            /*F = 15 = 1111*/
                            /*E = 14 = 1110*/
                            /*D = 13 = 1101*/
                            /*bit 4,5 data type right justified zero filled MSB*/
                            /*bit 6 INVRFS = 0*/
                            /*bit 7 INVTFS = 0*/
                            /*bit 8 IRFS = 1 receive internal frame sync*/
                            /*bit 9,10,11 are for TFS (don't care)*/
                            /*bit 12 TFSW = 1 receive is Normal mode*/
                            /*bit 13 RTFS = 1 receive is framed mode*/
                            /*bit 14 ISCLK internal = 1*/
                            /*bit 15 multichannel mode = 0*/
   ax0 = 0x6B0D;            /*normal mode, bit12 = 0*/
                            /*if alternate mode bit12 = 1, ax0 = 0x7F0E*/
   dm (0x3FF6) =ax0;

/*Section 3: configure CLKDIV and RFSDIV, setup interrupts*/
/*to configure CLKDIV reg*/
    ax0 = 2;
    dm(0x3FF5) = ax0;       /*set the serial clock divide modulus reg
                            SCLKDIV*/
                            /*the input clock frequency = 16.67MHz*/
                            /*CLKOUT frequency = 2x = 33MHz*/
                            /*SCLK= 1/2*CLKOUT*1/(SCLKDIV+1)*/
                            /*for SCLKDIV = 2, SCLK = 33/6 = 5.5MHz*/
/*to Configure RFSDIV*/
    ax0 = 15;               /*set the RFSDIV reg = 15*/
                            /*= > the frame sync pulse for every 16 SCLK*/
                            /*if frame sync pulse in every 15 SCLK, ax0 = 14*/
    dm(0x3FF4) = ax0;
/*to setup interrupt*/
    ifc = 0x0066;           /*clear any extraneous SPORT interrupts*/
    icntl = 0;              /*IRQXB = level sensitivity*/
                            /*disable nesting interrupt*/
    imask= 0x0020;          /*bit 0 = timer int = 0*/
                            /*bit 1 = SPORT1 or IRQ0B int = 0*/
                            /*bit 2 = SPORT1 or IRQ1B int = 0*/
                            /*bit 3 = BDMA int = 0*/
                            /*bit 4 = IRQEB int = 0*/
                            /*bit 5 = SPORT0 receive int = 1*/
                            /*bit 6 = SPORT0 transmit int = 0*/
                            /*bit 7 = IRQ2B int = 0*/
                            /*enable SPORT0 receive interrupt*/

/*Section 4: Configure System Control Register and Start Communication*/
/*to configure system control reg*/
    ax0 = dm(0x3FFF);       /*read the system control reg*/
    ay0 = 0xFFF0;
    ar = ax0 AND ay0;       /*set wait state to zero*/
    ay0 = 0x1000;
    ar = ar OR ay0;         /*bit12 = 1, enable SPORT0*/
    dm(0x3FFF) = ar;
/*frame sync pulse regenerated automatically*/
    cntr = 5000;
do waitloop until ce;
    nop;
    nop;
    nop;
    nop;
    nop;
    nop;
waitloop: nop;
    rts;
.endmod;
```

## TYPICAL APPLICATIONS

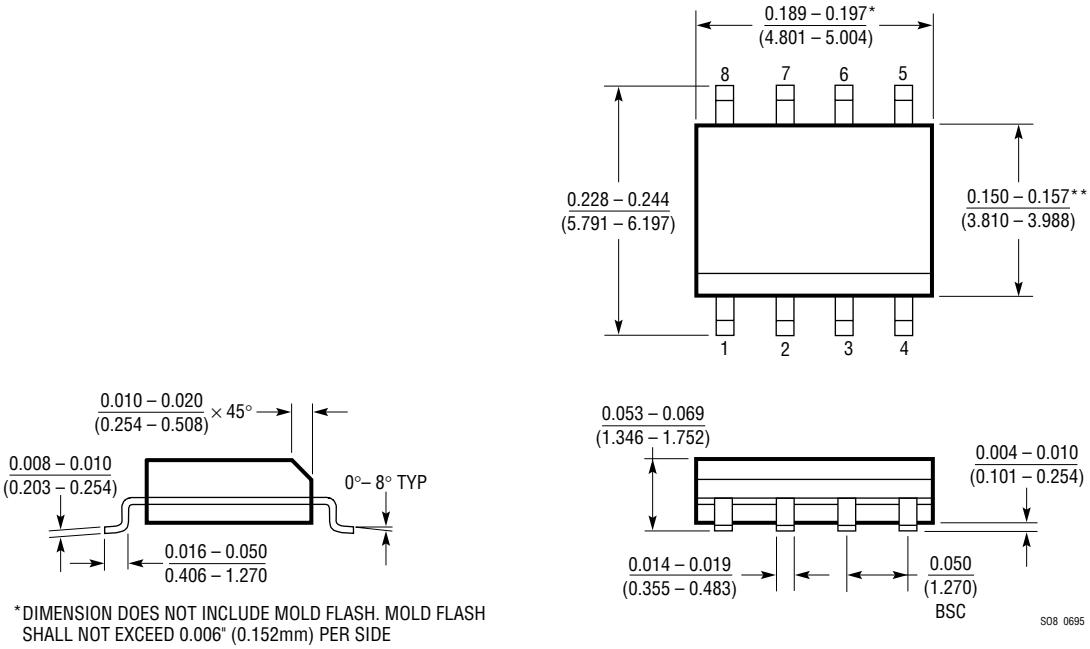
**Quick Look Circuit for Converting Data to Parallel Format**



## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**S8 Package**
**8-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

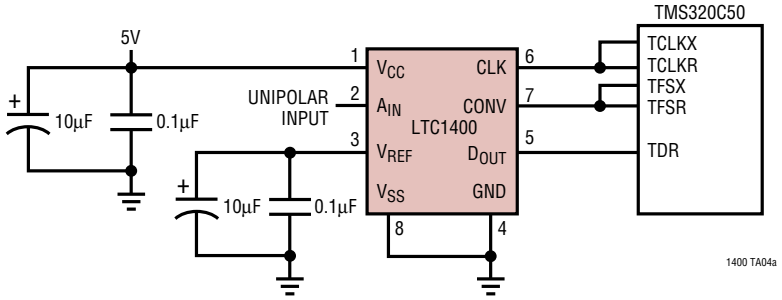


LINEAR TECHNOLOGY

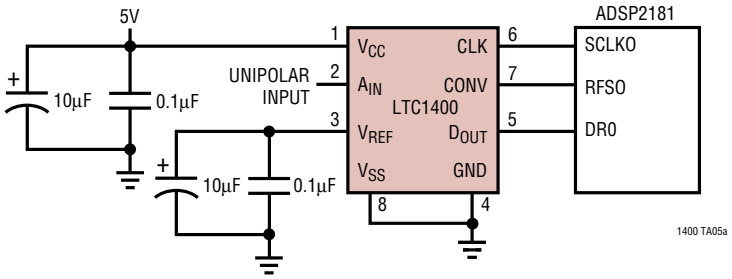
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATIONS

**LTC1400 Interface to TMS320C50**




**LTC1400 Interface to ADSP2181**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1285/LTC1288 | 12-Bit, 3V, 7.5/6.6ksps, Micropower Serial ADCs | 0.48mW, 1 or 2 Channel Input, SO-8 |
| LTC1286/LTC1298 | 12-Bit, 5V 12.5/11.16ksps, Micropower Serial ADCs | 1.25mW, 1 or 2 Channel Input, SO-8 |
| LTC1290 | 12-Bit, 50ksps 8-Channel Serial ADC | 5V or ± 5V Input Range, 30mW, Full-duplex |
| LTC1296 | 12-Bit, 46.5ksps 8-Channel Serial ADC | 5V or ± 5V Input Range, 30mW, Half-duplex |
| LTC1403/LTC1403A | 12-/14-Bit, 2.8Msps Serial ADCs | 3V, 15mW, MSOP Package |
| LTC1407/LTC1407A | 12-/14-Bit, 3Msps Simultaneous Sampling ADCs | 3V, 14mW, 2-Channel Differential Inputs, MSOP Package |
| LTC1417 | 14-Bit, 400ksps Serial ADC | 5V or ± 5V, 20mW, Internal Reference, SSOP-16 |
| LTC1609 | 16-Bit, 200ksps Serial ADC | 5V, Configurable Bipolar or Unipolar Inputs to ±10V |
| LTC1860L/LTC1861L | 12-Bit, 3V, 150ksps Serial ADCs | 1.22mW, 1-/2-Channel Inputs, MSOP and SO-8 |
| LTC1860/LTC1861 | 12-Bit, 5V, 250ksps Serial ADCs | 4.25mW, 1-/2-Channel Inputs, MSOP and SO-8 |
| LTC1864L/LTC1864L | 16-Bit, 3V, 150KSPS Serial ADCs | 1.22mW, 1-/2-Channel Inputs, MSOP and SO-8 |
| LTC1864/LTC1864 | 16-Bit, 5V, 250ksps Serial ADCs | 4.25mW, 1-/2-Channel Inputs, MSOP and SO-8 |

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LT 0606 REV A • PRINTED IN USA

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