Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulators

FEATURES

- **Maintains Constant Frequency at Low Output Currents**
- Dual N-Channel MOSFET Synchronous Drive
- **Programmable Fixed Frequency (PLL Lockable)**
- **Wide V_{IN} Range: 3.5V to 36V Operation**
- Ultrahigh Efficiency
- Very Low Dropout Operation: 99% Duty Cycle
- Low Dropout, 0.5A Linear Regulator for VPP Generation or Low Noise Audio Supply
- Built-In Power-On Reset Timer
- Programmable Soft Start
- Low-Battery Detector
- Remote Output Voltage Sense
- Foldback Current Limiting (Optional)
- Pin Selectable Output Voltage
- Logic-Controlled Micropower Shutdown: $I_Q < 30\mu A$
- Output Voltages from 1.19V to 9V
- Available in 28- and 36-Lead SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Portable Instruments
- Battery-Operated Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®1438/LTC1439 are dual, synchronous step-down switching regulator controllers which drive external N-channel power MOSFETs in a phase-lockable fixed frequency architecture. The Adaptive Power™ output stage selectively drives two N-channel MOSFETs at frequencies up to 400kHz while reducing switching losses to maintain high efficiencies at low output currents.

An auxiliary 0.5A linear regulator using an external PNP pass device provides a low noise, low dropout voltage source. A secondary winding feedback control pin (SFB1) guarantees regulation regardless of load on the main output by forcing continuous operation.

An additional comparator is available for use as a low battery detector. A power-on reset timer (POR) is included which generates a signal delayed by $65536/f_{CLK}$ (typ 300ms) after the output is within 5% of the regulated output voltage. Internal resistive dividers provide pin selectable output voltages with remote sense capability on one of the two outputs.

The operating current levels are user-programmable via external current sense resistors. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

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TYPICAL APPLICATION

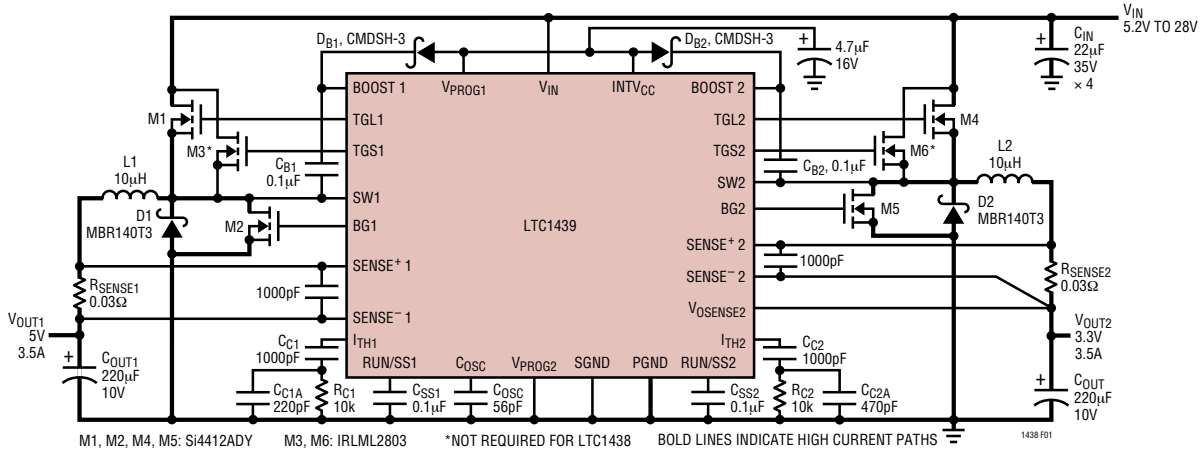
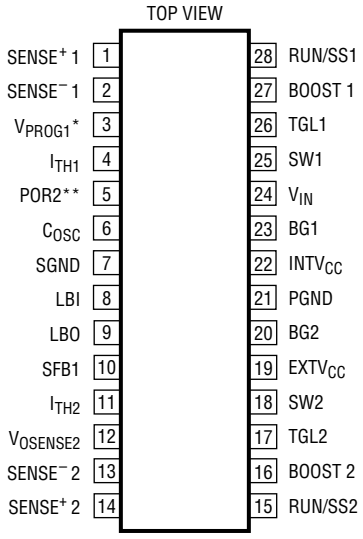


Figure 1. High Efficiency Dual 5V/3V Step-Down Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Voltage (BOOST 1, 2) ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... V_{IN} + 5V to –5V
$EXTV_{CC}$ Voltage ..... 10V to –0.3V
POR2, LBO Voltages ..... 12V to –0.3V
AUXFB Voltage ..... 20V to –0.3V
AUXDR Voltage ..... 28V to –0.3V
$SENSE^+$ 1, $SENSE^+$ 2, $SENSE^-$ 1, $SENSE^-$ 2,
$V_{OSENSE2}$ Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
V_{PROG1}, V_{PROG2} Voltages ..... $INTV_{CC}$ to –0.3V
PLL LPF, I_{TH1}, I_{TH2} Voltages ..... 2.7V to –0.3V
AUXON, PLLIN, SFB1,
RUN/SS1, RUN/SS2, LBI Voltages ..... 10V to –0.3V
Peak Output Current < 10μs (TGL1, 2, BG1, 2) 2A
Peak Output Current < 10μs (TGS1, 2) 250mA
$INTV_{CC}$ Output Current 50mA
Operating Ambient Temperature Range
Commercial ..... 0°C to 70°C
Extended (Note 7) ..... –40°C to 85°C
Industrial ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



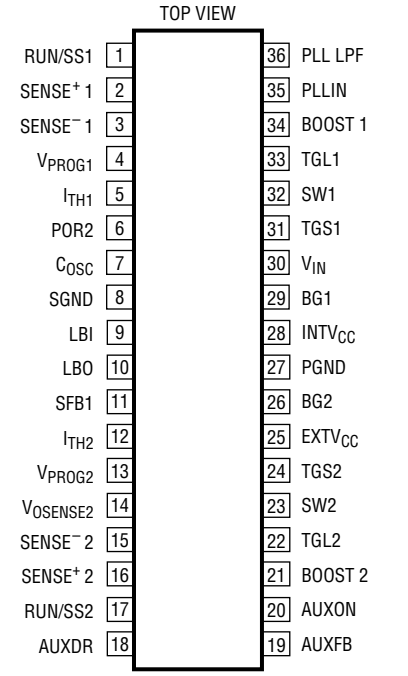
G PACKAGE
28-LEAD PLASTIC SSOP

*$V_{OSENSE1}$ ON LTC1438-ADJ
**NC ON THE LTC1438XCG

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1438CG
LTC1438CG-ADJ
LTC1438IG
LTC1438IG-ADJ
LTC1438XCG



G PACKAGE
36-LEAD PLASTIC SSOP

GW PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (GW)

ORDER PART NUMBER

LTC1439CG
LTC1439EG
LTC1439IG
LTC1439CGW
LTC1439IGW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
I_{IN} $V_{OSENSE1,2}$	Feedback Current	V_{PROG1}, V_{PROG2} Pins Open (Note 3)			10	50	nA
$V_{OUT1,2}$	Regulated Output Voltage	(Note 3)					
	1.19V (Adjustable) Selected	V_{PROG1}, V_{PROG2} Pins Open	●	1.178	1.19	1.202	V
	3.3V Selected	V_{PROG1}, V_{PROG2} = 0V	●	3.220	3.30	3.380	V
	5V Selected	V_{PROG1}, V_{PROG2} = INT V_{CC}	●	4.900	5.00	5.100	V
$V_{LINEREG1,2}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 20V (Note 3), $V_{PROG1,2}$ Pins Open			0.002	0.01	%/V
$V_{LOADREG1,2}$	Output Voltage Load Regulation	$I_{TH1,2}$ Sinking 5μA (Note 3)	●		0.5	0.8	%
		$I_{TH1,2}$ Sourcing 5μA	●		–0.5	–0.8	%
V_{SFB1}	Secondary Feedback Threshold	V_{SFB1} Ramping Negative	●	1.16	1.19	1.22	V
I_{SFB1}	Secondary Feedback Current	V_{SFB1} = 1.5V			–1	–2	μA
V_{OVL}	Output Overvoltage Lockout	$V_{PROG1,2}$, SENSE⁻ 1 and $V_{OSENSE1,2}$ Pins Open		1.24	1.28	1.32	V
$I_{PROG1,2}$	$V_{PROG1,2}$ Input Current	0.5V > $V_{PROG1,2}$			–3	–6	μA
		INTV_{CC} – 0.5V < $V_{PROG1,2}$ < INTV_{CC}			3	6	μA
I_Q	Input DC Supply Current	EXTV_{CC} = 5V (Note 4)					
	Normal Mode	3.6V < V_{IN} < 30V, V_{AUXON} = 0V			320		μA
	Shutdown	$V_{RUN/SS1,2}$ = 0V, 3.6V < V_{IN} < 15V			16	30	μA
$V_{RUN/SS1,2}$	Run Pin Threshold		●	0.8	1.3	2	V
$I_{RUN/SS1,2}$	Soft Start Current Source	$V_{RUN/SS1,2}$ = 0V		1.5	3	4.5	μA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{OSENSE1,2}$ = 0V, 5V $V_{PROG1,2}$ = Pins Open		130	150	180	mV
TGL1, 2 t_r, t_f	TGL1, TGL2 Transition Time						
	Rise Time	C_{LOAD} = 3000pF			50	150	ns
	Fall Time	C_{LOAD} = 3000pF			50	150	ns
TGS1, 2 t_r, t_f	TGS1, TGS2 Transition Time						
	Rise Time	C_{LOAD} = 500pF			100	200	ns
	Fall Time	C_{LOAD} = 500pF			50	150	ns
BG1, 2 t_r, t_f	BG1, BG2 Transition Time						
	Rise Time	C_{LOAD} = 3000pF			50	150	ns
	Fall Time	C_{LOAD} = 3000pF			50	150	ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.8	5.0	5.2	V
V_{LDO} INT	INTV_{CC} Load Regulation	I_{INTVCC} = 20mA, V_{EXTVCC} = 4V			–0.2	–1	%
V_{LDO} EXT	EXTV_{CC} Voltage Drop	I_{INTVCC} = 20mA, V_{EXTVCC} = 5V			170	300	mV
V_{EXTVCC}	EXTV_{CC} Switchover Voltage	I_{INTVCC} = 20mA, EXTV_{CC} Ramping Positive	●	4.5	4.7		V
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF, LTC1439: PLL LPF = 0V (Note 5)		112	125	138	kHz
	VCO High	LTC1439, V_{PLLLPF} = 2.4V		200	240		kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
I_{PLLLPF}	Phase Detector Output Current	LTC1439					
	Sinking Capability	f_{PLLIN} < f_{OSC}		10	15	20	μA
	Sourcing Capability	f_{PLLIN} > f_{OSC}		10	15	20	μA
Power-On Reset							
$V_{SATPOR2}$	POR2 Saturation Voltage	I_{POR2} = 1.6mA, $V_{OSENSE2}$ = 1V, V_{PROG2} Pin Open			0.6	1	V
I_{LPOR2}	POR2 Leakage	V_{POR2} = 12V, $V_{OSENSE2}$ = 1.2V, V_{PROG2} Pin Open			0.2	1	μA
V_{THPOR2}	POR2 Trip Voltage	V_{PROG2} Pin Open % of V_{REF} $V_{OSENSE2}$ Ramping Negative		–11	–7.5	–4	%
t_{DPOR2}	POR2 Delay	V_{PROG2} Pin Open			65536		Cycles

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Battery Comparator							
V_{SATLBO}	LBO Saturation Voltage	I_{LBO} = 1.6mA, V_{LBI} = 1.1V			0.6	1	V
I_{LLBO}	LBO Leakage	V_{LBO} = 12V, V_{LBI} = 1.4V	●		0.01	1	µA
V_{THLB1}	LBI Trip Voltage	High to Low Transition on LBO	●	1.16	1.19	1.22	V
I_{INLB1}	LBI Input Current	V_{LBI} = 1.19V	●		1	50	nA
V_{HYSLBO}	LBO Hysteresis				20		mV
Auxiliary Regulator/Comparator							
I_{AUXDR}	AUXDR Current	V_{EXTVCC} = 0V					
	Max Current Sinking Capability	V_{AUXDR} = 4V, V_{AUXFB} = 1.0V, V_{AUXON} = 5V		10	15		mA
	Control Current	V_{AUXDR} = 5V, V_{AUXFB} = 1.5V, V_{AUXON} = 5V			1	5	µA
	Leakage when OFF	V_{AUXDR} = 24V, V_{AUXFB} = 1.5V, V_{AUXON} = 0V			0.01	1	µA
$I_{INAUXFB}$	AUXFB Input Current	V_{AUXFB} = 1.19V, V_{AUXON} = 5V			0.01	1	µA
$I_{INAUXON}$	AUXON Input Current	V_{AUXON} = 5V			0.01	1	µA
$V_{THAUXON}$	AUXON Trip Voltage	V_{AUXDR} = 4V, V_{AUXFB} = 1V		1.0	1.19	1.4	V
$V_{SATAUXDR}$	AUXDR Saturation Voltage	I_{AUXDR} = 1.6mA, V_{AUXFB} = 1V, V_{AUXON} = 5V			0.4	0.8	V
V_{AUXFB}	AUXFB Voltage	V_{AUXON} = 5V, 11V < V_{AUXDR} < 24V (Note 6)	●	11.5	12.0	12.5	V
		V_{AUXON} = 5V, 3V < V_{AUXDR} < 7V	●	1.14	1.19	1.24	V
$V_{THAUXDR}$	AUXFB Divider Disconnect Voltage	V_{AUXON} = 5V (Note 6); Ramping Negative		7.5	8.5	9.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1438CG, LTC1439CG: $T_J = T_A + (P_D)(95°C/W)$

LTC1439CGW: $T_J = T_A + (P_D)(85°C/W)$

Note 3: The LTC1438 and LTC1439 are tested in a feedback loop which servos $V_{OSENSE1,2}$ to the balance point for the error amplifier ($V_{ITH1,2}$ = 1.19V).

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: Oscillator frequency is tested by measuring the C_{OSC} charge and discharge current (I_{OSC}) and applying the formula:

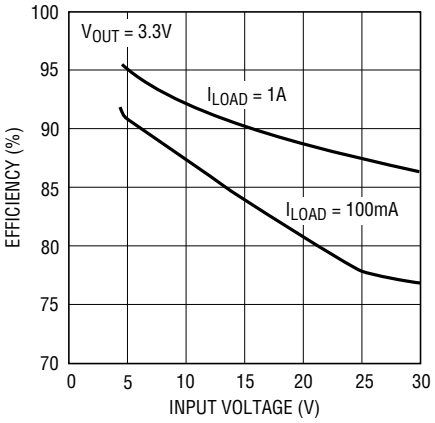
$$f_{OSC}\ (kHz) = 8.4(10^8)[C_{OSC}\ (pF) + 11]^{-1}\ (1/I_{CHG} + 1/I_{DISC})^{-1}$$

Note 6: The auxiliary regulator is tested in a feedback loop which servos V_{AUXFB} to the balance point for the error amplifier. For applications with V_{AUXDR} > 9.5V, V_{AUXFB} uses an internal resistive divider. See Applications Information section.

Note 7: The LTC1439EG is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

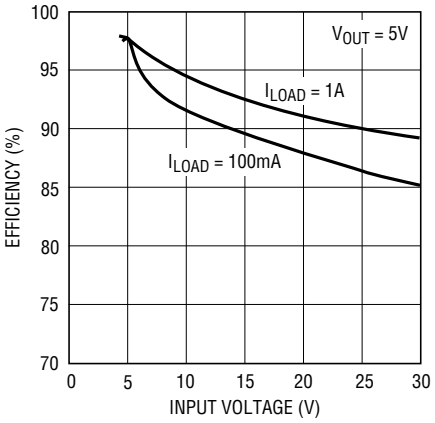
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage V_{OUT} = 3.3V



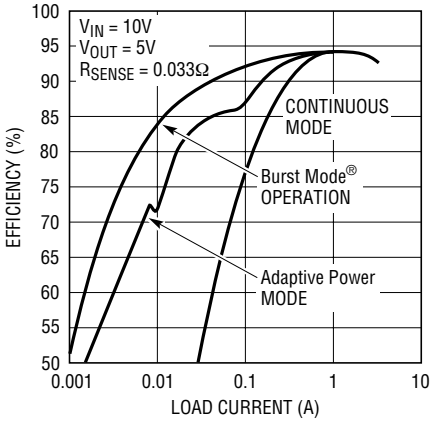
1438 G01

Efficiency vs Input Voltage V_{OUT} = 5V



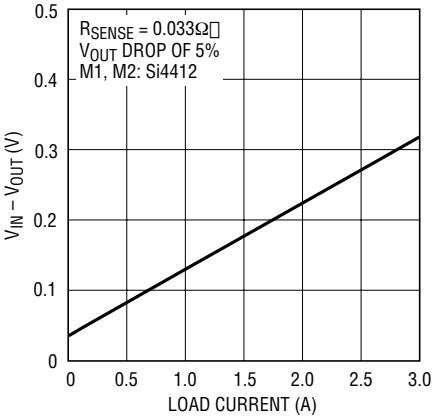
1438 G02

Efficiency vs Load Current



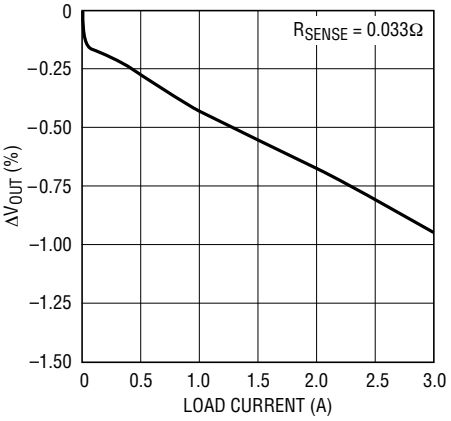
1435 G03

$V_{IN} - V_{OUT}$ Dropout Voltage vs Load Current



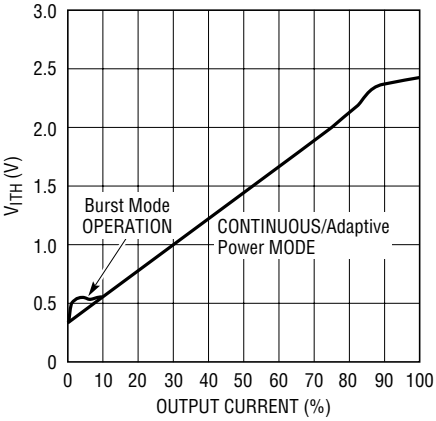
1438 G04

Load Regulation



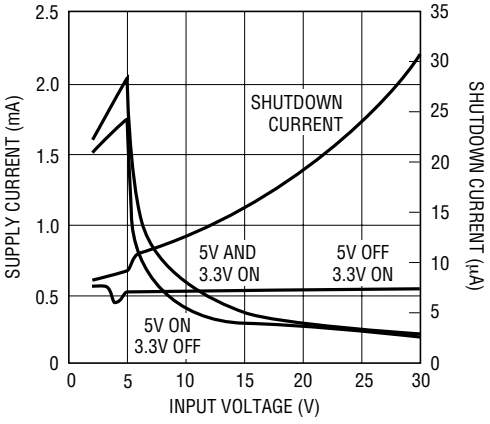
1438 G05

V_{ITH} Pin Voltage vs Output Current



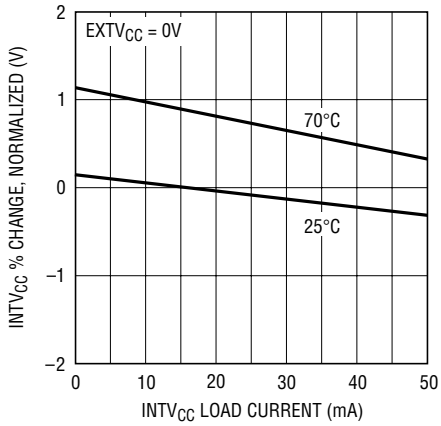
1438 G06

Input Supply Current vs Input Voltage



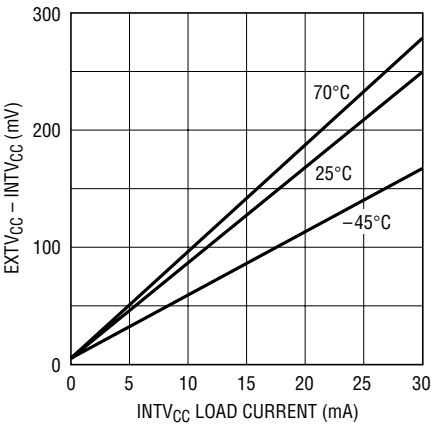
1438 G07

$INTV_{CC}$ Regulation vs $INTV_{CC}$ Load Current



1438 G08

$EXTV_{CC}$ Switch Drop vs $INTV_{CC}$ Load Current

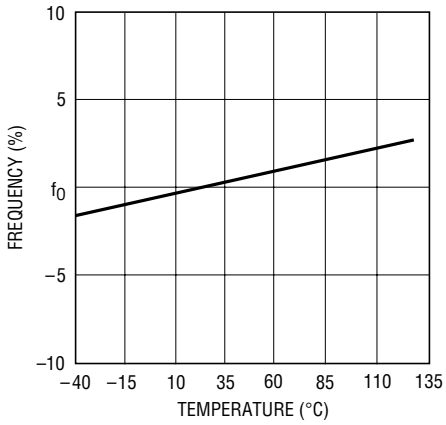


1438 G09

Burst Mode is a registered trademark of Linear Technology Corporation.

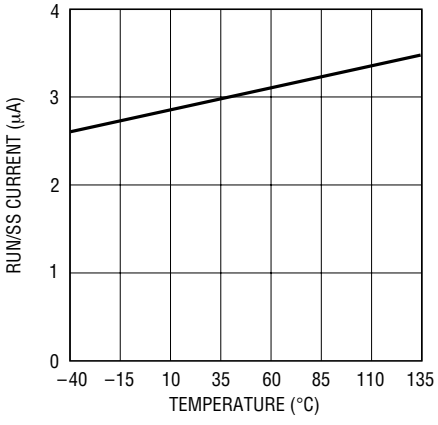
TYPICAL PERFORMANCE CHARACTERISTICS

Normalized Oscillator Frequency vs Temperature



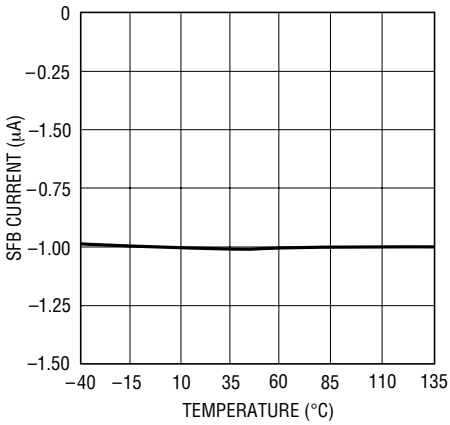
1438 G10

RUN/SS Pin Current vs Temperature



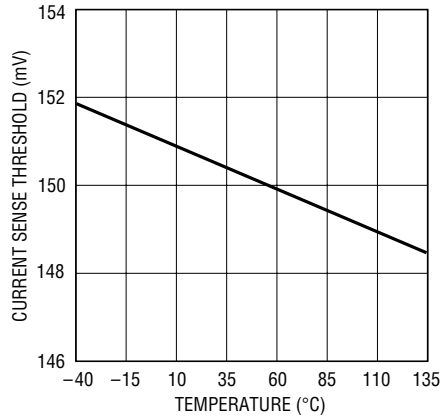
1438 G11

SFB1 Pin Current vs Temperature



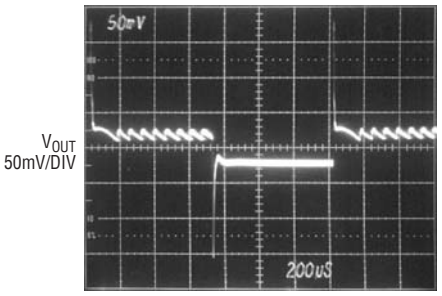
1438 G12

Maximum Current Sense Threshold Voltage vs Temperature



1438 G13

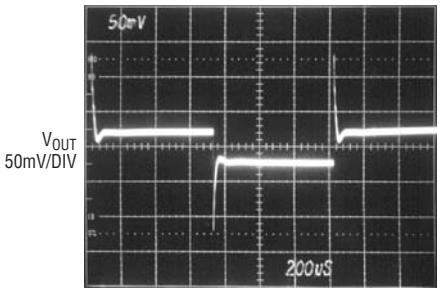
Transient Response



I_{LOAD} = 50mA to 1A

1438 G14

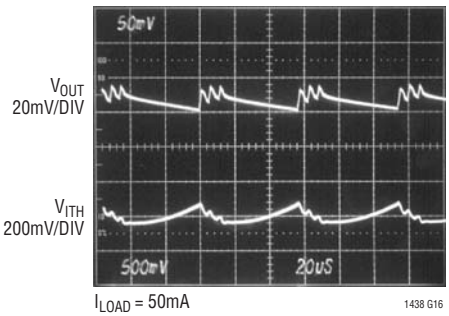
Transient Response



I_{LOAD} = 1A to 3A

1438 G15

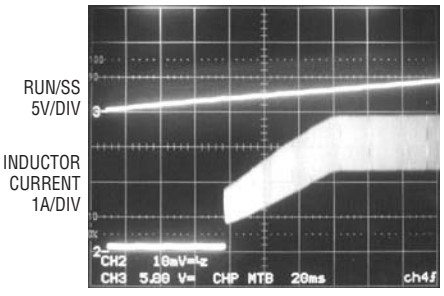
Burst Mode Operation



I_{LOAD} = 50mA

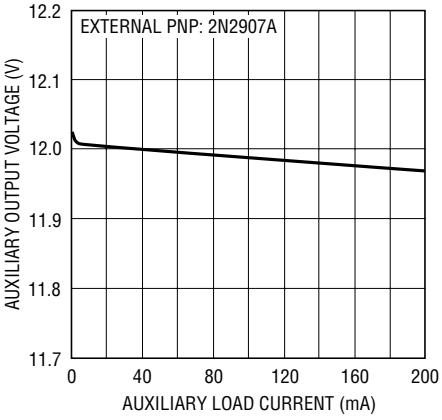
1438 G16

Soft Start: Load Current vs Time



1438 G17

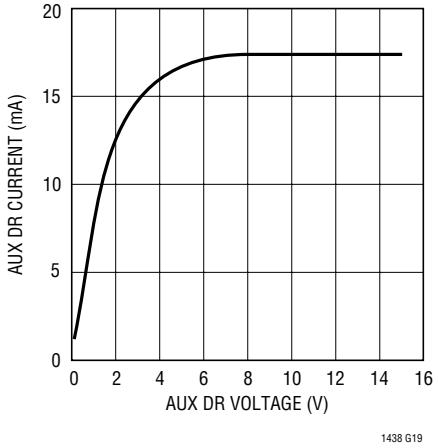
Auxiliary Regulator Load Regulation



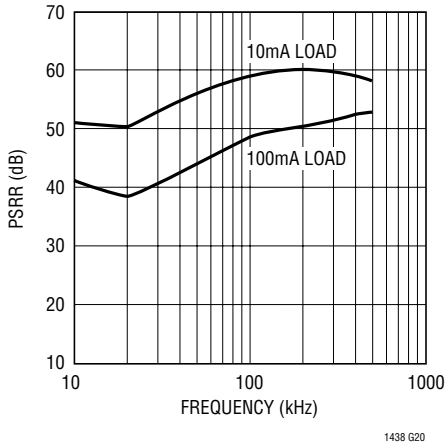
1438 G18

TYPICAL PERFORMANCE CHARACTERISTICS

Auxiliary Regulator Sink Current Available



Auxiliary Regulator PSRR



PIN FUNCTIONS

V_{IN}: Main Supply Pin. Must be closely decoupled to the IC's signal ground pin.

$INTV_{CC}$: Output of the Internal 5V Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage. Must be closely decoupled to power ground with a minimum of 2.2µF tantalum or electrolytic capacitor. The $INTV_{CC}$ regulator turns off when both RUN/SS1 and RUN/SS2 are low. Refer to the LTC1538/LTC1539 for 5V keep-alive applications.

$EXTV_{CC}$: External Power Input to an Internal Switch. This switch closes and supplies $INTV_{CC}$, bypassing the internal low dropout regulator whenever $EXTV_{CC}$ is higher than 4.7V. Connect this pin to V_{OUT} of the controller with the higher output voltage. Do not exceed 10V on this pin. See $EXTV_{CC}$ connection in Applications Information section.

BOOST 1, BOOST 2: Supplies to the Topside Floating Drivers. The bootstrap capacitors are returned to these pins. Voltage swing at these pins is from $INTV_{CC}$ to V_{IN} + $INTV_{CC}$.

SW1, SW2: Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

SGND: Small-Signal Ground. Common to both controllers, must be routed separately from high current grounds to the (–) terminals of the C_{OUT} capacitors.

PGND: Driver Power Ground. Connects to sources of bottom N-channel MOSFETs and the (–) terminals of C_{IN}.

$SENSE^-$ 1, $SENSE^-$ 2: Connects to the (–) input for the current comparators. Except for the LTC1438-ADJ, $SENSE^-$ 1 is internally connected to the first controller's V_{OUT} sensing point. The first controller can only be used as a 3.3V or 5.0V regulator controlled by the V_{PROG1} pin with the LTC1438, LTC1438X and LTC1439. The LTC1438-ADJ Controller 1 implements a remote sensing adjustable regulator. The second controller can be set to a 3.3V, 5.0V or an adjustable regulator controlled by the V_{PROG2} pin (see Table 1).

Table 1. Output Voltage Table

	LTC1438-ADJ	LTC1438/LTC1438X	LTC1439
Controller 1	Adjustable Only	5V or 3.3V Only	
	Secondary Feedback Loop		
Controller 2	Adjustable Only Remote Sensing POR2 Output	Adjustable Only Remote Sensing POR2 Output	5V/3.3V/Adjustable Remote Sensing POR2 Output

PIN FUNCTIONS

SENSE+ 1, **SENSE+ 2:** The (+) Input to Each Current Comparator. Built-in offsets between SENSE– 1 and SENSE+ 1 pins in conjunction with R_{SENSE1} set the current trip threshold (same for second controller).

$V_{OSENSE1,2}$: Receives the remotely sensed feedback voltage either from the output directly or from an external resistive divider across the output. The V_{PROG2} pin determines which point $V_{OSENSE2}$ must connect to. The $V_{OSENSE1}$ pin, only available on the LTC1438-ADJ, requires an external resistive divider to set the output voltage.

V_{PROG1}, **V_{PROG2}:** Programs Internal Voltage Attenuators for Output Voltage Sensing. The voltage sensing for thefirst controller is internally connected to SENSE– 1 while the $V_{OSENSE2}$ pin allows for remote sensing for the second controller. For V_{PROG1}, $V_{PROG2} < V_{INTVCC}/3$, the divider is set for an output voltage of 3.3V. With V_{PROG1}, $V_{PROG2} > V_{INTVCC}/1.5$ the divider is set for an output voltage of 5V. Leaving V_{PROG2} open (DC) allows the output voltage of the second controller to be set by an external resistive divider connected to $V_{OSENSE2}$.

C_{OSC}: External capacitor C_{OSC} from this pin to ground sets the operating frequency.

I_{TH1}, **I_{TH2}:** Error Amplifier Compensation Point. Each associated current comparator threshold increases with this control voltage.

RUN/SS1, **RUN/SS2:** Combination of Soft Start and Run Control Inputs. A capacitor to ground at each of these pins sets the ramp time to full current output. The time is approximately 0.5s/μF. Forcing either of these pins below 1.3V causes the IC to shut down the circuitry required for that particular controller. Forcing both of these pins below 1.3V causes the device to shut down completely. For applications which require 5V keep-alive, refer to the LTC1538-AUX/LTC1539.

TGL1, **TGL2:** High Current Gate Drives for Main Top N-Channel MOSFET. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW1 and SW2.

TGS1, **TGS2:** Gate Drives for Small Top N-Channel MOSFET. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW. Leaving TGS1 or TGS2 open invokes Burst Mode operation for that controller.

BG1, **BG2:** High Current Gate Drive Outputs for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

SFB1: Secondary Winding Feedback Input. This input acts only on the first controller and is normally connected to a feedback resistive divider from the secondary winding. Pulling this pin below 1.19V will force continuous synchronous operation for the first controller. This pin should be tied to: ground to force continuous operation; $INTV_{CC}$ in applications that don't use a secondary winding; and a resistive divider from the output in applications using a secondary winding.

POR2: This output is a drain of an N-channel pull-down. This pin sinks current when the output voltage of the second controller drops 7.5% below its regulated voltage and releases 65536 oscillator cycles after the output voltage of the second controller rises to within –5% value of its regulated value. The POR2 output is asserted when RUN/SS1 and RUN/SS2 are both low, independant of the V_{OUT2}. This pin is not functional on the LTC1438X.

LBO: This output is a drain of an N-channel pull-down. This pin will sink current when the LBI pin goes below 1.19V.

LBI: The (+) input of a comparator which can be used as a low-battery voltage detector. The (–) input is connected to the 1.19V internal reference.

PLLIN: External Synchronizing Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. Tie this pin to SGND in applications which do not use the phase-locked loop.

PLL LPF: Output of Phase Detector and Control Input of Oscillator. Normally a series RC lowpass filter network is connected from this pin to ground. Tie this pin to SGND in applications which do not use the phase-locked loop. Can be driven by a 0V to 2.4V logic signal for a frequency shifting option.

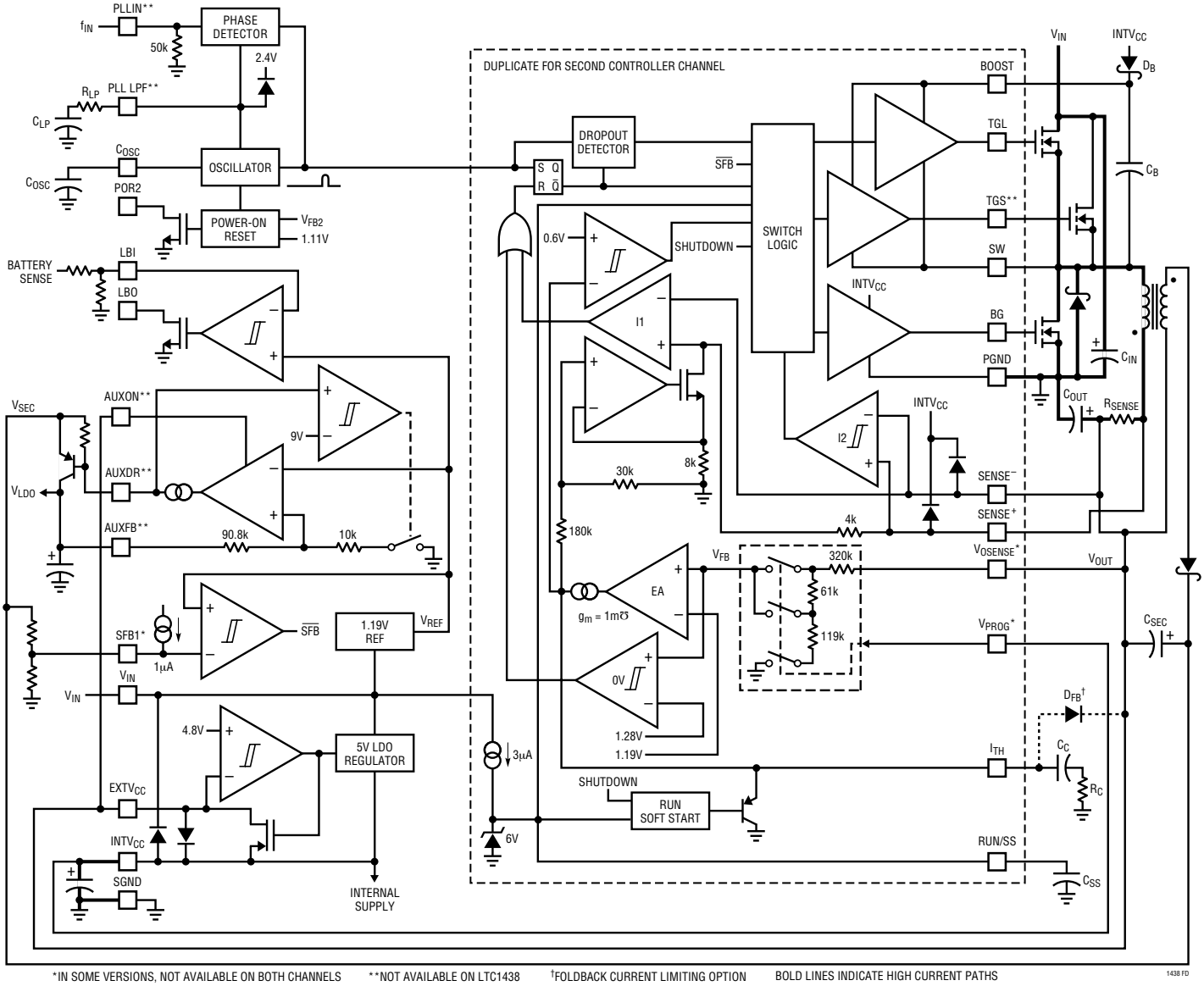
AUXFB: Feedback Input to the Auxiliary Regulator/Comparator. When used as a linear regulator, this input can either be connected to an external resistive divider or

directly to the collector of the external PNP pass device for 12V operation. When used as a comparator, this is the noninverting input of a comparator whose inverting input is tied to the internal 1.19V reference. See Auxiliary Regulator Application section.

AUXON: Pulling this pin high turns on the auxiliary regulator/comparator. The threshold is 1.19V. This is a convenient linear power supply logic-controlled on/off input.

AUXDR: Open Drain Output of the Auxiliary Regulator/Comparator. The base of an external PNP device is connected to this pin when used as a linear regulator. An external pull-up resistor is required for use as a comparator. A voltage >9.5V on AUXDR causes the internal 12V resistive divider to be connected in series with the AUXFB pin.

FUNCTIONAL DIAGRAM



*IN SOME VERSIONS, NOT AVAILABLE ON BOTH CHANNELS **NOT AVAILABLE ON LTC1438 †FOLDBACK CURRENT LIMITING OPTION BOLD LINES INDICATE HIGH CURRENT PATHS

1438 FD

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1438/LTC1439 use a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch and turned off when the main current comparator I1 resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on the I_{TH1} (I_{TH2}) pin, which is the output of each error amplifier (EA). The V_{PROG1} pin, described in the Pin Functions, allows the EA to receive a selectively attenuated output feedback voltage V_{FB1} from the SENSE$^-$1 pin while V_{PROG2} and $V_{OSENSE2}$ allow EA to receive an output feedback voltage V_{FB2} from either internal or external resistive dividers on the second controller. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH1} (I_{TH2}) voltage to increase until the average inductor current matches the new load current. After the large top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating boot strap capacitor C_B, which normally is recharged during each Off cycle. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains on and periodically forces a brief off period to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS1 (RUN/SS2) pin low. Releasing RUN/SS1 (RUN/SS2) allows an internal 3μA current source to charge soft start capacitor C_{SS}. When C_{SS} reaches 1.3V, the main control loop is enabled with the I_{TH1} (I_{TH2}) voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH1} (I_{TH2}) is gradually released allowing normal operation to resume. When both RUN/SS1 and RUN/SS2 are low, all LTC1438/LTC1439 functions are shut down. Refer to the LTC1538-AUX/LTC1539 data sheet for 5V keep-alive applications.

Comparator OV guards against transient overshoots > 7.5% by turning off the top MOSFET and keeping it off until the fault is removed.

Low Current Operation

Adaptive Power mode allows the LTC1439 to automatically change between two output stages sized for different load currents. The TGL1 (TGL2) and BG1 (BG2) pins drive large synchronous N-channel MOSFETs for operation at high currents, while the TGS1 (TGS2) pin drives a much smaller N-channel MOSFET used in conjunction with a Schottky diode for operation at low currents. This allows the loop to continue to operate at normal operating frequency as the load current decreases without incurring the large MOSFET gate charge losses. If the TGS1 (TGS2) pin is left open, the loop defaults to Burst Mode operation in which the large MOSFETs operate intermittently based on load demand.

Adaptive Power mode provides constant frequency operation down to approximately 1% of rated load current. This results in an order of magnitude reduction of load current before Burst Mode operation commences. Without the small MOSFET (i.e., no Adaptive Power mode) the transition to Burst Mode operation is approximately 10% of rated load current.

The transition to low current operation begins when comparator I2 detects current reversal and turns off the bottom MOSFET. If the voltage across R_{SENSE} does not exceed the hysteresis of I2 (approximately 20mV) for one full cycle, then on following cycles the top drive is routed to the small MOSFET at the TGS1 (TGS2) pin and the BG1 (BG2) pin is disabled. This continues until an inductor current peak exceeds 20mV/R_{SENSE} or the I_{TH1} (I_{TH2}) voltage exceeds 0.6V, either of which causes drive to be returned to the TGL1 (TGL2) pin on the next cycle.

Two conditions can force continuous synchronous operation, even when the load current would otherwise dictate low current operation. One is when the common mode voltage of the SENSE$^+$ 1 (SENSE$^+$ 2) and SENSE$^-$ 1 (SENSE$^-$2) pins are below 1.4V, and the other is when the SFB1 pin is below 1.19V. The latter condition is used to assist in secondary winding regulation, as described in the Applications Information section.

OPERATION (Refer to Functional Diagram)

Frequency Synchronization

A Phase-Locked Loop (PLL) is available on the LTC1439 to allow the oscillator to be synchronized to an external source connected to the PLLIN pin. The output of the phase detector at the PLL LPF pin is also the control input of the oscillator, which operates over a 0V to 2.4V range corresponding to –30% to 30% in frequency. When locked, the PLL aligns the turn-on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, PLL LPF goes low, forcing the oscillator to minimum frequency.

Power-On Reset

The POR2 pin is an open drain output which pulls low when the main regulator output voltage of the second controller is out of regulation. When the output voltage rises to within 7.5% of regulation, a timer is started which releases POR2 after 2^{16} (65536) oscillator cycles. This function is not available on the LTC1438X.

Auxiliary Linear Regulator

The auxiliary linear regulator in the LTC1439 controls an external PNP transistor for operation up to 500mA. A precise internal AUXFB resistive divider is invoked when the AUXDR pin is above 9.5V to allow regulated 12V VPP supplies to be easily implemented. When AUXDR is below 8.5V an external feedback divider may be used to set other output voltages. Taking the AUXON pin low shuts down the auxiliary regulator providing a convenient logic-controlled power supply.

The AUX block can be used as a comparator having its inverting input tied to the internal 1.19V reference. The AUXDR pin is used as the output and requires an external pull-up to a supply of less than 8.5V in order to inhibit the invoking of the internal resistive divider.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the other LTC1438/LTC1439 circuitry is derived from the $INTV_{CC}$ pin. The bottom MOSFET driver supply is also connected to $INTV_{CC}$. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on to connect $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.

APPLICATIONS INFORMATION

The basic LTC1439 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1438/LTC1439 current comparator has a maximum threshold of 150mV/R_{SENSE} and an input common mode range of SGND to $INTV_{CC}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing some margin for variations in the LTC1438/LTC1439 and external component values yield:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1438/LTC1439 work well with values of R_{SENSE} from 0.005Ω to 0.2Ω.

C_{OSC} Selection for Operating Frequency

The LTC1438/LTC1439 use a constant frequency architecture with the frequency determined by an external oscillator capacitor on C_{OSC}. Each time the topside MOSFET turns on, the voltage on C_{OSC} is reset to ground. During the on-time, C_{OSC} is charged by a fixed current plus an additional current which is proportional to the output voltage of the phase detector (V_{PLLLPF})(LTC1439 only). When the voltage on the capacitor reaches 1.19V, C_{OSC} is reset to ground. The process then repeats.

The value of C_{OSC} is calculated from the desired operating frequency. Assuming the phase-locked loop has no external oscillator input (V_{PLLLPF} = 0V):

$$C_{OSC}(pF) = \left[\frac{1.37(10^4)}{Frequency\ (kHz)}\right] - 11$$

A graph for selecting C_{OSC} vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum recommended switching frequency is 400kHz. When using Figure 2 for synchronizable applications, choose C_{OSC} corresponding to a frequency approximately 30% below your center frequency. (See Phase-Locked Loop and Frequency Sychronization).

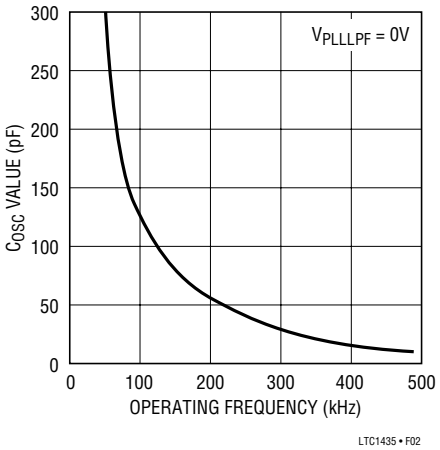


Figure 2. Timing Capacitor Value

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation (TGS1, 2 pins open), lower inductance values will cause the burst frequency to decrease.

The Figure 3 graph gives a range of recommended inductor values vs operating frequency and V_{OUT}.

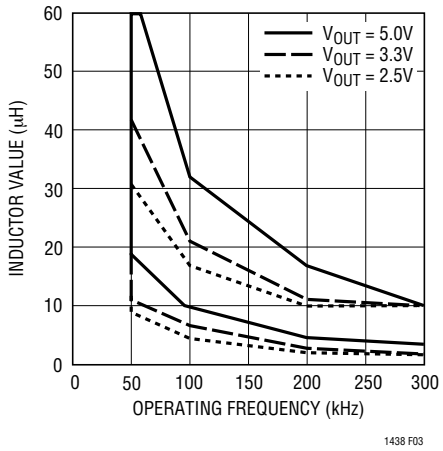


Figure 3. Recommended Inductor Values

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET and D1 Selection

Three external power MOSFETs must be selected for each controller with the LTC1439: a pair of N-channel MOSFETs for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch. Only one top MOSFET is required for each LTC1438 controller.

To take advantage of the Adaptive Power output stage, two topside MOSFETs must be selected. A large [low $R_{SD(ON)}$] MOSFET and a small [higher $R_{DS(ON)}$] MOSFET are required. The large MOSFET is used as the main switch and works in conjunction with the synchronous switch. The smaller MOSFET is only enabled under low load current conditions. The benefit of this is to boost low to midcurrent efficiencies while continuing to operate at constant frequency. Also, by using the small MOSFET the circuit will keep switching at a constant frequency down to lower currents and delay skipping cycles.

The $R_{DS(ON)}$ recommended for the small MOSFET is around 0.5Ω. Be careful not to use a MOSFET with an $R_{DS(ON)}$ that is too low; remember, we want to conserve gate charge. (A higher $R_{DS(ON)}$ MOSFET has a smaller gate capacitance and thus requires less current to charge its gate). For all LTC1438 and cost sensitive LTC1439 applications, the small MOSFET is not required. The circuit then begins Burst Mode operation as the load current drops.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic level threshold MOSFETs must be used in most LTC1438/LTC1439 applications. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V (must be less than 10V), in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{SD(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1438/LTC1439 are operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + k(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. Refer to the Foldback Current Limiting section for further applications information.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 2.5 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 serves two purposes. During continuous synchronous operation, D1 conducts during the dead-time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. During low current operation, D1 operates in conjunction with the small top MOSFET to provide an efficient low current output stage. A 1A Schottky is generally a good compromise for both regions of operation due to the relatively small average current.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX}\frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

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The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisified the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{4fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4 I_{OUT(MAX)}$ the output ripple will be less than 100mV at max V_{IN} assuming:

C_{OUT} Required ESR < $2R_{SENSE}$

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the drivers and internal circuitry within the LTC1438/LTC1439. The $INTV_{CC}$ pin regulator can supply 40mA and must be bypassed to ground with a minimum of 2.2µF tantalum or low ESR electrolytic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1438/LTC1439 to be exceeded. The IC supply current is dominated by the gate charge supply current when not using an output derived $EXTV_{CC}$ source. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC1439 is limited to less than 21mA from a 30V supply:

$T_J = 70°C + (21mA)(30V)(85°C/W) = 124°C$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The LTC1438/LTC1439 contain an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the internal regulator is turned off and an internal switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal power to the IC. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation (4.8V < V_{OUT} < 9V) and from the internal regulator when the output is out of regulation (start-up, short circuit). Do not apply greater than 10V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this supply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting

APPLICATIONS INFORMATION

in an efficiency penalty of up to 10% at high input voltages.

2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.8V. This can be done with either the inductive boost winding as shown in Figure 4a or the capacitive charge pump shown in Figure 4b. The charge pump has the advantage of simple magnetics.

4. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 10V range ($EXTV_{CC} \leq V_{IN}$) it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must be always present during operation to prevent MOSFET failure due to insufficient gate drive.

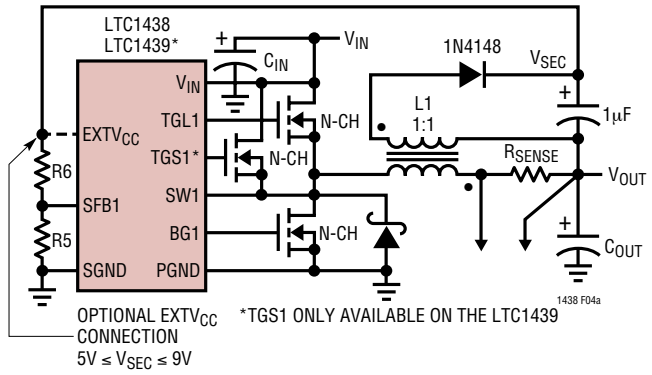

Figure 4a. Secondary Output Loop and $EXTV_{CC}$ Connection

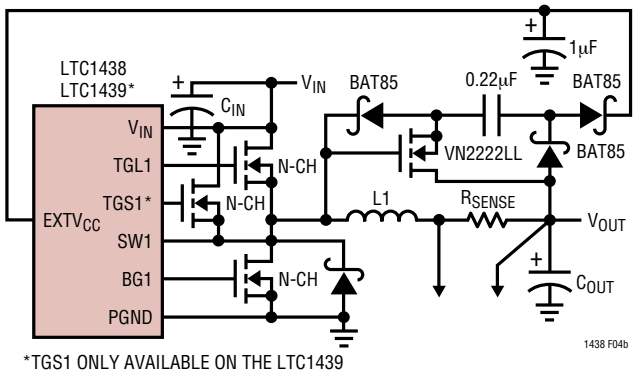

Figure 4b. Capacitive Charge Pump for $EXTV_{CC}$

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST 1 and BOOST 2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged through diode D_B from $INTV_{CC}$ when the SW1(SW2) pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW1(SW2) rises to V_{IN} and the BOOST 1(BOOST 2) pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown on D_B must be greater than $V_{IN(MAX)}$.

Output Voltage Programming

The LTC1438/LTC1439 have pin selectable output voltage programming. Controller 1 on the LTC1438-ADJ is a dedicated adjustable controller. The output voltage is selected by the V_{PROG1} (V_{PROG2}) pin as follows on all of the other parts:

$V_{PROG1,2}$ = 0V	$V_{OUT1,2}$ = 3.3V
$V_{PROG1,2}$ = $INTV_{CC}$	$V_{OUT1,2}$ = 5V
V_{PROG2} = Open (DC)	V_{OUT2} = Adjustable

Except for the LTC1438-ADJ, the top of an internal resistive divider is connected to $SENSE^-1$ pin in Controller 1. For fixed output voltage applications the $SENSE^-1$ pin is connected to the output voltage as shown in Figure 5a. When using an external resistive divider for an adjustable regulator, the V_{PROG2} pin is left open (V_{PROG1} is internally left open on the LTC1438-ADJ) and the $V_{OSENSE2}$ pin is connected to the feedback resistors as shown in Figure 5b. The adjustable controller will force the externally attenuated output voltage to 1.19V.

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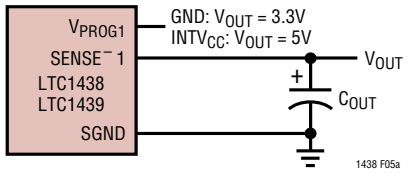

Figure 5a. LTC1438/LTC1439 Fixed Output Applications

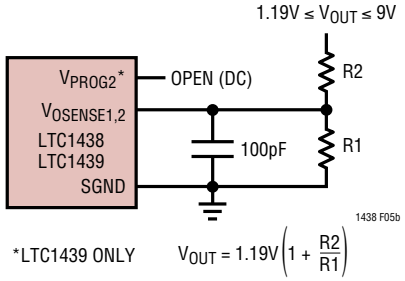

Figure 5b. LTC1438/LTC1439 Adjustable Applications

Power-On Reset Function (POR)

The power-on reset function (not available on the LTC1438X) monitors the output voltage of the second controller and turns on an open drain device when it is below its properly regulated voltage. An external pull-up resistor is required on the POR2 pin.

When power is first applied or when coming out of shutdown, the POR2 output is held at ground. When the output voltage rises above a level which is 5% below the final regulated output value, an internal counter starts. After this counter counts 2^{16} (65536) clock cycles, the POR2 pull-down device turns off.

The POR2 output will go low whenever the output voltage of the second controller drops below 7.5% of its regulated value for longer than approximately 30μs, signaling an out-of-regulation condition. In shutdown, when RUN/SS1 and RUN/SS2 are both below 1.3V, the POR2 output is pulled low even if the regulator's output is held up by an external source. The POR2 output is active during shutdown if V_{IN} is powered.

Run/Soft Start Function

The RUN/SS1 and RUN/SS2 pins each serve two functions. Each pin provides the soft start function and a means to shut down each controller. Soft start reduces surge currents from V_{IN} by providing a gradual ramp-up of the internal current limit. *Power supply sequencing* can also be accomplished using this pin.

An internal 3μA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS1 (RUN/SS2) reaches 1.3V the particular controller is permitted to start operating. As the voltage on the pin continues to ramp from 1.3V to 2.4V, the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately $50mV/R_{SENSE}$ (at $V_{RUN/SS} = 1.3V$) and ends at $150mV/R_{SENSE}$ ($V_{RUN/SS} \geq 2.7V$). The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately 500ms/μF, followed by a similar time to reach full current on that controller.

By pulling both RUN/SS controller pins below 1.3V, the LTC1438/LTC1439 are put into low current shutdown ($I_Q < 25\mu A$). These pins can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft start function; this diode and C_{SS} can be deleted if soft start is not needed. Each RUN/SS pin has an internal 6V Zener clamp (See Functional Diagram).

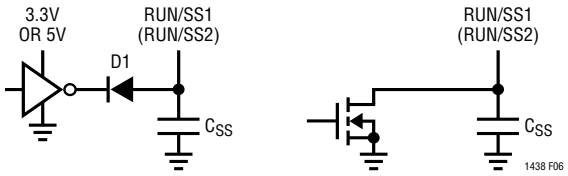

Figure 6. RUN/SS Pin Interfacing

Foldback Current Limiting

As described in Power MOSFET and D1 Selection, the worst-case dissipation for either MOSFET occurs with a short-circuited output, when the synchronous MOSFET conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher $R_{DS(ON)}$ MOSFETs are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diode D_{FB} between the output and the I_{TH} pin as shown in the

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Functional Diagram. In a hard short (V_{OUT} = 0V) the current will be reduced to approximately 25% of the maximum output current. This technique may be used for all applications with regulated output voltages of 1.8V or greater.

Phase-Locked Loop and Frequency Synchronization

The LTC1439 has an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage-controlled oscillator is ±30% around the center frequency f_O.

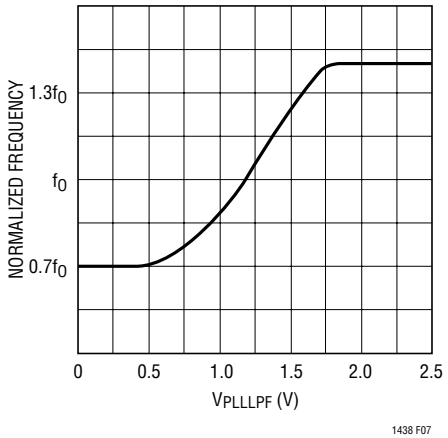

Figure 7. Operating Frequency vs V_{PLLLPF}

The value of C_{OSC} is calculated from the desired operating frequency (f_O). Assuming the phase-locked loop is *locked* (V_{PLLLPF} = 1.19V):

$$C_{OSC}\,(pF) = \left[\frac{2.1(10^4)}{\text{Frequency}\ (kHz)}\right] - 11$$

Stating the frequency as a function of V_{PLLLPF} and C_{OSC}:

$$\text{Frequency}\left(kHz\right) = \frac{8.4(10^8)}{\left[C_{OSC}\left(pF\right) + 11\right]\left[\frac{1}{17\mu A + 18\mu A\left(\frac{V_{PLLLPF}}{2.4V}\right)} + 2000\right]}$$

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.3\ f_O.$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLL LPF pin. A simplified block diagram is shown in Figure 8.

If the external frequency f_{PLLIN} is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLL LPF pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLL LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor

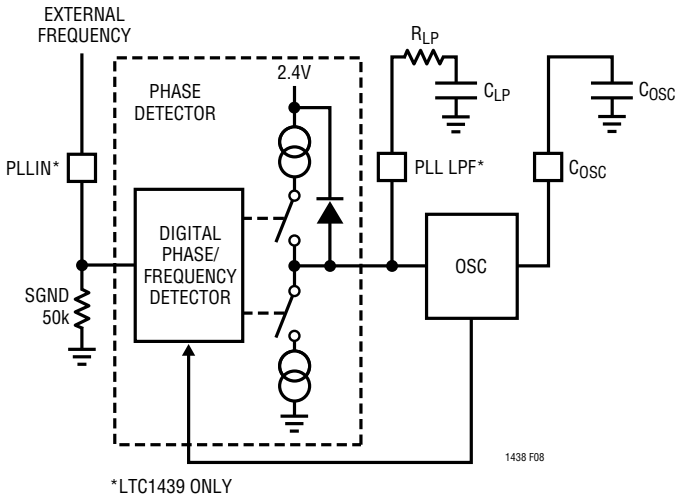

Figure 8. Phase-Locked Loop Block Diagram

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C_{LP} holds the voltage. The LTC1439 PLLIN pin must be driven from a low impedance such as a logic gate located close to the pin. Any external attenuator used needs to be referenced to SGND.

The loop filter components C_{LP}, R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically, R_{LP}=10k and C_{LP} is 0.01μF to 0.1μF. The low side of the filter needs to be connected to SGND.

The PLL LPF pin can be driven with external logic to obtain a 1:1.9 frequency shift. The circuit shown in Figure 9 will provide a frequency shift from f_0 to $1.9f_0$ as the voltage on V_{PLLLPF} increases from 0V to 2.4V. Do not exceed 2.4V on V_{PLLLPF}.

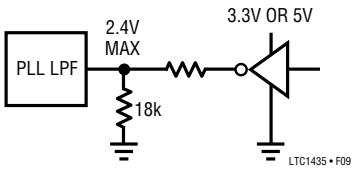

Figure 9. Directly Driving PLL LPF Pin

Low-Battery Comparator

The LTC1438/LTC1439 have an on-chip low-battery comparator which can be used to sense a low-battery condition when implemented as shown in Figure 10. The resistor divider R3/R4 sets the comparator trip point as follows:

$$V_{LBITRIP} = 1.19V\left(1+\frac{R4}{R3}\right)$$

The divided down voltage at the negative (–) input to the comparator is compared to an internal 1.19V reference. A 20mV hysteresis is built in to assure rapid switching. The output is an open drain MOSFET and requires a pull-up resistor. This comparator is *not* active when both the RUN/SS1 and RUN/SS2 pins are low. Refer to the LTC1538/LTC1539 for a comparator which is active during shutdown. The low side of the resistive divider needs to be connected to SGND.

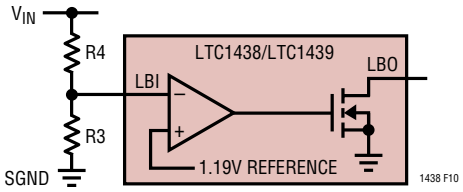

Figure 10. Low-Battery Comparator

SFB1 Pin Operation

When the SFB1 pin drops below its ground referenced 1.19V threshold, continuous mode operation is forced. In continuous mode, the large N-channel main and synchronous switches are used regardless of the load on the main output.

In addition to providing a logic input to force continuous synchronous operation, the SFB1 pin provides a means to regulate a flyback winding output. The use of a synchronous switch removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary winding. With the loop in continuous mode, the auxiliary output may be loaded without regard to the primary output load. The SFB1 pin provides a way to force continuous synchronous operation as needed by the flyback winding.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SFB1 pin as shown in Figure 4a. The secondary regulated voltage V_{SEC} in Figure 4a is given by:

$$V_{SEC} \approx (N+1)V_{OUT} > 1.19V\left(1+\frac{R6}{R5}\right)$$

where N is the turns ratio of the transformer, and V_{OUT} is the main output voltage sensed by Sense$^-$ 1.

Auxiliary Regulator/Comparator

The auxiliary regulator/comparator can be used as a comparator or low dropout regulator (by adding an external PNP pass device).

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When the voltage present at the AUXON pin is greater than 1.19V the regulator/comparator is on. The amplifier is stable when operating as a low dropout regulator. This same amplifier can be used as a comparator whose inverting input is tied to the 1.19V reference.

The AUXDR pin is internally connected to an open drain MOSFET which can sink up to 10mA. The voltage on AUXDR determines whether or not an internal 12V resistive divider is connected to AUXFB as described below. A pull-up resistor is required on AUXDR and the voltage must not exceed 28V.

With the addition of an external PNP pass device, a linear regulator capable of supplying up to 0.5A is created. As shown in Figure 11a, the base of the external PNP connects to the AUXDR pin together with a pull-up resistor. The output voltage V_{OAUX} at the collector of the external PNP is sensed by the AUXFB pin.

The input voltage to the auxiliary regulator can be taken from a secondary winding on the primary inductor as shown in Figure 11a. In this application, the SFB1 pin regulates the input voltage to the PNP regulator (see SFB1 Pin Operation) and should be set to approximately 1V to 2V above the required output voltage of the auxiliary regulator. A Zener clamp diode may be required to keep the secondary winding resultant output voltage under the 28V AUXDR pin specification when the primary is heavily loaded and the secondary is not.

The AUXFB pin is the feedback point of the regulator. An internal resistor divider is available to provide a 12V output by simply connecting AUXFB directly to the collector of the external PNP. The internal resistive divider is switched in when the voltage at AUXFB goes above 9.5V with 1V built-in hysteresis. For other output voltages, an external resistive divider is fed back to AUXFB as shown in Figure 11b. The output voltage V_{OAUX} is set as follows:

$$V_{OAUX} = 1.19V\left(1+\frac{R8}{R7}\right) < 8V \quad AUXDR < 8.5V$$

$$V_{OAUX} = 12V \quad AUXDR \geq 12V$$

When used as a voltage comparator as shown in Figure 11c, the auxiliary block has a noninverting characteristic. When AUXFB drops below 1.19V, the AUXDR pin will be pulled low. A minimum current of 5μA is required to pull up the AUXDR pin to 5V when used as a comparator output in order to counteract a 1.5μA internal pull-down current source.

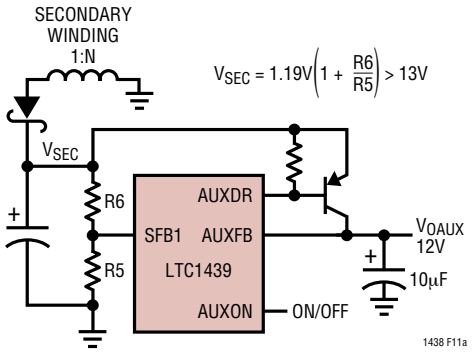

Figure 11a. 12V Output Auxiliary Regulator Using Internal Feedback Resistors

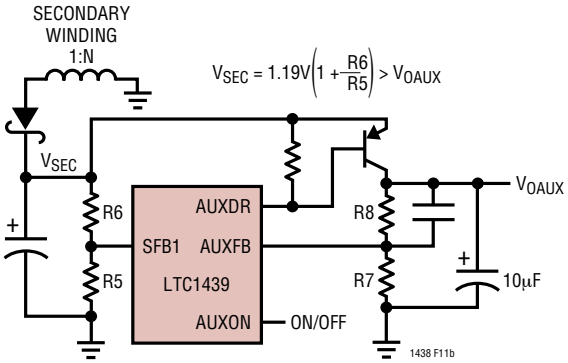

Figure 11b. 5V Output Auxiliary Regulator Using External Feedback Resistors

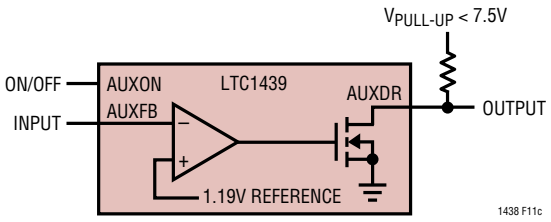

Figure 11c. Auxiliary Comparator Configuration

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Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1438/LTC1439 circuits. LTC1438/LTC1439 V_{IN} current, $INTV_{CC}$ current, I^2R losses and topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current typically results in a small ($\ll$ 1%) loss which increases with V_{IN}.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs. It is for this reason that the large topside and synchronous MOSFETs are turned off during low current operation in favor of the small topside MOSFET and external Schottky diode, allowing efficient, constant-frequency operation at low output currents.

   By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current sense R. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.05Ω, R_L = 0.15Ω and R_{SENSE} = 0.05Ω, then the total resistance is 0.25Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4. Transition losses apply only to the topside MOSFET(s) and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 2.5(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$ where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal which forces the regulator loop to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} external components shown in Figure 1 will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1μF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load

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switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25)(C_{LOAD}). Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 12 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT1438/LT1439 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

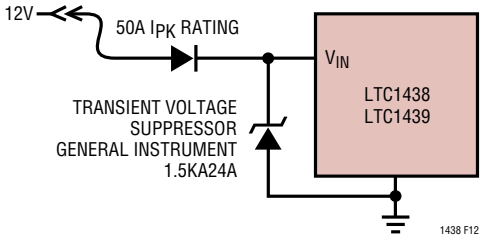

Figure 12. Automotive Application Protection

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 3.3V, I_{MAX} = 3A and f = 250kHz, R_{SENSE} and C_{OSC} can immediately be calculated:

R_{SENSE} = 100mV/3A = 0.033Ω

$C_{OSC} = [1.37(10^4)/250] - 11 \approx 43pF$

Refering to Figure 3, a 10µH inductor falls within the recommended range. To check the actual value of the ripple current the following equation is used :

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I_L = \frac{3.3V}{250kHz(10\mu H)}\left(1-\frac{3.3V}{22V}\right) = 1.12A$$

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4412DY for example; $R_{DS(ON)}$ = 0.042Ω, C_{RSS} = 100pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(3)^2\left[1+(0.005)(50°C-25°C)\right](0.042\Omega)$$
$$+ 2.5(22V)^{1.85}(3A)(100pF)(250kHz) = 122mW$$

The most stringent requirement for the synchronous N-channel MOSFET is with V_{OUT} = 0V (i.e. short circuit). During a continuous short circuit, the worst-case dissipation rises to:

$P_{SYNC} = [I_{SC(AVG)}]^2(1 + \delta)R_{DS(ON)}$

With the 0.033Ω sense resistor $I_{SC(AVG)}$ = 4A will result, increasing the Si4412DY dissipation to 950mW at a die temperature of 105°C.

C_{IN} will require an RMS current rating of at least 1.5A at temperature and C_{OUT} will require an ESR of 0.03Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.03\Omega(1.12A) = 34mV_{P-P}$

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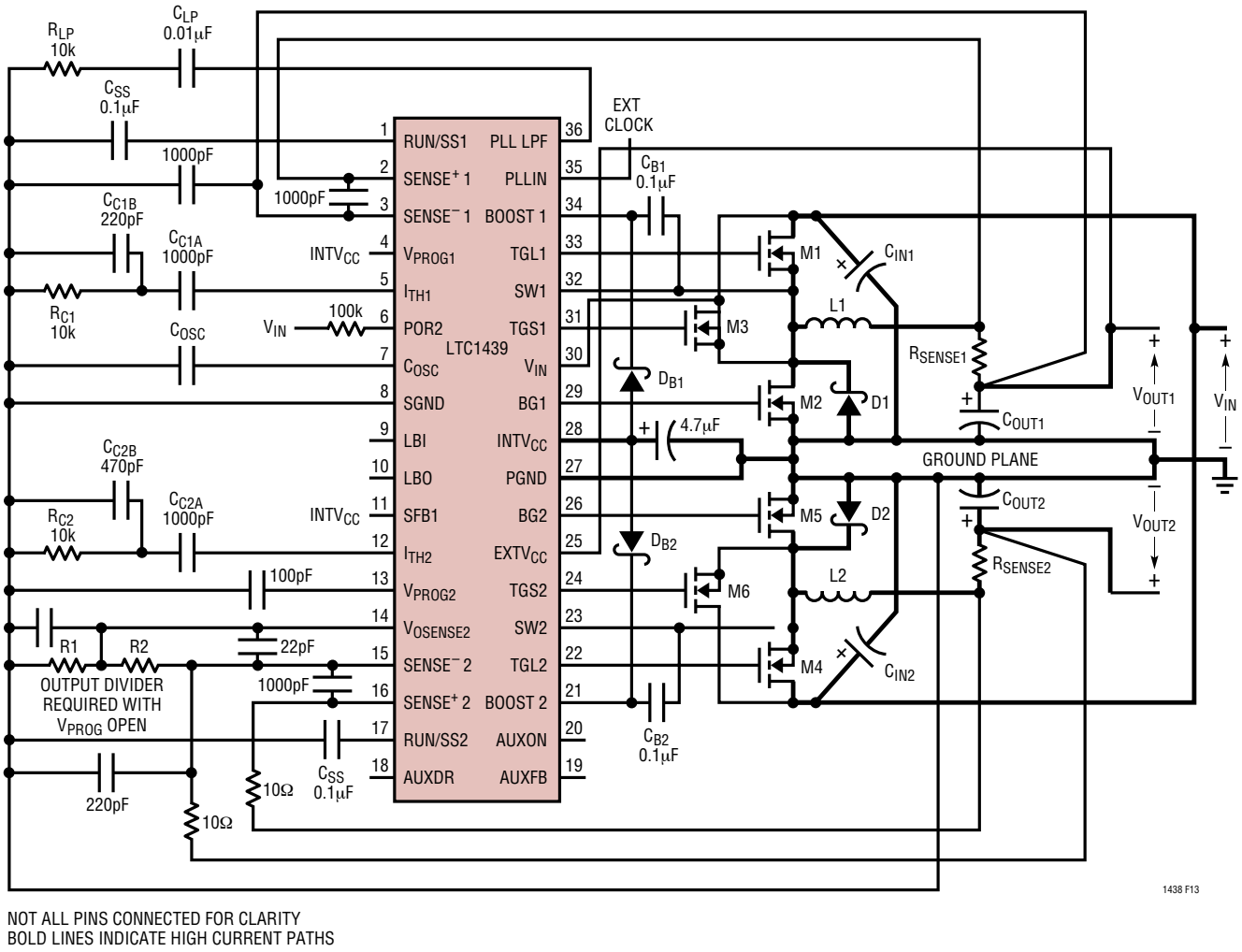

NOT ALL PINS CONNECTED FOR CLARITY
BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 13. LTC1439 Physical Layout Diagram

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1438/LTC1439. These items are also illustrated graphically in the layout diagram of Figure 13. Check the following in your layout:

1. Are the high current power ground current paths using or running through any part of signal ground? The LTC1438/LTC1438X/LTC1439 ICs have their sensitive pins on one side of the package. These pins include the signal ground for the reference, the oscillator input, the voltage and current sensing for both controllers and the low-battery/comparator input. The signal ground area used on this side of the IC must return to the bottom plates of all of the output capacitors. The high current power loops formed by the input capacitors and the ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes and (–) plates of C_{IN}, should be as short as possible and tied through a low resistance path to the bottom plates of the output capacitors for the ground return.
2. Do the LTC1438/LTC1439 SENSE$^-$1 and $V_{OSENSE2}$ pins connect to the (+) plates of C_{OUT}? In adjustable applications, the resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground and the HF decoupling capacitor should be as close as possible to the LTC1438/LTC1439.

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3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitors between SENSE$^+$1 (SENSE$^+$2) and SENSE$^-$1 (SENSE$^-$2) should be as close as possible to the LTC1438/LTC1439.
4. Do the (+) plates of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs.
5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents.
6. Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC1438/LTC1439.
7. Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

PC Board Layout Suggestions

Switching power supply printed circuit layouts are certainly among the most difficult analog circuits to design. The following suggestions will help to get a reasonably close solution on the first try.

The output circuits, including the external switching MOSFETs, inductor, secondary windings, sense resistor, input capacitors and output capacitors all have very large voltage and/or current levels associated with them. These components and the radiated fields (electrostatic and/or electromagnetic) **must** be kept away from the very sensitive control circuitry and loop compensation components required for a current mode switching regulator.

The electrostatic or capacitive coupling problems can be reduced by increasing the distance from the radiator, typically a very large or very fast moving voltage signal. The signal points that cause problems generally include: the "switch" node, any secondary flyback winding voltage and any nodes which also move with these nodes. The switch, MOSFET gate and boost nodes move between V_{IN} and PGND each cycle with less than a 100ns transition time. The secondary flyback winding output has an AC signal component of $-V_{IN}$ times the turns ratio of the transformer, and also has a similar <100ns transition time. The feedback control input signals need to have less than a few millivolts of noise in order for the regulator to perform properly. A rough calculation shows that 80dB of isolation at 2MHz is required from the switch node for low noise switcher operation. The situation is worse by a factor of the turns ratio for the secondary flyback winding. Keep these switch node related PC traces small and away from the "quiet" side of the IC (not just above and below each other on the opposite side of the board).

The electromagnetic or current loop induced feedback problems can be minimized by keeping the high AC current (transmitter) paths **and** the feedback circuit (receiver) path small and/or short. Maxwell's equations are at work here, trying to disrupt our clean flow of current and voltage information from the output back to the controller input. It is crucial to understand and minimize the susceptibility of the control input stage as well as the more obvious reduction of radiation from the high current output stage(s). An inductive transmitter depends upon the frequency, current amplitude and the size of the current loop to determine the radiation characteristic of the generated field. The current levels are set in the output stage once the input voltage, output voltage and inductor value(s) have been selected. The frequency is set by the output stage transition times. The only parameter over which we have some control is the size of the antenna we create on the PC board, i.e., the loop. A loop is formed with the input capacitance, the top MOSFET, the Schottky diode and the path from the Schottky diode's ground connection and the input capacitor's ground connection. A second path is formed when a secondary winding is used comprising the secondary output capacitor, the secondary winding and the rectifier diode or switching MOSFET (in the case of a synchronous approach). These "loops" should be kept as small and tightly packed as possible in order to minimize their "far field" radiation effects. The radiated field produced is picked up by the current comparator input filter circuit(s), as well as by the voltage feedback circuit(s). The current comparator's filter capacitor placed across the sense pins attenuates the radiated current signal. It is important to place this capacitor immediately adjacent to the IC sense pins. The voltage sensing input(s) minimizes the inductive pickup component by using an input capacitance filter to SGND. The capacitors in both case serve to integrate the induced

APPLICATIONS INFORMATION

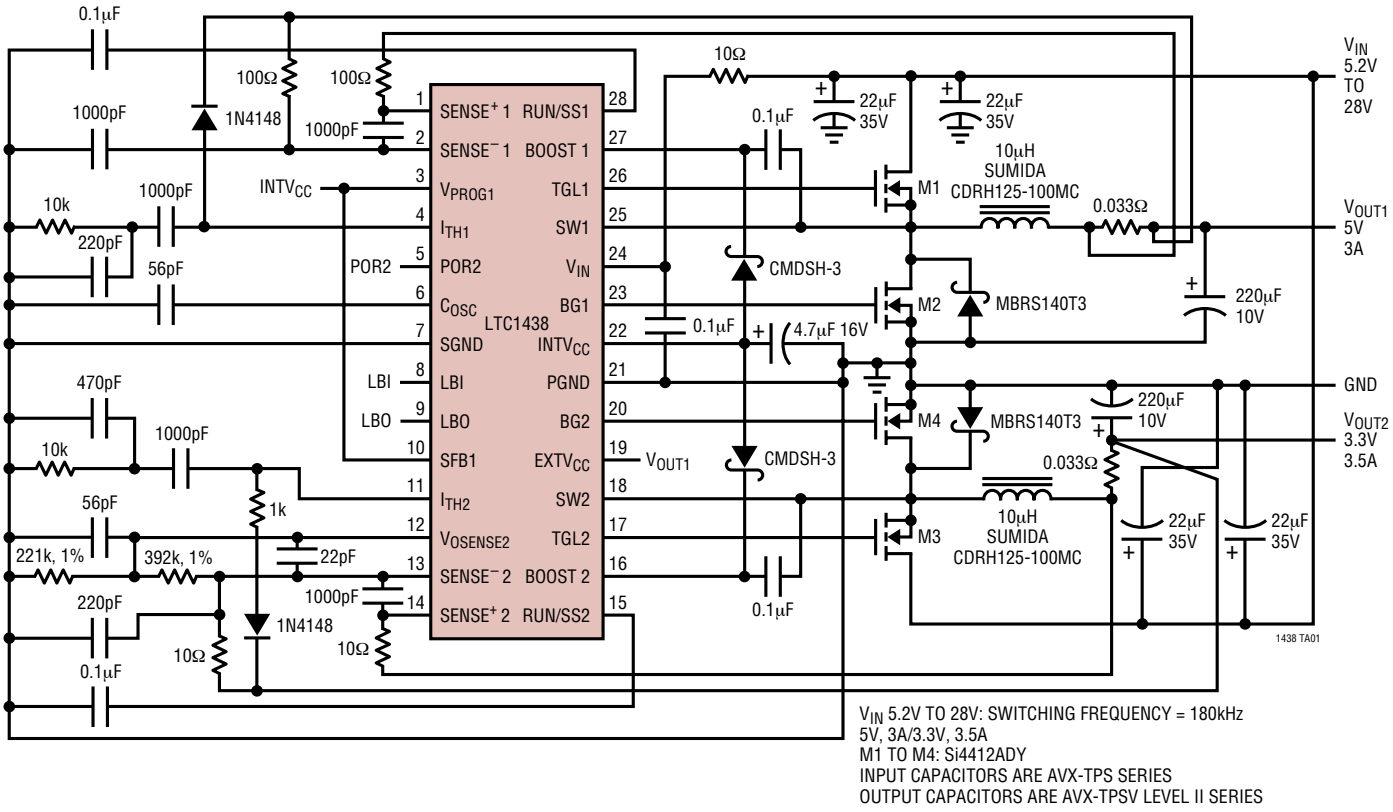
current, reducing the susceptibility to both the "loop" radiated magnetic fields and the transformer or inductor leakage fields.

The capacitor on $INTV_{CC}$ acts as a reservoir to supply the high transient currents to the bottom gates *and* to recharge the boost capacitor. This capacitor should be a 4.7µF tantalum capacitor placed as close as possible to the $INTV_{CC}$ and PGND pins of the IC. Peak current driving the MOSFET gates exceeds 1A. The PGND pin of the IC, connected to this capacitor, should connect directly to the lower plates of the output capacitors to minimize the AC ripple on the $INTV_{CC}$ IC power supply.

The previous instructions will yield a PC layout which has three separate ground regions returning separately to the bottom plates of the output capacitors: a signal ground, a MOSFET gate/$INTV_{CC}$ ground and the ground from the input capacitors, Schottky diode and synchronous MOSFET. In practice, this may produce a long power ground path from the input and output capacitors. A long, low resistance path between the input and output capacitor power grounds will not upset the operation of the switching controllers as long as the signal and power grounds from the IC pins does not "tap in" along this path.

TYPICAL APPLICATIONS

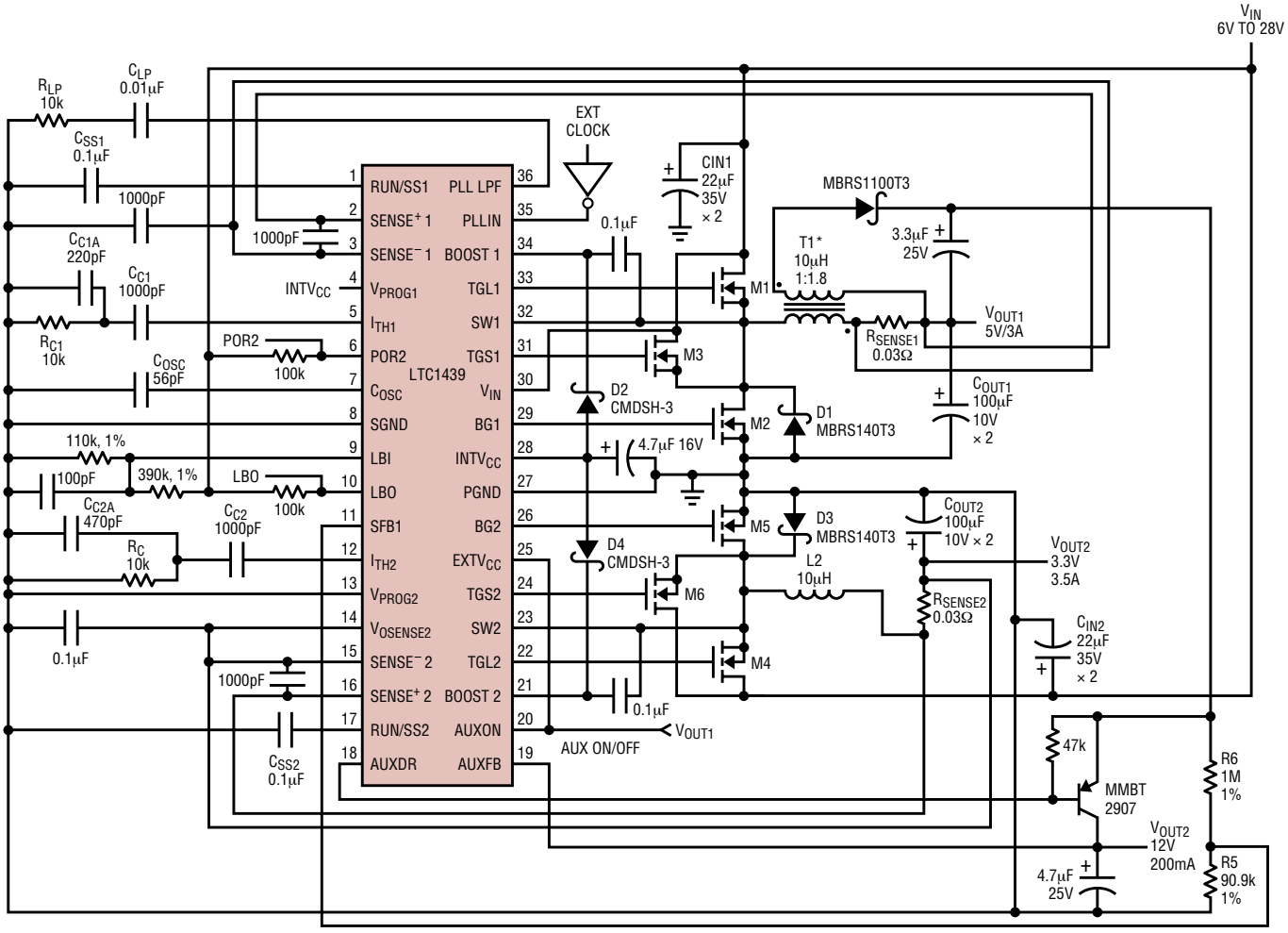
LTC1438 5V/3A, 3.3V/3.5A Regulator



V_{IN} 5.2V TO 28V: SWITCHING FREQUENCY = 180kHz
5V, 3A/3.3V, 3.5A
M1 TO M4: Si4412ADY
INPUT CAPACITORS ARE AVX-TPS SERIES
OUTPUT CAPACITORS ARE AVX-TPSV LEVEL II SERIES

TYPICAL APPLICATIONS

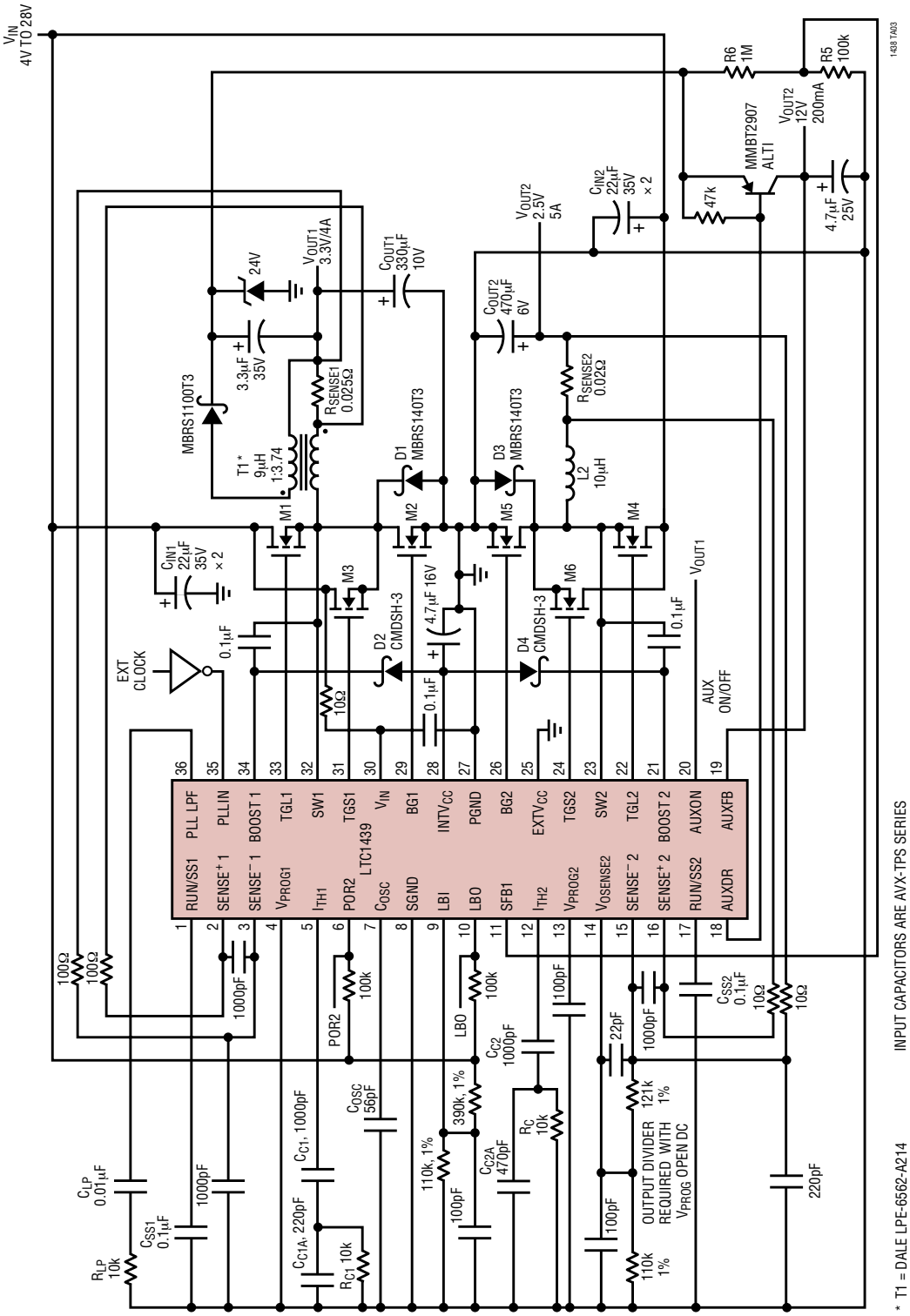
LTC1439 High Efficiency Low Noise 5V/3A, 3.3V/3.5A and 12V/200mA Regulator



* T1 = DALE LPE-6562-A262 GAPPED E-CORE
BH ELECTRONICS 501-0657 GAPPED TOROID
M1, M2, M4, M5 = IRF7403
M3, M6 = IRLML2803
L2 = SUMIDA CDRH125-100MC
ALL INPUT OUTPUT CAPACITORS ARE AVX-TPS SERIES

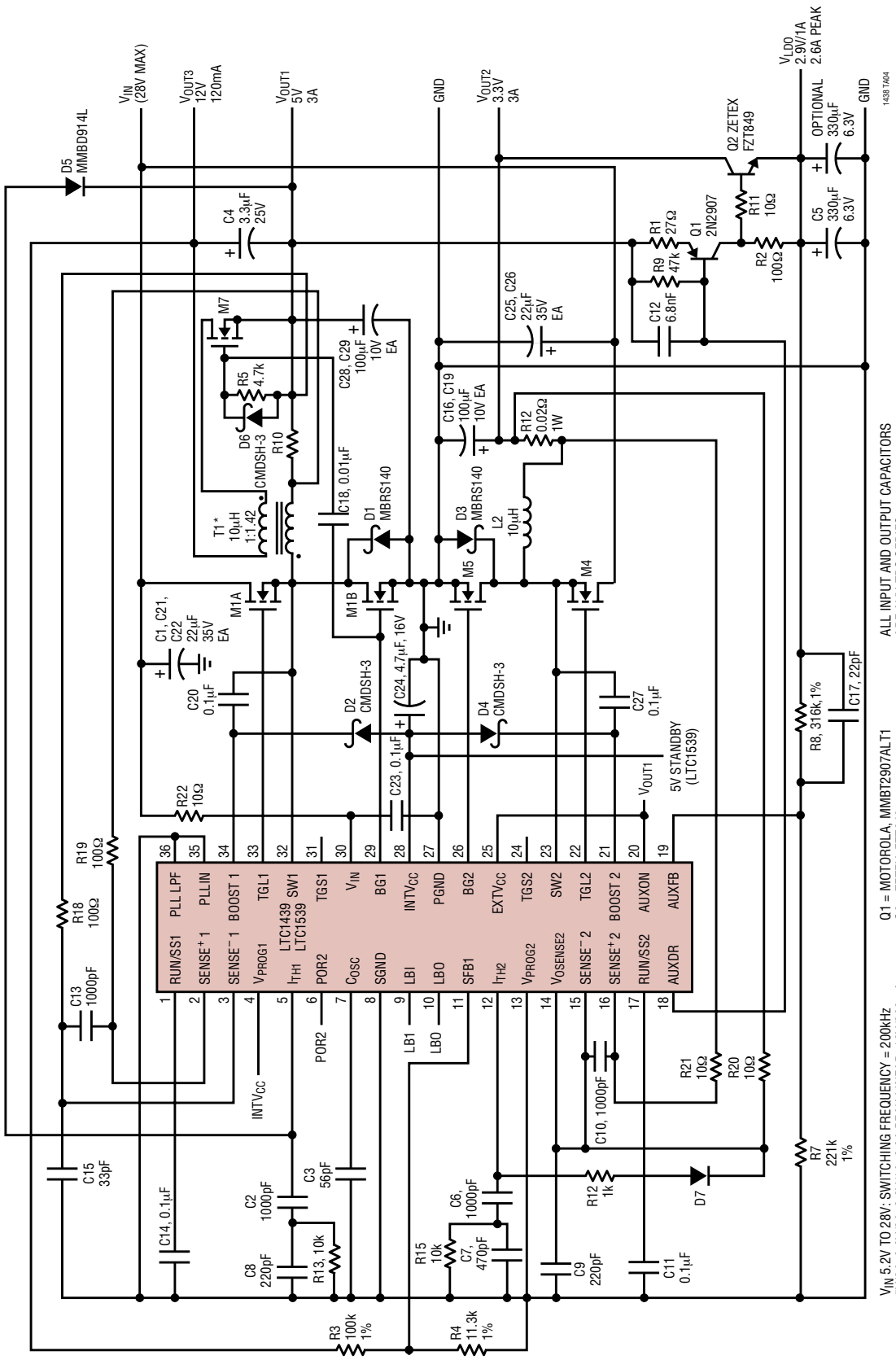
TYPICAL APPLICATIONS

LTC1439 High Effciency 3.3V/2.5V Regulator with Low Noise 12V Linear Regulator

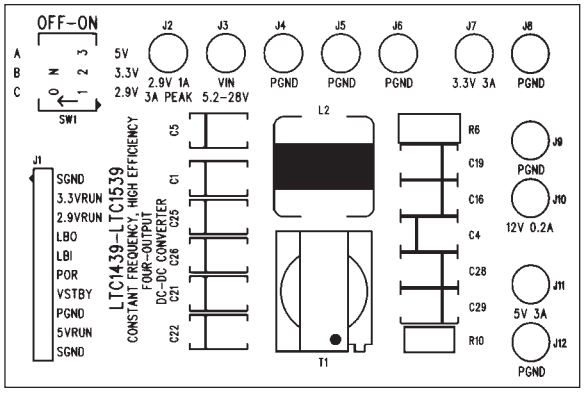


TYPICAL APPLICATIONS

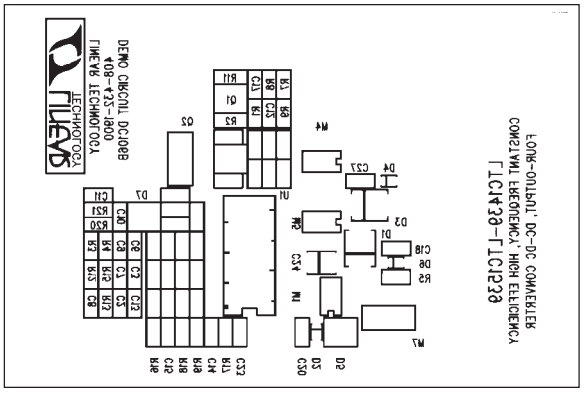
LTC1439/LTC1539 4-Output High Efficiency Low Noise 5V/3A, 3.3V/3A, 2.9V/2.6A, 12V/200mA Notebook Computer Power Supply
(See PCB LAYOUT AND FILM for Layout of Schematic)



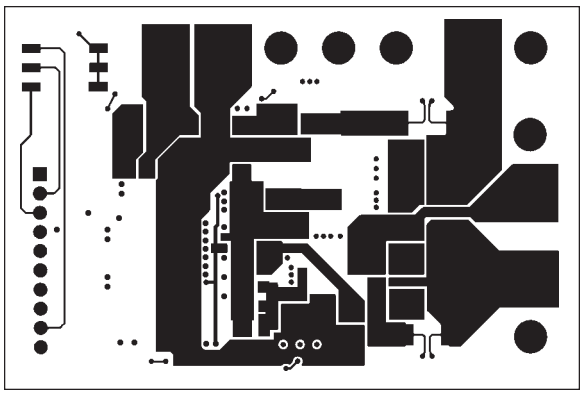
PCB LAYOUT AND FILM (Gerber files for this circuit board are available. Call LTC Marketing.)



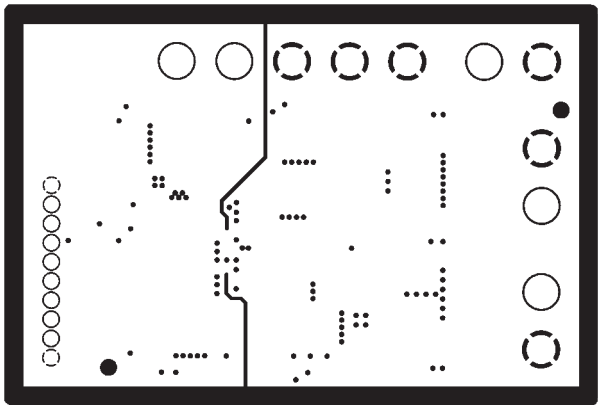
Silkscreen Top



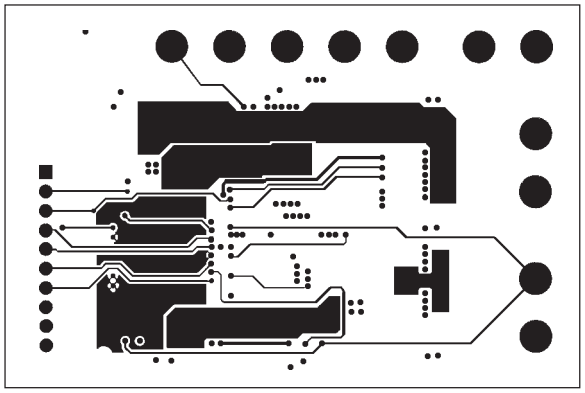
Silkscreen Bottom



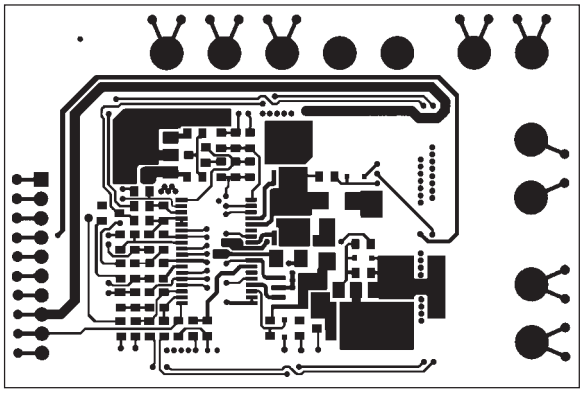
Copper Layer 1



Copper Layer 2 Ground Plane



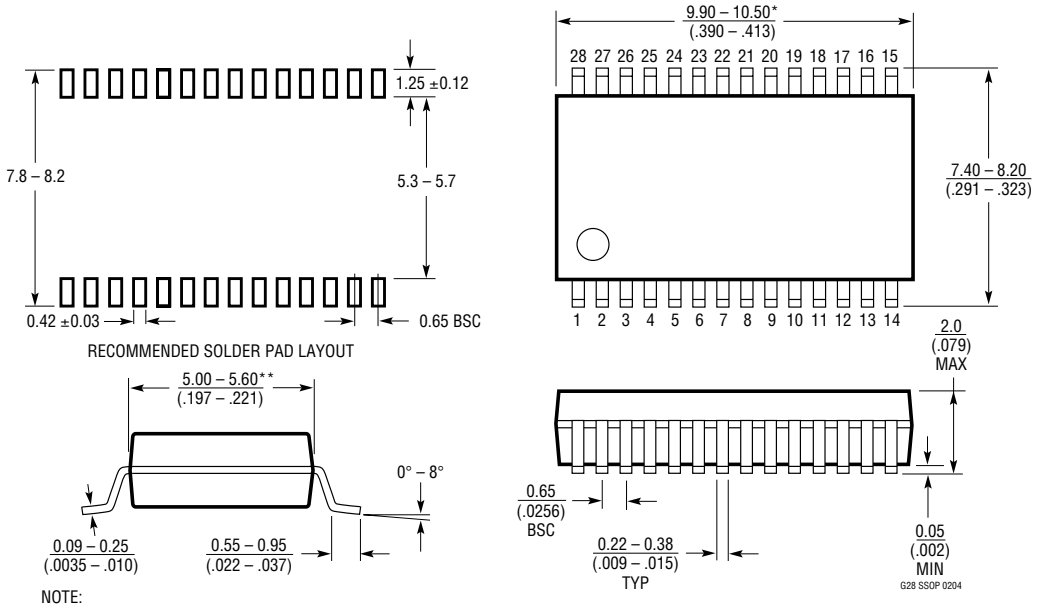
Copper Layer 3



Copper Layer 4

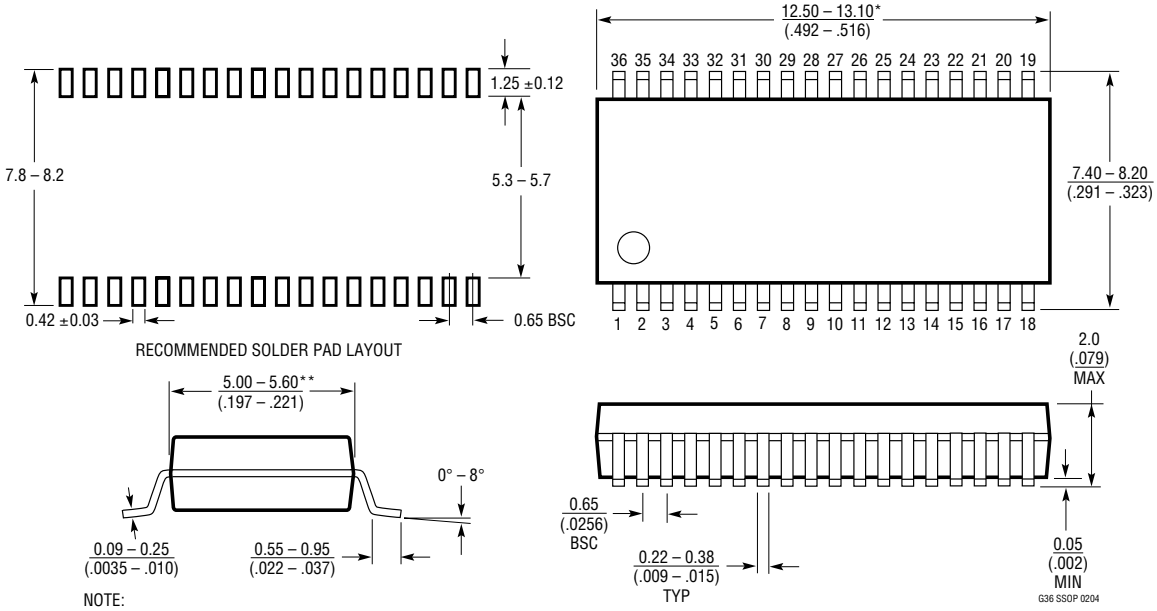
PACKAGE DESCRIPTION

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

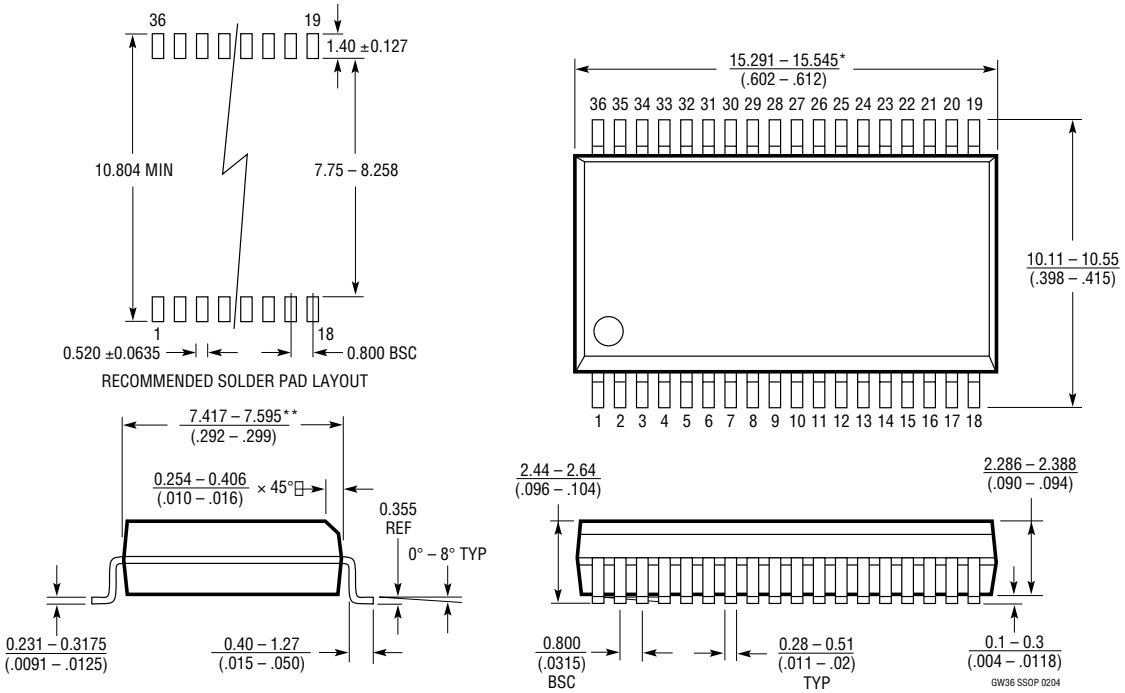
G Package
36-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

GW Package
36-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

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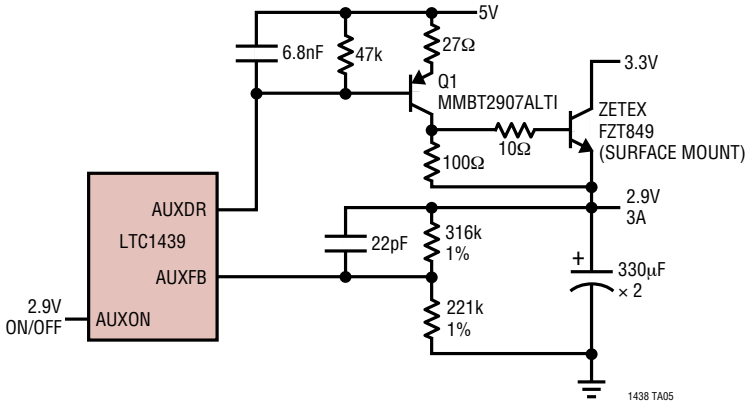
TYPICAL APPLICATION

3.3V to 2.9V at 3A Low Noise Linear Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1159	High Efficiency Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LT®1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LTC1436/LTC1436-PLL/ LTC1437	High Efficiency Low Noise Synchronous Step-Down Switching Regulator Controllers	Full-Featured Single Controller
LT1510	Constant-Voltage/Constant-Current Battery Charger	1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger
LTC1538-AUX	Dual, Synchronous Controller with AUX Regulator	5V Standby in Shutdown
LTC1539	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator Controller	5V Standby in Shutdown
LTC1778	Fast Step-Down Synchronous Controller	Fast Transient Response; No R_{SENSE}
LTC3728	2-Phase, Dual Synchronous Step-Down Controller	Minimum C_{IN} and C_{OUT}, 550kHz/Phase; Current Mode

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