High Voltage, Low Noise Zero-Drift Operational Amplifier

FEATURES

- **Supply Voltage Range**
  - **4.75V to 36V (LTC2057)**
  - **4.75V to 60V (LTC2057HV)**
- **Offset Voltage: 4µV (Maximum)**
- **Offset Voltage Drift: 0.015µV/°C (Maximum, –40°C to 125°C)**
- **Input Noise Voltage**
  - **200nV$_{P-P}$, DC to 10Hz (Typ)**
  - **11nV/√Hz, 1kHz (Typ)**
- Input Common Mode Range: V^- – 0.1V to V^+ – 1.5V
- Rail-to-Rail Output
- Unity Gain Stable
- Gain Bandwidth Product: 1.5MHz (Typ)
- Slew Rate: 0.45V/µs (Typ)
- A_{VOL}: 150dB (Typ)
- PSRR: 160dB (Typ)
- CMRR: 150dB (Typ)
- Shutdown Mode

APPLICATIONS

- High Resolution Data Acquisition
- Reference Buffering
- Test and Measurement
- Electronic Scales
- Thermocouple Amplifiers
- Strain Gauges
- Low-Side Current Sense
- Automotive Monitors and Control

DESCRIPTION

The LTC®2057 is a high voltage, low noise, zero-drift operational amplifier that offers precision DC performance over a wide supply range of 4.75V to 36V or 4.75V to 60V for the LTC2057HV. Offset voltage and 1/f noise are suppressed, allowing this amplifier to achieve a maximum offset voltage of 4µV and a DC to 10Hz input noise voltage of 200nV$_{P-P}$ (typ). The LTC2057's self-calibrating circuitry results in low offset voltage drift with temperature, 0.015µV/°C (max), and zero-drift over time. The amplifier also features an excellent power supply rejection ratio (PSRR) of 160dB and a common mode rejection ratio (CMRR) of 150dB (typ).

The LTC2057 provides rail-to-rail output swing and an input common mode range that includes the V^- rail (V^- – 0.1V to V^+ – 1.5V). In addition to low offset and noise, this amplifier features a 1.5MHz (typ) gain-bandwidth product and a 0.45V/µs (typ) slew rate.

Wide supply range, combined with low noise, low offset, and excellent PSRR and CMRR make the LTC2057 and LTC2057HV well suited for high dynamic-range test, measurement, and instrumentation systems.

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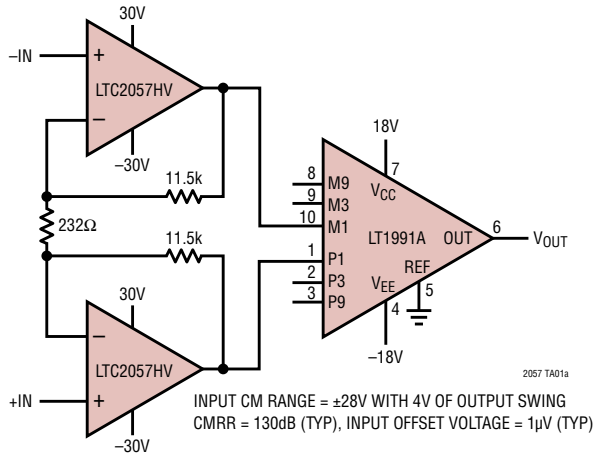
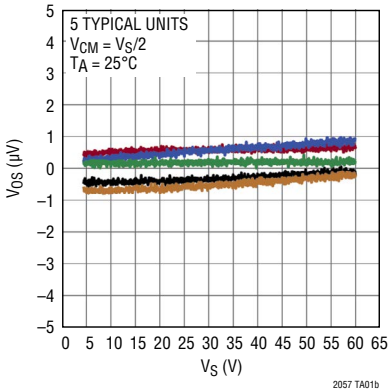
TYPICAL APPLICATION

Wide Input Range Precision Gain-of-100 Instrumentation Amplifier



INPUT CM RANGE = ±28V WITH 4V OF OUTPUT SWING
CMRR = 130dB (TYP), INPUT OFFSET VOLTAGE = 1µV (TYP)

Input Offset Voltage vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)
- LTC2057 ..... 40V
- LTC2057HV 65V

Input Voltage
- –IN, +IN ..... V^- – 0.3V to V^+ + 0.3V
- $\overline{SD}$, SDCOM ..... V^- – 0.3V to V^+ + 0.3V

Input Current
- –IN, +IN ..... ±10mA
- $\overline{SD}$, SDCOM ..... ±10mA

Differential Input Voltage
- –IN – +IN ..... ±6V
- $\overline{SD}$ – SDCOM ..... –0.3V to 5.3V

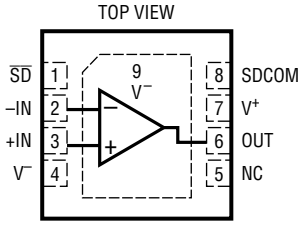
Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range (Note 2)
- LTC2057I/LTC2057HVI ..... –40°C to 85°C
- LTC2057H/LTC2057HVH ..... –40°C to 125°C

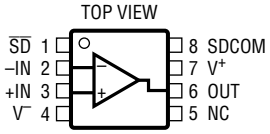
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

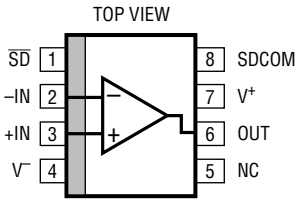
PIN CONFIGURATION



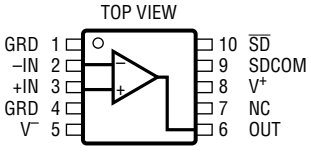
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS V^-
PCB CONNECTION REQUIRED



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 120°C/W



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2057IDD#PBF	LTC2057IDD#TRPBF	LGCZ	8-Lead Plastic DFN (3mm × 3mm)	–40°C to 85°C
LTC2057HVIDD#PBF	LTC2057HVIDD#TRPBF	LGDB	8-Lead Plastic DFN (3mm × 3mm)	–40°C to 85°C
LTC2057HDD#PBF	LTC2057HDD#TRPBF	LGCZ	8-Lead Plastic DFN (3mm × 3mm)	–40°C to 125°C
LTC2057HVHDD#PBF	LTC2057HVHDD#TRPBF	LGDB	8-Lead Plastic DFN (3mm × 3mm)	–40°C to 125°C
LTC2057IMS8#PBF	LTC2057IMS8#TRPBF	LTFGK	8-Lead Plastic MSOP	–40°C to 85°C
LTC2057HVIMS8#PBF	LTC2057HVIMS8#TRPBF	LTGDC	8-Lead Plastic MSOP	–40°C to 85°C
LTC2057HMS8#PBF	LTC2057HMS8#TRPBF	LTFGK	8-Lead Plastic MSOP	–40°C to 125°C
LTC2057HVHMS8#PBF	LTC2057HVHMS8#TRPBF	LTGDC	8-Lead Plastic MSOP	–40°C to 125°C
LTC2057IMS#PBF	LTC2057IMS#TRPBF	LTGCX	10-Lead Plastic MSOP	–40°C to 85°C
LTC2057HVIMS#PBF	LTC2057HVIMS#TRPBF	LTGCY	10-Lead Plastic MSOP	–40°C to 85°C
LTC2057HMS#PBF	LTC2057HMS#TRPBF	LTGCX	10-Lead Plastic MSOP	–40°C to 125°C
LTC2057HVHMS#PBF	LTC2057HVHMS#TRPBF	LTGCY	10-Lead Plastic MSOP	–40°C to 125°C
LTC2057IS8#PBF	LTC2057IS8#TRPBF	2057	8-Lead Plastic Small Outline	–40°C to 85°C
LTC2057HVIS8#PBF	LTC2057HVIS8#TRPBF	2057HV	8-Lead Plastic Small Outline	–40°C to 85°C
LTC2057HS8#PBF	LTC2057HS8#TRPBF	2057	8-Lead Plastic Small Outline	–40°C to 125°C
LTC2057HVHS8#PBF	LTC2057HVHS8#TRPBF	2057HV	8-Lead Plastic Small Outline	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(LTC2057/LTC2057HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = ±2.5V; V_{CM} = V_{OUT} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 3)				0.5	4	µV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift (Note 3)	–40°C to 125°C	●			0.015	µV/°C
I_B	Input Bias Current (Note 4)				30	200	pA
		–40°C to 85°C	●			300	pA
		–40°C to 125°C	●			3.5	nA
I_{OS}	Input Offset Current (Note 4)				60	400	pA
		–40°C to 85°C	●			460	pA
		–40°C to 125°C	●			1.0	nA
i_n	Input Noise Current Spectral Density	1kHz			170		fA/√Hz
e_n	Input Noise Voltage Spectral Density	1kHz			11		nV/√Hz
$e_{n\ P-P}$	Input Noise Voltage	DC to 10Hz			200		nV_{P-P}
C_{IN}	Differential Input Capacitance				3		pF
	Common Mode Input Capacitance				3		pF
CMRR	Common Mode Rejection Ratio (Note 5)	V_{CM} = V^- – 0.1V to V^+ – 1.5V		114	150		dB
		–40°C to 125°C	●	111			dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 4.75V to 36V		133	160		dB
		–40°C to 125°C	●	129			dB
A_{VOL}	Open Loop Voltage Gain (Note 5)	V_{OUT} = V^- +0.2V to V^+ –0.2V, R_L =1kΩ		118	150		dB
		–40°C to 125°C	●	117			dB
$V_{OL} – V^-$	Output Voltage Swing Low	No Load			0.2	10	mV
		–40°C to 125°C	●			15	mV
		I_{SINK} = 1mA			35	60	mV
		–40°C to 125°C	●			90	mV
		I_{SINK} = 5mA			180	270	mV
		–40°C to 85°C	●			365	mV
		–40°C to 125°C	●			415	mV
$V^+ – V_{OH}$	Output Voltage Swing High	No Load			0.2	10	mV
		–40°C to 125°C	●			15	mV
		I_{SOURCE} = 1mA			50	75	mV
		–40°C to 125°C	●			115	mV
		I_{SOURCE} = 5mA			250	345	mV
		–40°C to 85°C	●			470	mV
		–40°C to 125°C	●			535	mV
I_{SC}	Short Circuit Current			17	26		mA
SR_{RISE}	Rising Slew Rate	A_V = –1, R_L = 10kΩ			1.2		V/µs
SR_{FALL}	Falling Slew Rate	A_V = –1, R_L = 10kΩ			0.45		V/µs
GBW	Gain Bandwidth Product				1.5		MHz
f_C	Internal Chopping Frequency				100		kHz
I_S	Supply Current	No Load			0.8	1.21	mA
		–40°C to 85°C	●			1.50	mA
		–40°C to 125°C	●			1.70	mA
		In Shutdown Mode			2.5		µA
		–40°C to 85°C	●			5.6	µA
		–40°C to 125°C	●			6.5	µA
V_{SDL}	Shutdown Threshold ($\overline{SD}$ – SDCOM) Low	–40°C to 125°C	●			0.8	V
V_{SDH}	Shutdown Threshold ($\overline{SD}$ – SDCOM) High	–40°C to 125°C	●	2			V
	SDCOM Voltage Range	–40°C to 125°C	●	V^-		V^+ –2V	V
$I_{\overline{SD}}$	$\overline{SD}$ Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●	–2	–0.5		µA
I_{SDCOM}	SDCOM Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●		0.5	2	µA

ELECTRICAL CHARACTERISTICS

(LTC2057/LTC2057HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = ±15V; V_{CM} = V_{OUT} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 3)				0.5	4.5	µV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift (Note 3)	–40°C to 125°C	●			0.015	µV/°C
I_B	Input Bias Current (Note 4)				30	200	pA
		–40°C to 85°C	●			360	pA
		–40°C to 125°C	●			6.0	nA
I_{OS}	Input Offset Current (Note 4)				60	400	pA
		–40°C to 85°C	●			480	pA
		–40°C to 125°C	●			1.5	nA
i_n	Input Noise Current Spectral Density	1kHz			150		fA/√Hz
e_n	Input Noise Voltage Spectral Density	1kHz			12		nV/√Hz
$e_{n\ P-P}$	Input Noise Voltage	DC to 10Hz			210		nV_{P-P}
C_{IN}	Differential Input Capacitance				3		pF
	Common Mode Input Capacitance				3		pF
CMRR	Common Mode Rejection Ratio (Note 5)	V_{CM} = V^- – 0.1V to V^+ – 1.5V		128	150		dB
		–40°C to 125°C	●	126			dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 4.75V to 36V		133	160		dB
		–40°C to 125°C	●	129			dB
A_{VOL}	Open Loop Voltage Gain (Note 5)	V_{OUT} = V^- +0.25V to V^+ –0.25V, R_L =10kΩ		130	150		dB
		–40°C to 125°C	●	128			dB
$V_{OL} – V^-$	Output Voltage Swing Low	No Load			2	12	mV
		–40°C to 125°C	●			45	mV
		I_{SINK} = 1mA			35	60	mV
		–40°C to 125°C	●			100	mV
		I_{SINK} = 5mA			175	255	mV
		–40°C to 85°C	●			360	mV
		–40°C to 125°C	●			435	mV
$V^+ – V_{OH}$	Output Voltage Swing High	No Load			3	15	mV
		–40°C to 125°C	●			45	mV
		I_{SOURCE} = 1mA			50	75	mV
		–40°C to 125°C	●			125	mV
		I_{SOURCE} = 5mA			235	335	mV
		–40°C to 85°C	●			465	mV
		–40°C to 125°C	●			560	mV
I_{SC}	Short Circuit Current			19	30		mA
SR_{RISE}	Rising Slew Rate	A_V = –1, R_L = 10kΩ			1.3		V/µs
SR_{FALL}	Falling Slew Rate	A_V = –1, R_L = 10kΩ			0.45		V/µs
GBW	Gain Bandwidth Product				1.5		MHz
f_C	Internal Chopping Frequency				100		kHz
I_S	Supply Current	No Load			0.88	1.35	mA
		–40°C to 85°C	●			1.65	mA
		–40°C to 125°C	●			1.83	mA
		In Shutdown Mode			3		µA
		–40°C to 85°C	●			8	µA
		–40°C to 125°C	●			9	µA
V_{SDL}	Shutdown Threshold ($\overline{SD}$ – SDCOM) Low	–40°C to 125°C	●			0.8	V
V_{SDH}	Shutdown Threshold ($\overline{SD}$ – SDCOM) High	–40°C to 125°C	●	2			V
	SDCOM Voltage Range	–40°C to 125°C	●	V–		V^+ –2V	V
$I_{\overline{SD}}$	$\overline{SD}$ Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●	–2.0	–0.5		µA
I_{SDCOM}	SDCOM Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●		0.5	2	µA

ELECTRICAL CHARACTERISTICS

(LTC2057HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_S = ±30V; V_{CM} = V_{OUT} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 3)				0.5	5	µV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift (Note 3)	–40°C to 125°C	●			0.025	µV/°C
I_B	Input Bias Current (Note 4)				30	200	pA
		–40°C to 85°C	●			455	pA
		–40°C to 125°C	●			11	nA
I_{OS}	Input Offset Current (Note 4)				60	400	pA
		–40°C to 85°C	●			500	pA
		–40°C to 125°C	●			3	nA
i_n	Input Noise Current Spectral Density	1kHz			130		fA/√Hz
e_n	Input Noise Voltage Spectral Density	1kHz			13		nV/√Hz
$e_{n\ P-P}$	Input Noise Voltage	DC to 10Hz			220		nV_{P-P}
C_{IN}	Differential Input Capacitance				3		pF
	Common Mode Input Capacitance				3		pF
CMRR	Common Mode Rejection Ratio (Note 5)	V_{CM} = V^- – 0.1V to V^+ – 1.5V		133	150		dB
		–40°C to 125°C	●	131			dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 4.75V to 60V		138	160		dB
		–40°C to 125°C	●	136			dB
A_{VOL}	Open Loop Voltage Gain (Note 5)	V_{OUT} = V^- +0.25V to V^+ – 0.25V, R_L = 10kΩ		135	150		dB
		–40°C to 125°C	●	130			dB
$V_{OL} – V^-$	Output Voltage Swing Low	No Load			3	15	mV
		–40°C to 125°C	●			45	mV
		I_{SINK} = 1mA			35	60	mV
		–40°C to 125°C	●			105	mV
		I_{SINK} = 5mA			175	260	mV
		–40°C to 85°C	●			370	mV
		–40°C to 125°C	●			445	mV
$V^+ – V_{OH}$	Output Voltage Swing High	No Load			3	15	mV
		–40°C to 125°C	●			45	mV
		I_{SOURCE} = 1mA			50	75	mV
		–40°C to 125°C	●			130	mV
		I_{SOURCE} = 5mA			235	335	mV
		–40°C to 85°C	●			475	mV
		–40°C to 125°C	●			575	mV
I_{SC}	Short Circuit Current			19	30		mA
SR_{RISE}	Rising Slew Rate	A_V = –1, R_L = 10kΩ			1.3		V/µs
SR_{FALL}	Falling Slew Rate	A_V = –1, R_L = 10kΩ			0.45		V/µs
GBW	Gain Bandwidth Product				1.5		MHz
f_C	Internal Chopping Frequency				100		kHz
IS	Supply Current	No Load			0.90	1.40	mA
		–40°C to 85°C	●			1.73	mA
		–40°C to 125°C	●			1.92	mA
		In Shutdown Mode			3		µA
		–40°C to 85°C	●			9	µA
		–40°C to 125°C	●			11	µA
V_{SDL}	Shutdown Threshold (SD – SDCOM) Low	–40°C to 125°C	●			0.8	V
V_{SDH}	Shutdown Threshold (SD – SDCOM) High	–40°C to 125°C	●	2			V
	SDCOM Voltage Range	–40°C to 125°C	●	V^-		V^+ –2V	V
$I_{\overline{SD}}$	$\overline{SD}$ Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●	–2	–0.5		µA
I_{SDCOM}	SDCOM Pin Current	–40°C to 125°C, $V_{\overline{SD}} – V_{SDCOM}$ = 0	●		0.5	2	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC2057I/LTC2057HVI are guaranteed to meet specified performance from –40°C to 85°C. The LTC2057H/LTC2057HVH are guaranteed to meet specified performance from –40°C to 125°C.

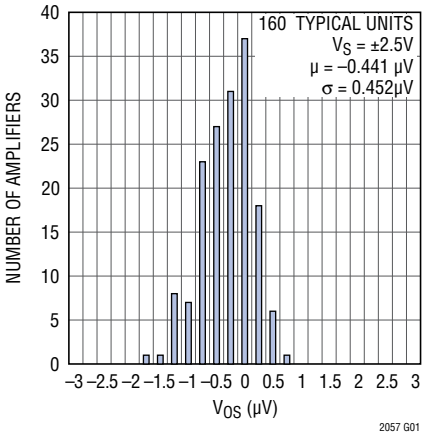
Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing. V_{OS} is measured to a limit determined by test equipment capability.

Note 4: These specifications are limited by automated test system capability. Leakage currents and thermocouple effects reduce test accuracy. For tighter specifications, please contact LTC Marketing.

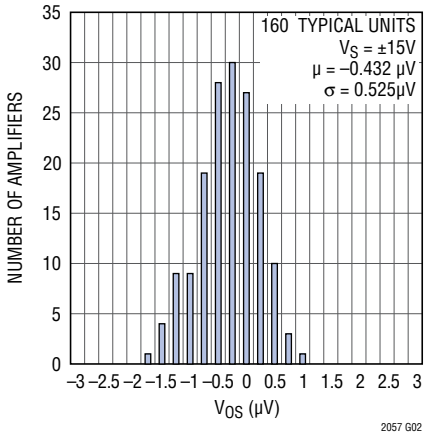
Note 5: Minimum specifications for these parameters are limited by the capabilities of the automated test system, which has an accuracy of approximately 10µV for V_{OS} measurements. For reference, 10µV/60V is 136dB, 10µV/30V is 130dB, and 10µV/5V is 114dB.

TYPICAL PERFORMANCE CHARACTERISTICS

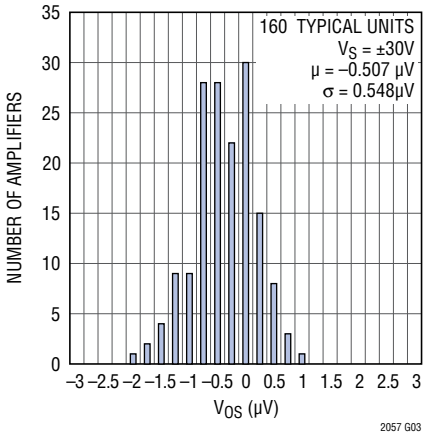
Input Offset Voltage Distribution



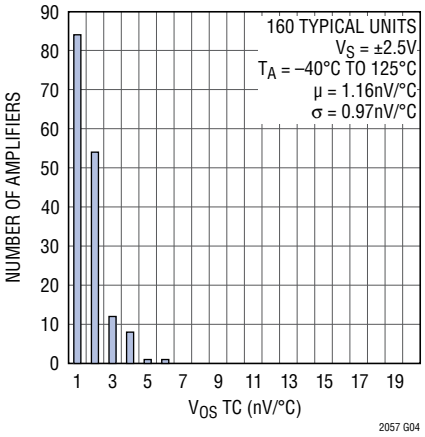
Input Offset Voltage Distribution



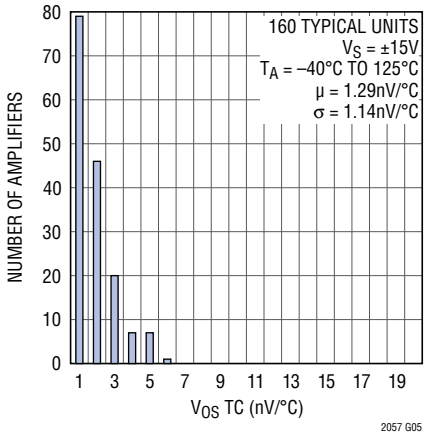
Input Offset Voltage Distribution



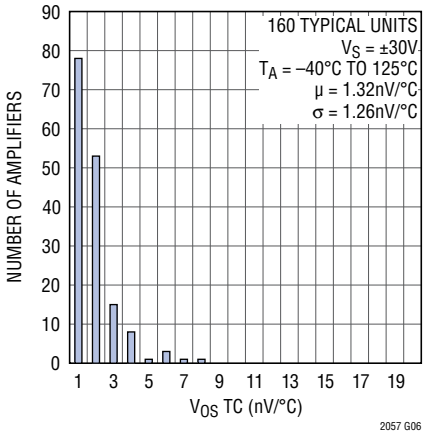
Input Offset Voltage Drift Distribution



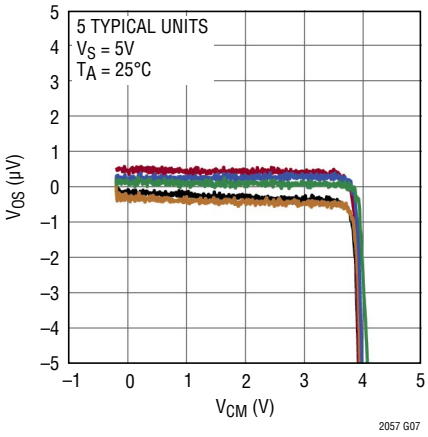
Input Offset Voltage Drift Distribution



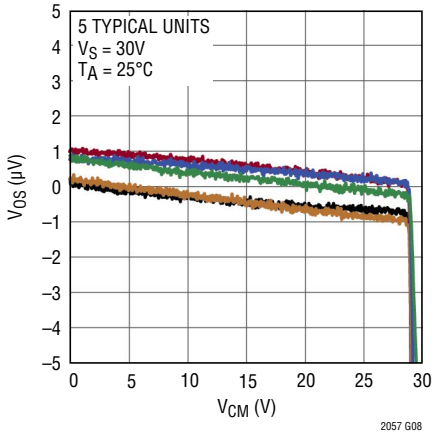
Input Offset Voltage Drift Distribution



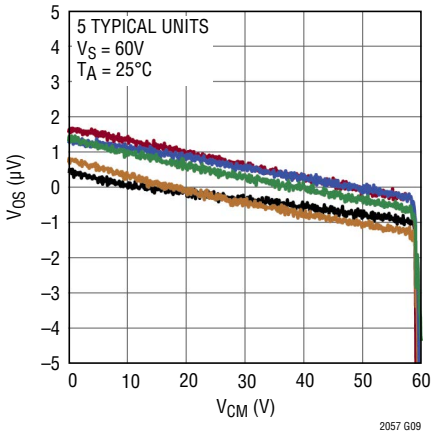
Input Offset Voltage vs Input Common Mode Voltage



Input Offset Voltage vs Input Common Mode Voltage

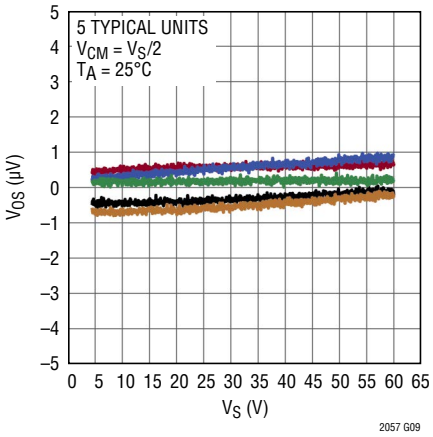


Input Offset Voltage vs Input Common Mode Voltage

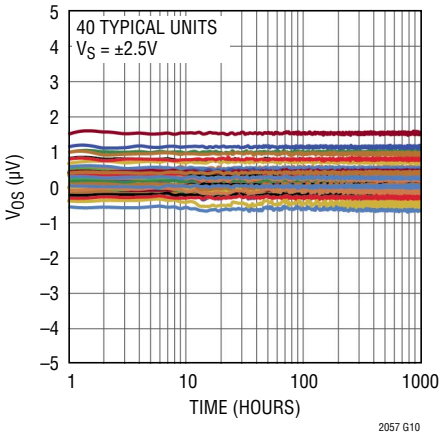


TYPICAL PERFORMANCE CHARACTERISTICS

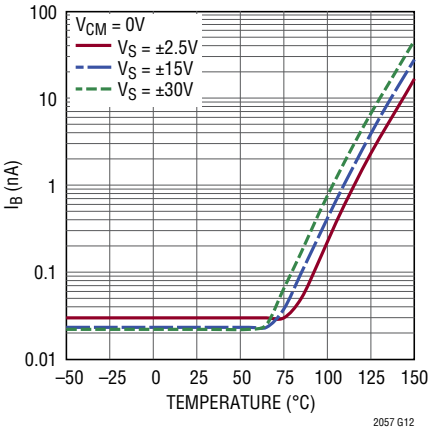
Input Offset Voltage vs Supply Voltage



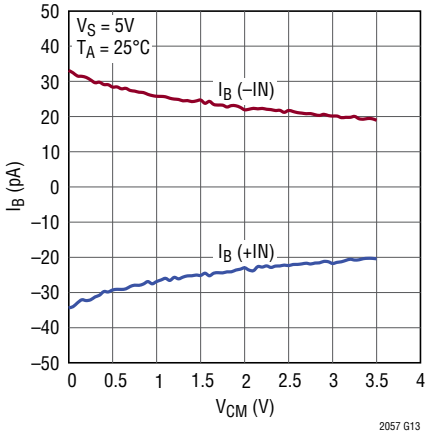
Long-Term Input Offset Voltage Drift



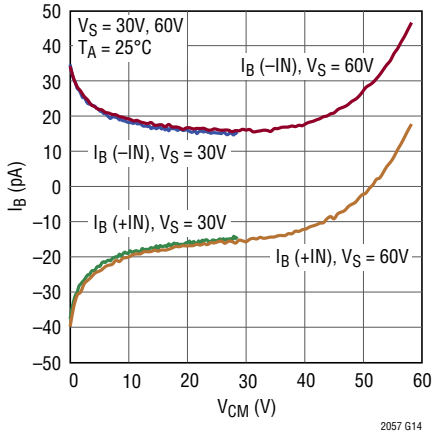
Input Bias Current vs Temperature



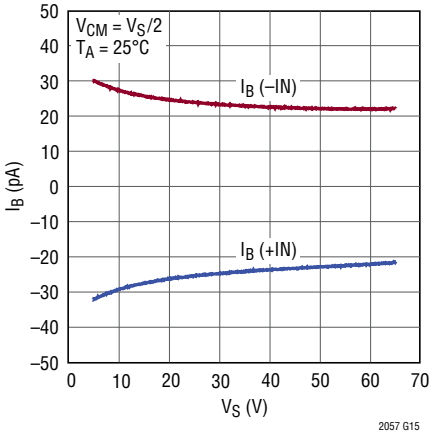
Input Bias Current vs Input Common Mode Voltage



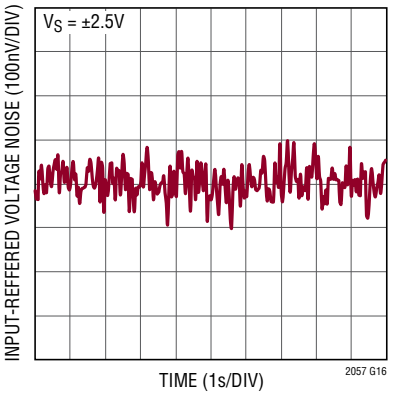
Input Bias Current vs Input Common Mode Voltage



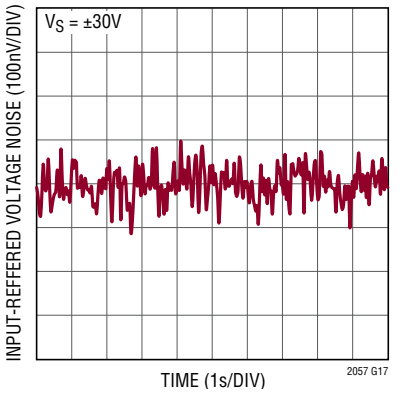
Input Bias Current vs Supply Voltage



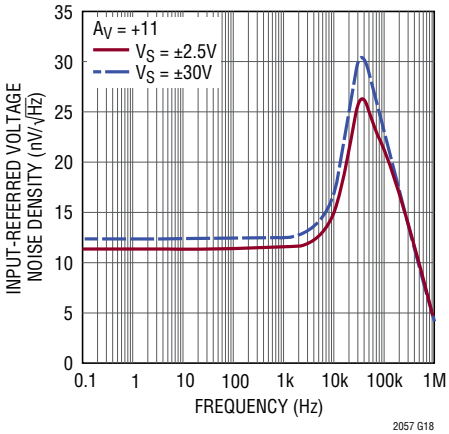
DC to 10Hz Voltage Noise



DC to 10Hz Voltage Noise

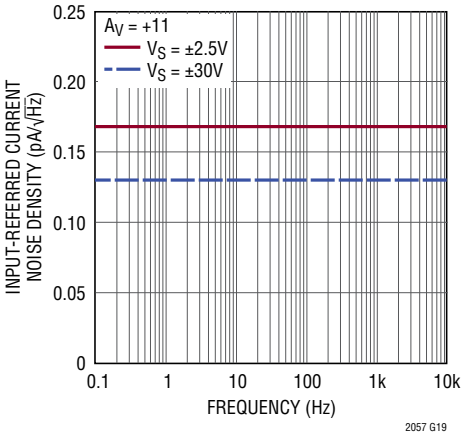


Input Voltage Noise Spectrum

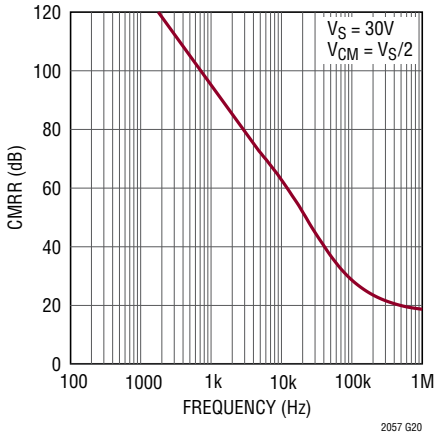


TYPICAL PERFORMANCE CHARACTERISTICS

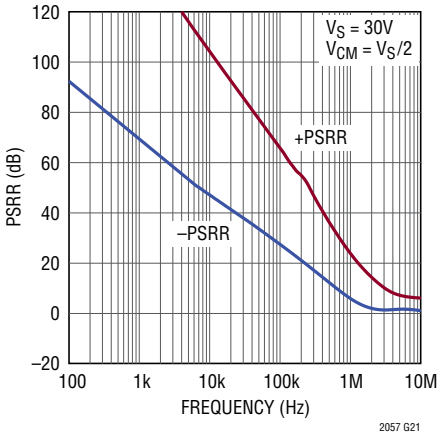
Input Current Noise Spectrum



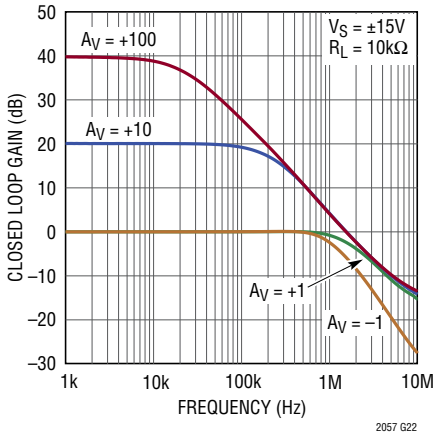
Common Mode Rejection Ratio vs Frequency



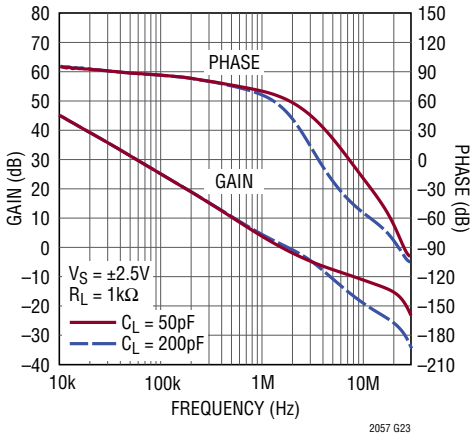
Power Supply Rejection Ratio vs Frequency



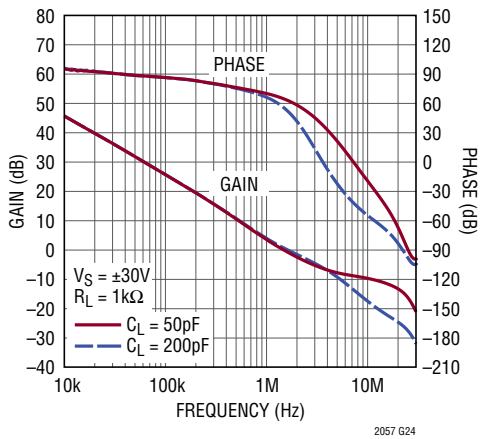
Closed Loop Gain vs Frequency



Gain/Phase vs Frequency

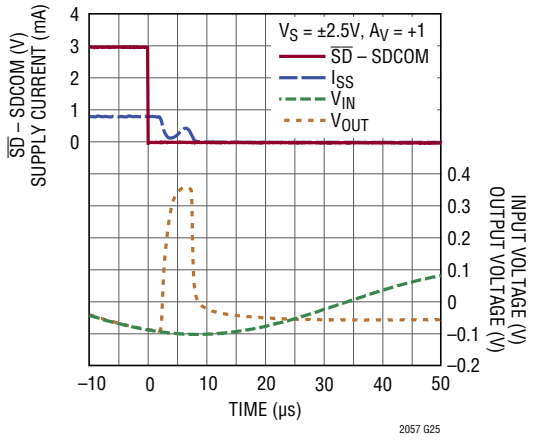


Gain/Phase vs Frequency

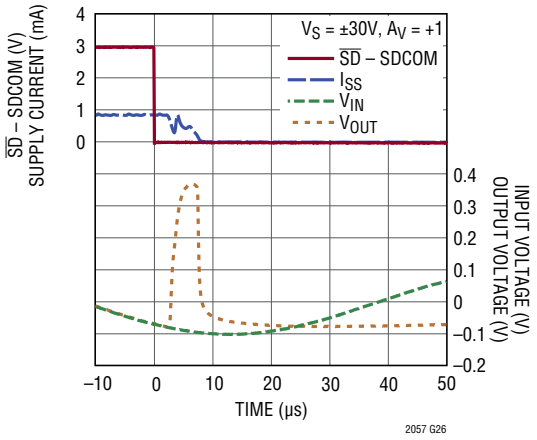


TYPICAL PERFORMANCE CHARACTERISTICS

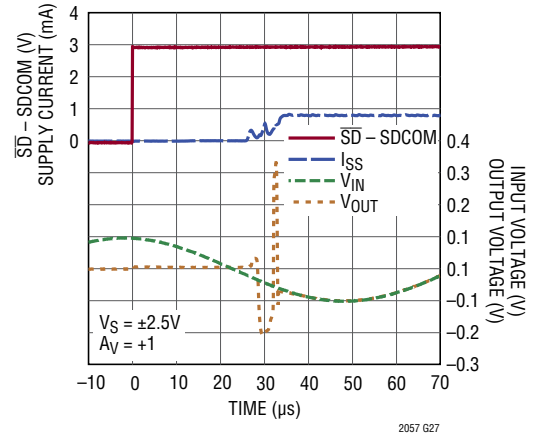
Shutdown Transient with Sinusoid Input



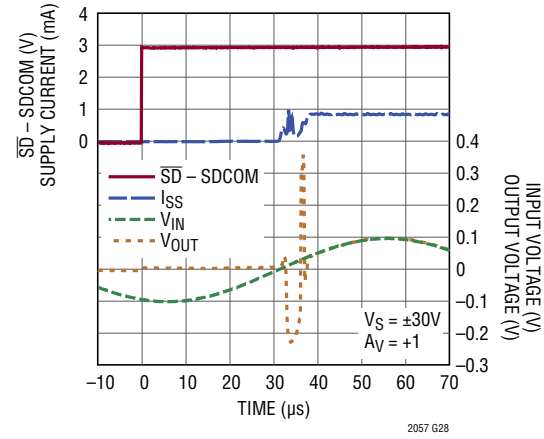
Shutdown Transient with Sinusoid Input



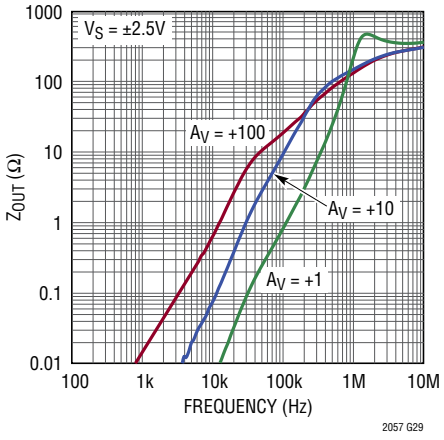
Start-Up Transient with Sinusoid Input



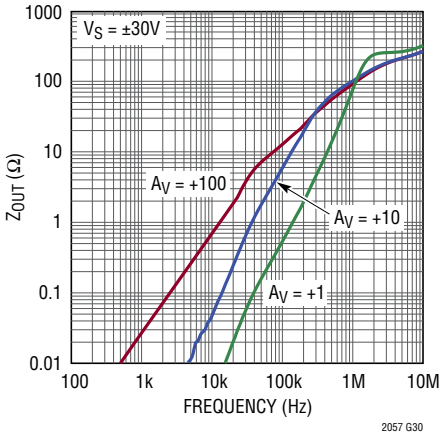
Start-Up Transient with Sinusoid Input



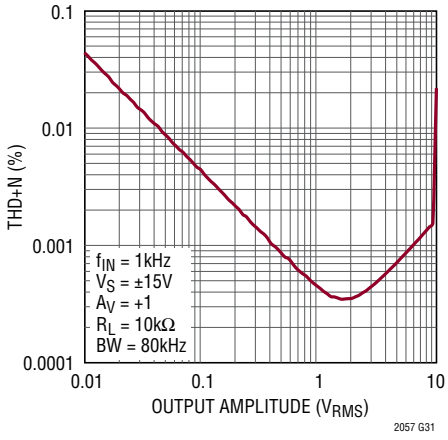
Closed Loop Output Impedance vs Frequency



Closed Loop Output Impedance vs Frequency

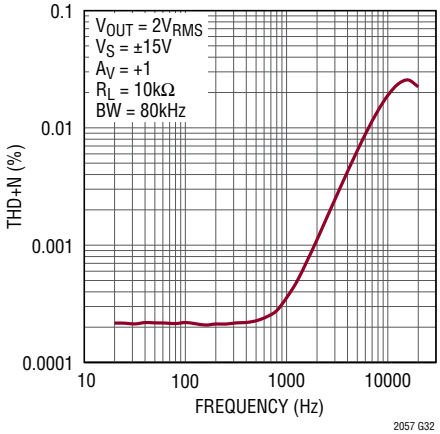


THD+N vs Amplitude

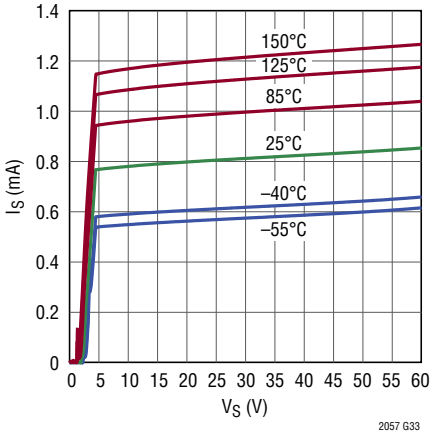


TYPICAL PERFORMANCE CHARACTERISTICS

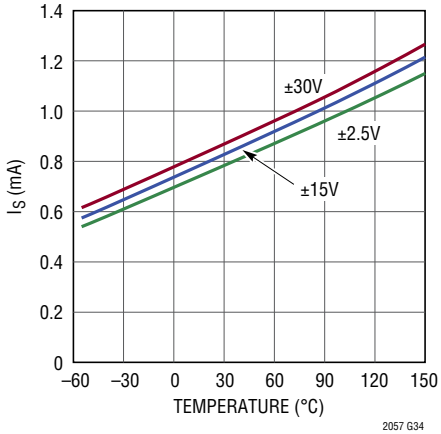
THD+N vs Frequency



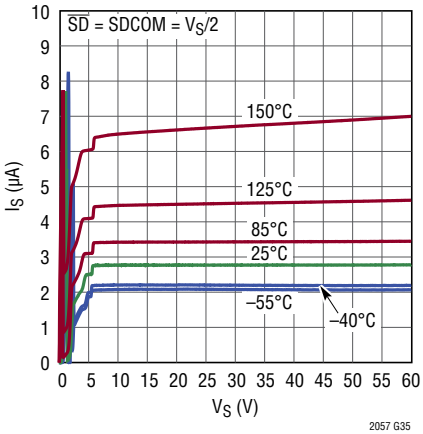
Supply Current vs Supply Voltage



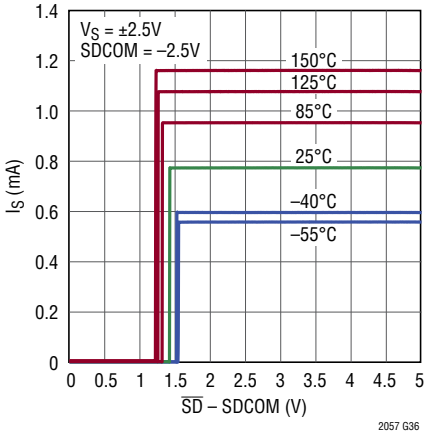
Supply Current vs Temperature



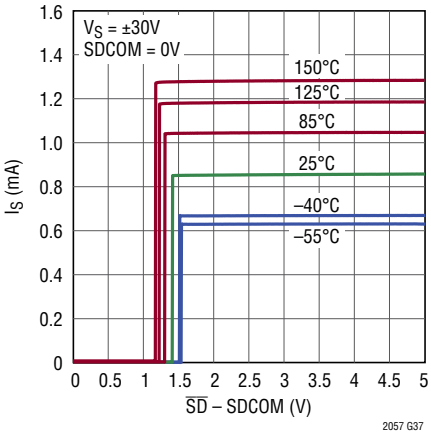
Shutdown Supply Current vs Supply Voltage



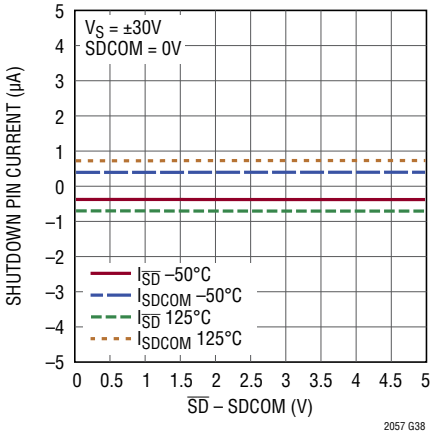
Supply Current vs Shutdown Control Voltage



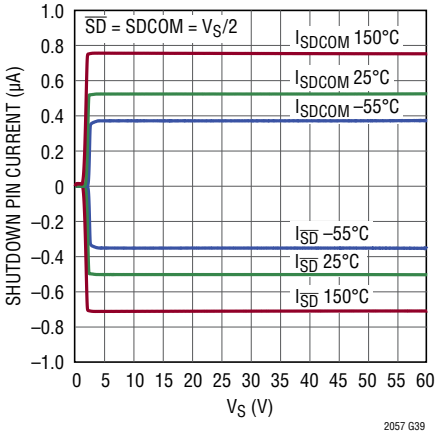
Supply Current vs Shutdown Control Voltage



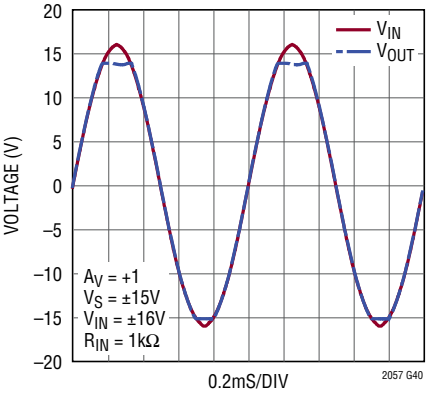
Shutdown Pin Current vs Shutdown Pin Voltage



Shutdown Pin Current vs Supply Voltage

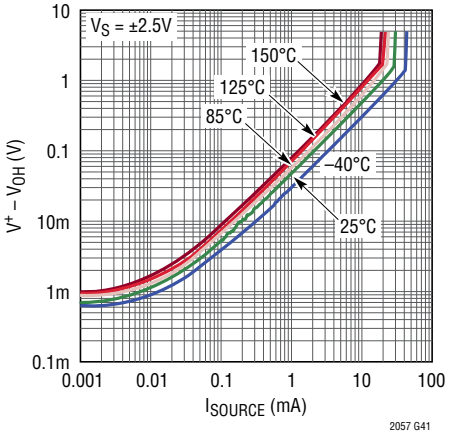


No Phase Reversal

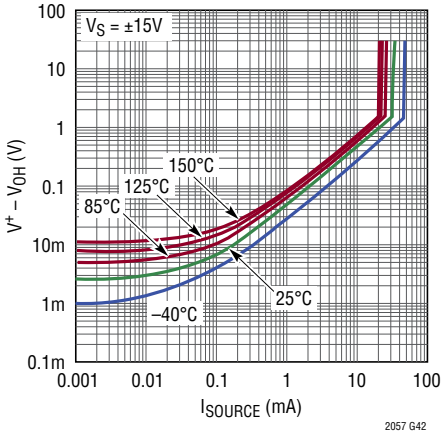


TYPICAL PERFORMANCE CHARACTERISTICS

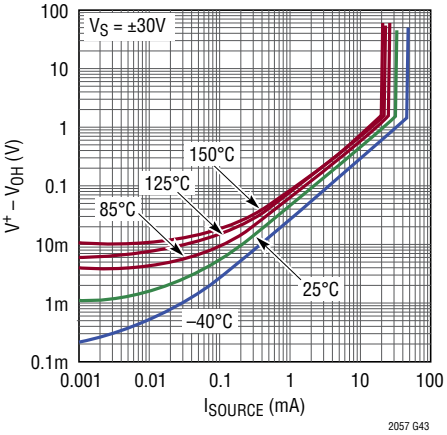
Output Voltage Swing High vs Load Current



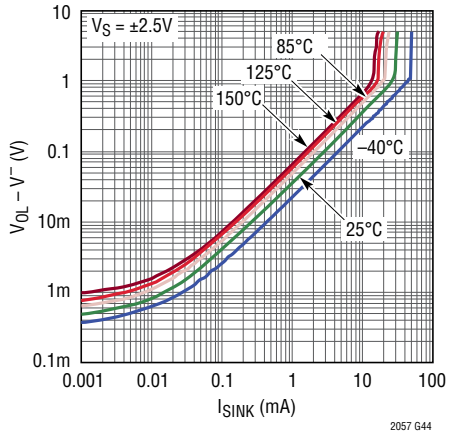
Output Voltage Swing High vs Load Current



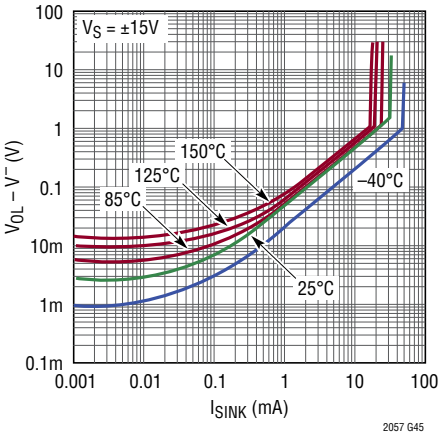
Output Voltage Swing High vs Load Current



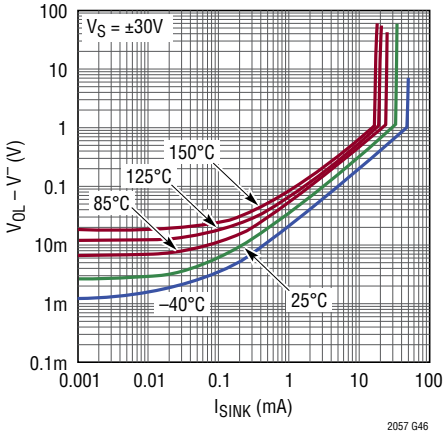
Output Voltage Swing Low vs Load Current



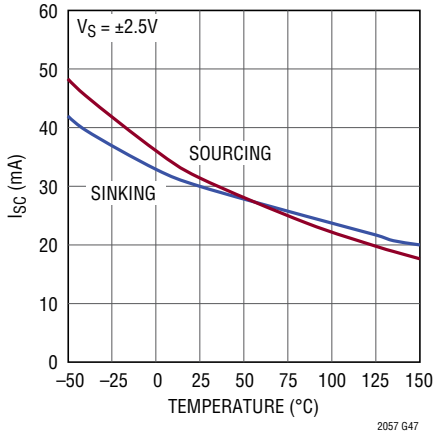
Output Voltage Swing Low vs Load Current



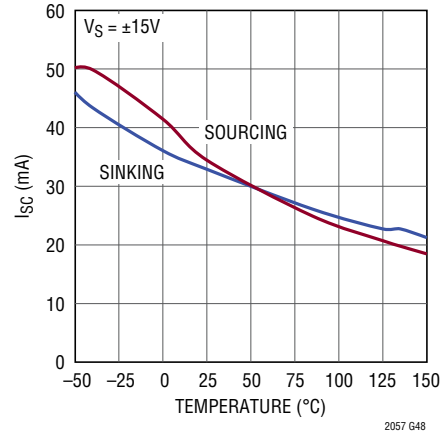
Output Voltage Swing Low vs Load Current



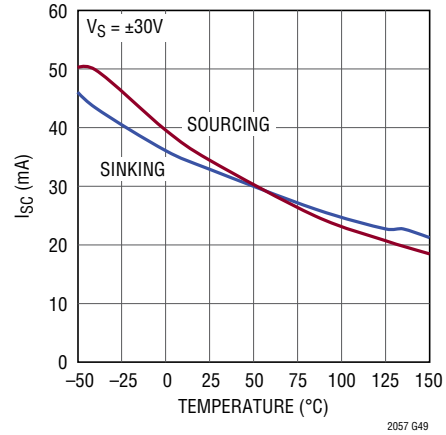
Short-Circuit Current vs Temperature



Short-Circuit Current vs Temperature

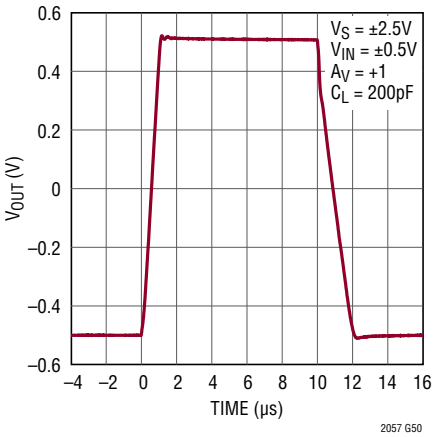


Short-Circuit Current vs Temperature

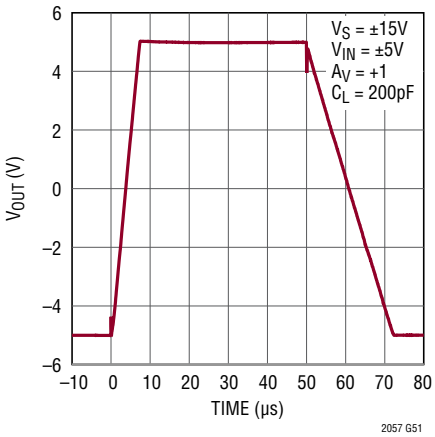


TYPICAL PERFORMANCE CHARACTERISTICS

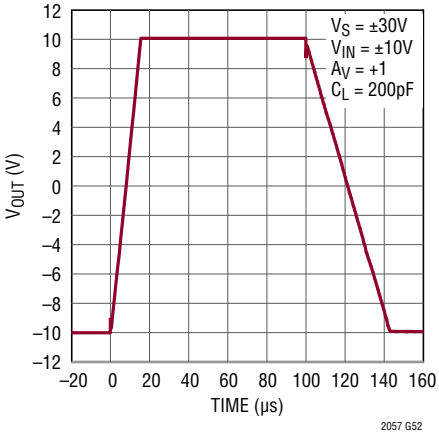
Large Signal Response



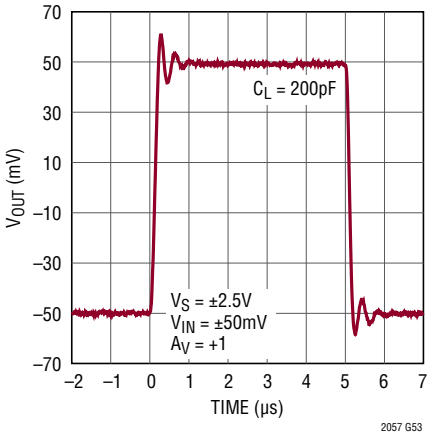
Large Signal Response



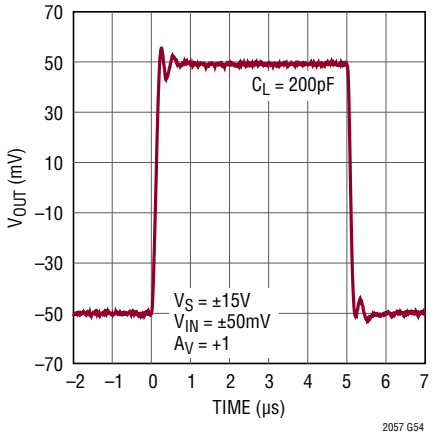
Large Signal Response



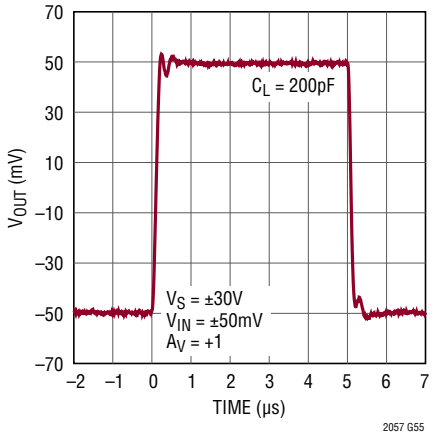
Small Signal Response



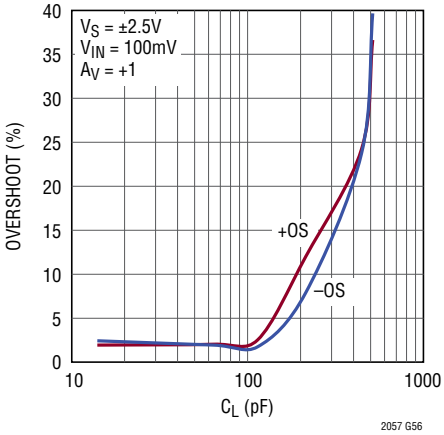
Small Signal Response



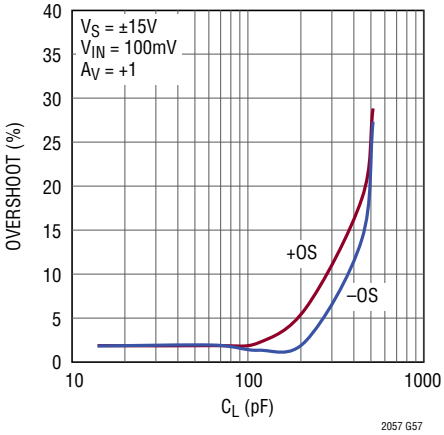
Small Signal Response



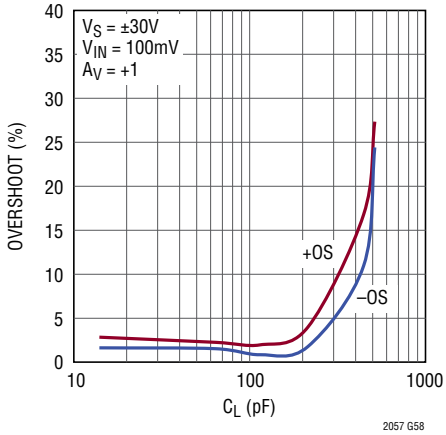
Small Signal Overshoot vs Load Capacitance



Small Signal Overshoot vs Load Capacitance

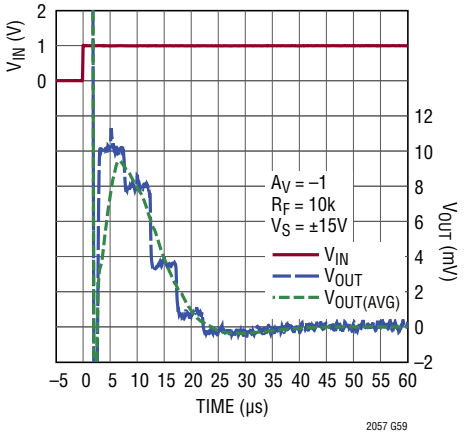


Small Signal Overshoot vs Load Capacitance

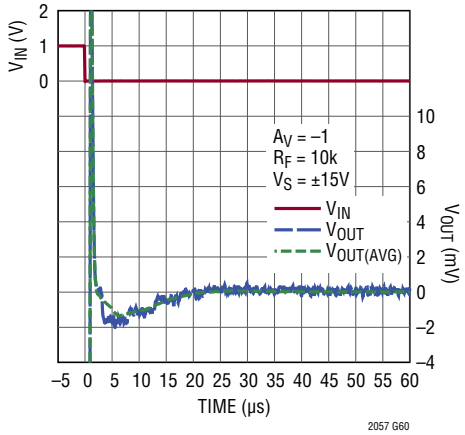


TYPICAL PERFORMANCE CHARACTERISTICS

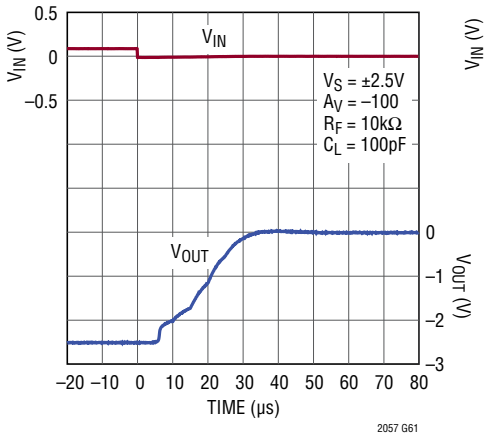
Large Signal Settling Transient



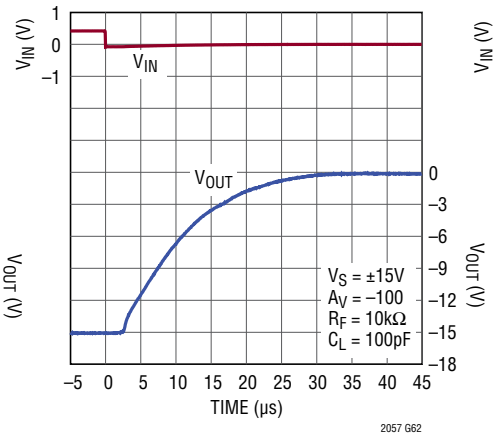
Large Signal Settling Transient



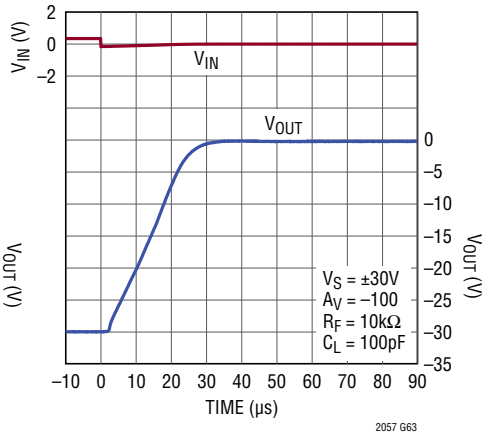
Output Overload Recovery



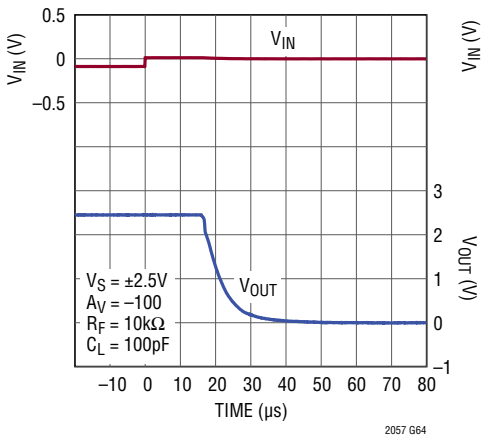
Output Overload Recovery



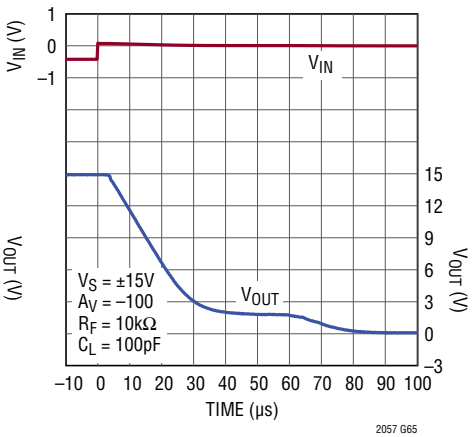
Output Overload Recovery



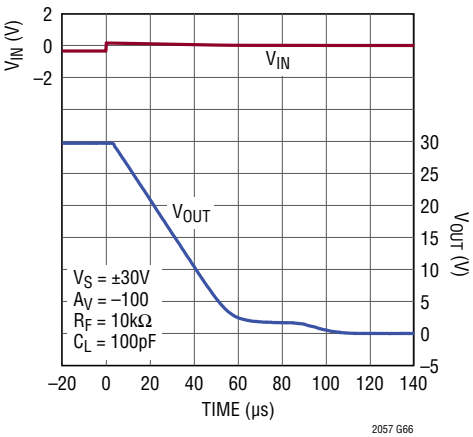
Output Overload Recovery



Output Overload Recovery



Output Overload Recovery



PIN FUNCTIONS

MS8 and S8/DD8

$\overline{SD}$ (Pin 1/Pin 1): Shutdown Control Pin.

–IN (Pin 2/Pin 2): Inverting Input.

+IN (Pin 3/Pin 3): Non-Inverting Input.

V^- (Pin 4/Pin 4, 9): Negative Power Supply.

SDCOM (Pin 8/Pin 8): Reference Voltage for $\overline{SD}$.

V^+ (Pin 7/Pin 7): Positive Power Supply.

OUT (Pin 6/Pin 6): Amplifier Output

NC (Pin 5/Pin 5): No Internal Connection.

MS10

GRD (Pin 1): Guard Ring. No Internal Connection.

–IN (Pin 2): Inverting Input.

+IN (Pin 3): Non-Inverting Input.

GRD (Pin 4): Guard Ring. No Internal Connection.

V^- (Pin 5): Negative Power Supply.

$\overline{SD}$ (Pin 10): Shutdown Control Pin.

SDCOM (Pin 9): Reference Voltage for $\overline{SD}$.

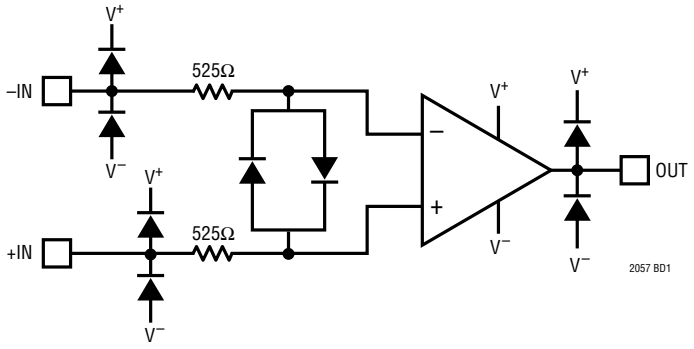
V^+ (Pin 8): Positive Power Supply.

NC (Pin 7): No Internal Connection.

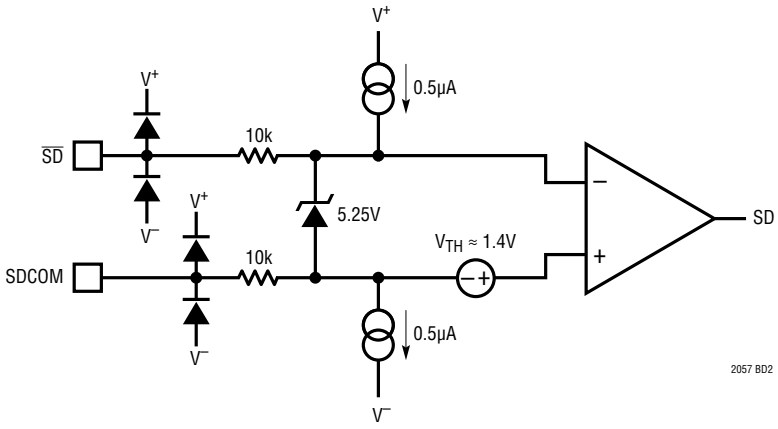
OUT (Pin 6): Amplifier Output.

BLOCK DIAGRAMS

Amplifier



Shutdown Circuit



APPLICATIONS INFORMATION

Input Voltage Noise

Chopper stabilized amplifiers like the LTC2057 achieve low offset and 1/f noise by heterodyning DC and flicker noise to higher frequencies. In a classical chopper stabilized amplifier, this process results in idle tones at the chopping frequency and its odd harmonics.

The LTC2057 utilizes circuitry to suppress these spurious artifacts to well below the offset voltage. The typical ripple magnitude at 100kHz is much less than $1\mu V_{RMS}$.

The voltage noise spectrum of the LTC2057 is shown in Figure 1. If lower noise is required, consider one of the following circuits from the Typical Applications section: "DC Stabilized, Ultralow Noise Amplifier" or "Paralleling Choppers to Improve Noise."

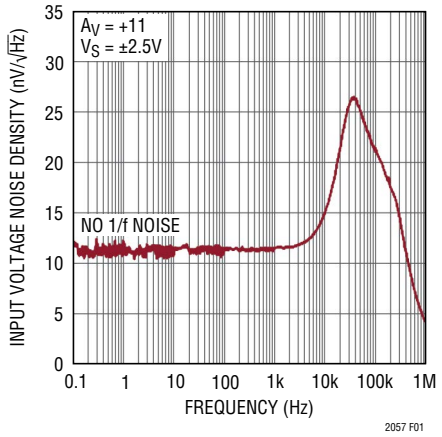


Figure 1. Input Voltage Noise Spectrum

Input Current Noise

For applications with high source impedances, input current noise can be a significant contributor to total output noise. For this reason, it is important to consider noise current interaction with circuit elements placed at an amplifier's inputs.

The current noise spectrum of the LTC2057 is shown in Figure 2. The characteristic curve shows no 1/f behavior. As with all zero-drift amplifiers, there is a significant current noise component at the offset-nulling frequency. This phenomenon is discussed in the Input Bias Current section.

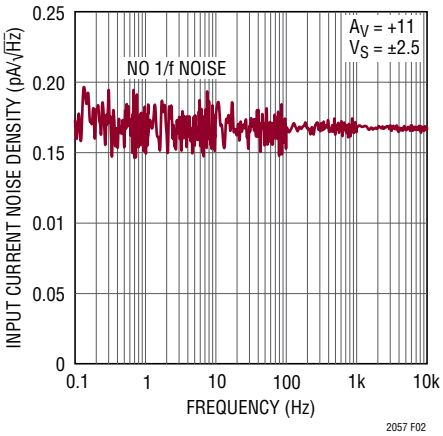


Figure 2. Input Current Noise Spectrum

It is important to note that the current noise is not equal to $2_q I_B$. This formula is relevant for base current in bipolar transistors and diode currents, but for most chopper and auto-zero amplifiers with switched inputs, the dominant current noise mechanism is not shot noise.

Input Bias Current

As illustrated in Figure 3, the LTC2057's input bias current originates from two distinct mechanisms. Below 75°C, input bias current is nearly constant with temperature, and is caused by charge injection from the clocked input switches used in offset correction.

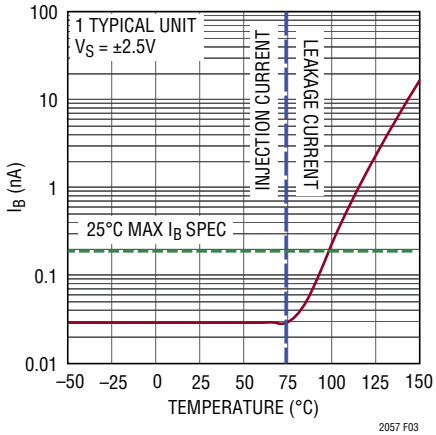


Figure 3. Input Bias Current vs Temperature

APPLICATIONS INFORMATION

The DC average of injection current is the specified input bias current, but this current has a frequency component at the chopping frequency as well. When these small current pulses, typically about $0.7nA_{RMS}$, interact with source impedances or gain setting resistors, the resulting voltage spikes are amplified by the closed loop gain. For high impedances, this may cause the 100kHz chopping frequency to be visible in the output spectrum, which is a phenomenon known as clock feed-through.

For zero-drift amplifiers, clock feed-through will be proportional to source impedance and the magnitude of injection current, a measure of which is I_B at 25°C. In order to minimize clock feed-through, keep gain-setting resistors and source impedances as low as possible. If high impedances are required, place a capacitor across the feedback resistor to limit the bandwidth of the closed loop gain. Doing so will effectively filter out the clock feed-through signal.

Injection currents from the two inputs are of equal magnitude but opposite direction. Therefore, input bias current effects due to injection currents will not be canceled by placing matched impedances at both inputs.

Above 75°C, leakage of the ESD protection diodes begins to dominate the input bias current and continues to increase exponentially at elevated temperatures. Unlike injection current, leakage currents are in the same direction for both inputs. Therefore, the output error due to leakage currents can be mitigated by matching the source impedances seen by the two inputs.

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which is over 13 times the maximum drift specification of the LTC2057. Figures 4 and 5 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

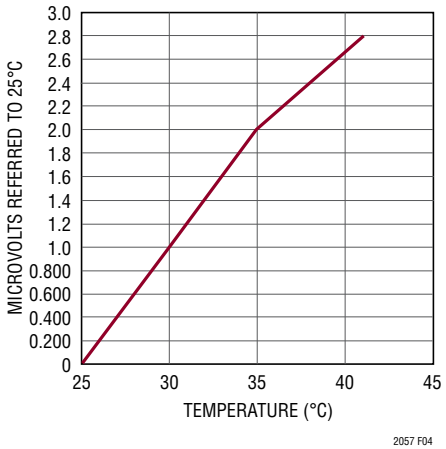


Figure 4. Thermal EMF Generated by Two Copper Wires From Different Manufacturers

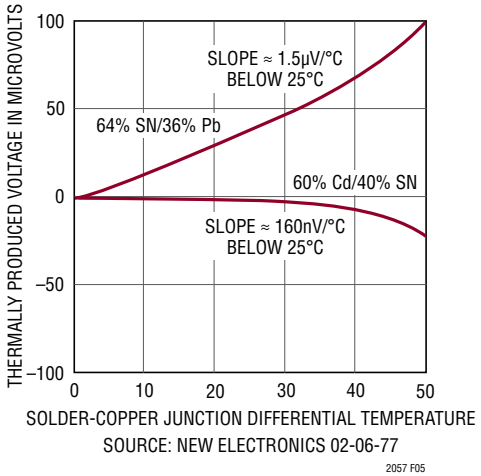
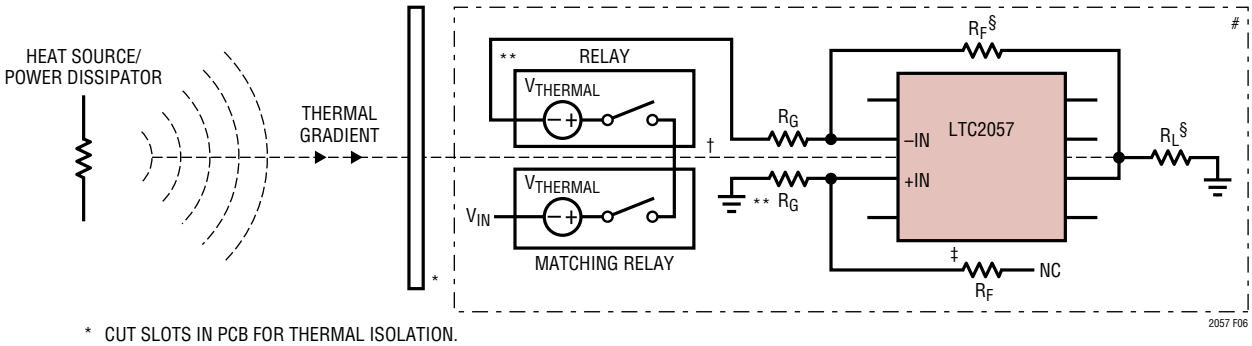


Figure 5. Solder-Copper Thermal EMFs

APPLICATIONS INFORMATION



* CUT SLOTS IN PCB FOR THERMAL ISOLATION.
** INTRODUCE DUMMY JUNCTIONS AND COMPONENTS TO OFFSET UNAVOIDABLE JUNCTIONS OR CANCEL THERMAL EMFs.
† ALIGN INPUTS SYMMETRICALLY WITH RESPECT TO THERMAL GRADIENTS.
‡ INTRODUCE DUMMY TRACES AND COMPONENTS FOR SYMMETRICAL THERMAL HEAT SINKING.
§ LOADS AND FEEDBACK CAN DISSIPATE POWER AND GENERATE THERMAL GRADIENTS. BE AWARE OF THEIR THERMAL EFFECTS.
# COVER CIRCUIT TO PREVENT AIR CURRENTS FROM CREATING THERMAL GRADIENTS.

Figure 6. Techniques for Minimizing Thermocouple-Induced Errors

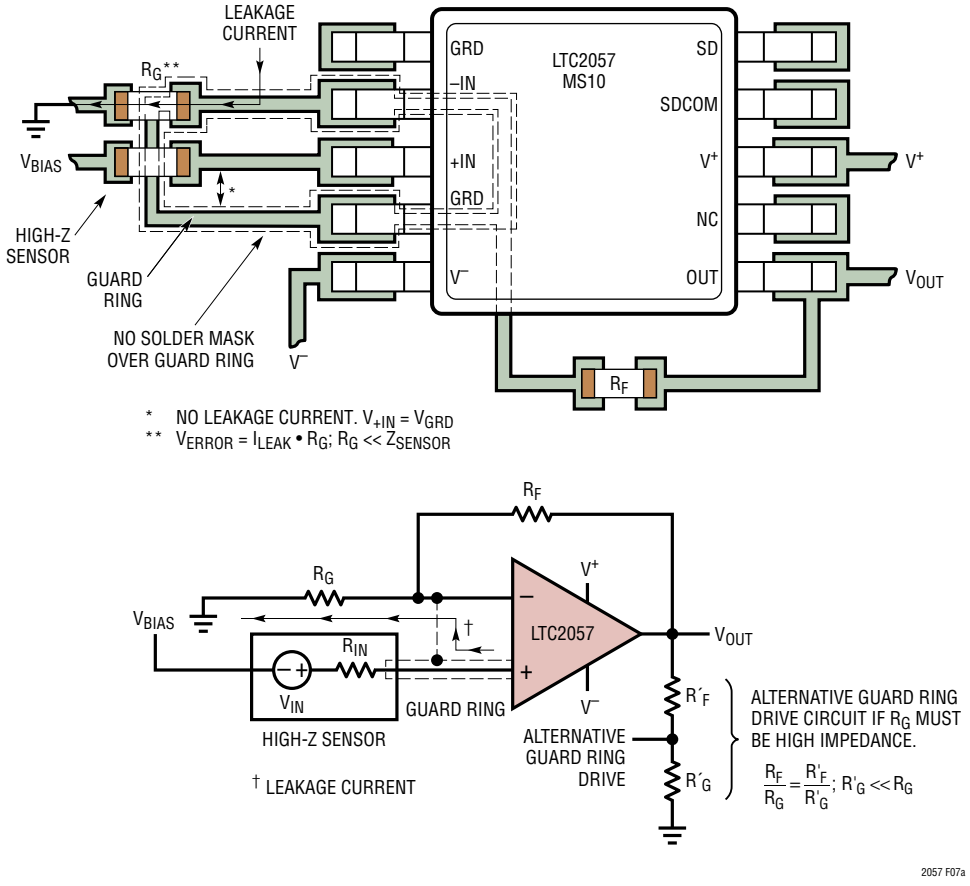


Figure 7a. Example Layout of Non-Inverting Amplifier with Leakage Guard Ring

APPLICATIONS INFORMATION

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially.

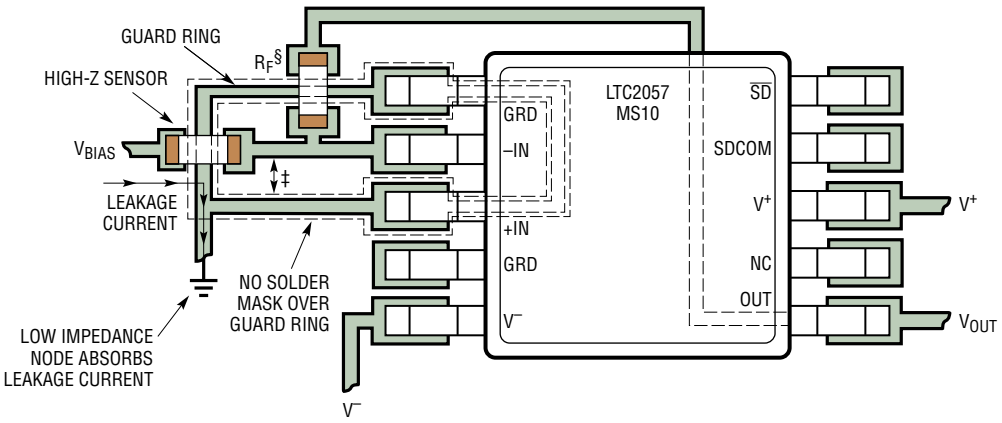
A summary of techniques can be found in Figure 6.

Leakage Effects

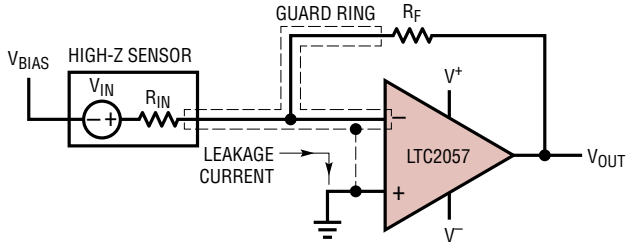
Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of sub-nanoamp signals. High voltage and high temperature applications are especially susceptible to these issues. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential very close to that of the inputs. The ring must be tied to a low impedance node. For inverting configurations, the guard ring should be tied to the potential of the positive input (+IN). For non-inverting configurations, the guard ring should be tied to the potential of the negative input (–IN). In order for this technique to be effective, the guard ring must not be covered by solder mask. Ringing both sides of the printed circuit board may be required. See Figures 7a and 7b for examples of proper layout.

For low-leakage applications, the LTC2057 is available in an MS10 package with a special pinout that facilitates the layout of guard ring structures. The pins adjacent to the inputs have no internal connection, allowing a guard ring to be routed through them.



‡ NO LEAKAGE CURRENT. $V_{–IN} = V_{GRD}$
§ AVOID DISSIPATING SIGNIFICANT AMOUNTS OF POWER IN THIS RESISTOR. IT WILL GENERATE THERMAL GRADIENTS WITH RESPECT TO THE INPUT PINS AND LEAD TO THERMOCOUPLE-INDUCED ERROR. THERMALLY ISOLATE OR ALIGN WITH INPUTS IF RESISTOR WILL CAUSE HEATING.



LEAKAGE CURRENT IS ABSORBED BY GROUND INSTEAD OF CAUSING A MEASUREMENT ERROR.

2057 F07b

Figure 7b. Example Layout of Inverting Amplifier with Leakage Guard Ring

APPLICATIONS INFORMATION

Power Dissipation

Since the LTC2057/LTC2057HV is capable of operating at >30V total supply, care should be taken with respect to power dissipation in the amplifier. When driving heavy loads at high voltages, use the θ_{JA} of the package to estimate the resulting die-temperature rise and take measures to ensure that the resulting junction temperature does not exceed specified limits. PCB metallization and heat sinking should also be considered when high power dissipation is expected. Thermal information for all packages can be found in the Pin Configuration section.

Electrical Overstress

Absolute Maximum Ratings should not be exceeded. Avoid driving the input and output pins beyond the rails, especially at supply voltages approaching 60V. If these fault conditions cannot be prevented, a series resistor at the pin of interest should help to limit the input current and reduce the possibility of device damage. This technique is shown in Figure 8.

Keep the value of the current limiting resistance as low as possible to avoid adding noise and error voltages from interaction with input bias currents but high enough to protect the device. Resistances up to 2k will not seriously impact noise or precision.

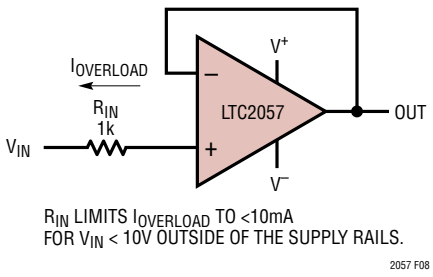


Figure 8. Using a Resistor to Limit Input Current

Shutdown Mode

The LTC2057/LTC2057HV features a shutdown mode for low-power applications. In the OFF state, the amplifier draws less than 11µA of supply current under all normal operating conditions, and the output presents a high-impedance to external circuitry.

Shutdown control is accomplished through differential signaling. This method allows for low voltage digital control logic to operate independently of the amplifier's high voltage supply rails.

Shutdown operation is accomplished by tying SDCOM to logic ground and $\overline{SD}$ to a 3V or 5V logic signal. A summary of control logic and operating ranges is shown in Tables 1 and 2.

Table 1. Shutdown Control Logic

SHUTDOWN PIN CONDITION	AMPLIFIER STATE
$\overline{SD}$ = Float, SDCOM = Float	ON
$\overline{SD}$ – SDCOM > 2V	ON
$\overline{SD}$ – SDCOM < 0.8V	OFF

Table 2. Operating Voltage Range for Shutdown Pins

	MIN	MAX
$\overline{SD}$ – SDCOM	–0.2V	5.2V
SDCOM	V^-	V^+ –2V
$\overline{SD}$	V^-	V^+

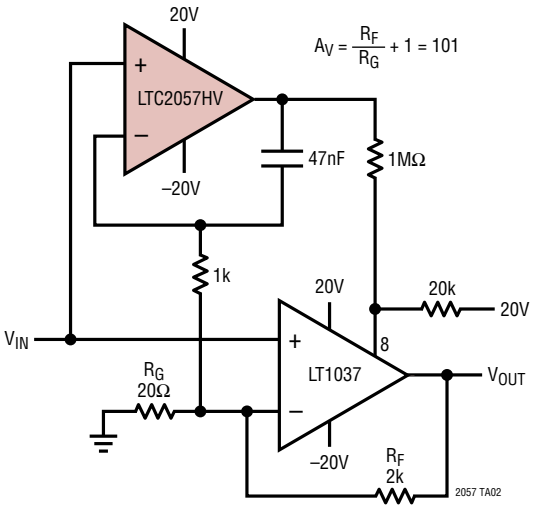
If the shutdown feature is not required, $\overline{SD}$ and SDCOM may be left floating. Internal circuitry will automatically keep the amplifier in the ON state.

For operation in noisy environments, a capacitor between $\overline{SD}$ and SDCOM is recommended to prevent noise from changing the shutdown state.

When there is a danger of $\overline{SD}$ and SDCOM being pulled beyond the supply rails, resistance in series with the shutdown pins is recommended to limit the resulting current.

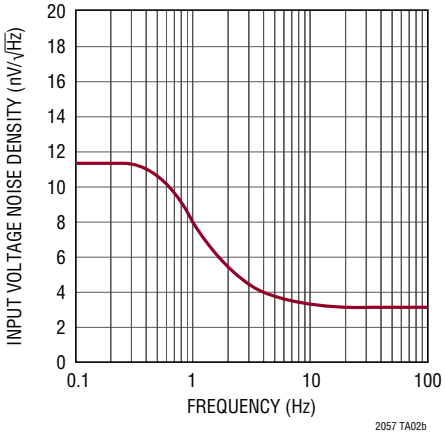
TYPICAL APPLICATIONS

DC Stabilized, Ultralow Noise Composite Amplifier

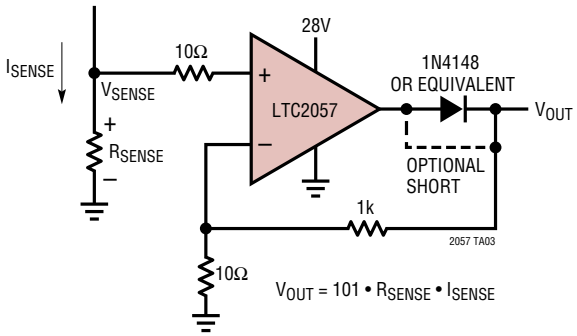


COMPOSITE AMPLIFIER COMBINES THE EXCELLENT BROADBAND NOISE PERFORMANCE OF THE LT1037 WITH THE ZERO-DRIFT PROPERTIES OF THE LTC2057. THE RESULTING CIRCUIT HAS MICROVOLT ACCURACY, SUPPRESSED 1/f NOISE, AND LOW BROADBAND NOISE.

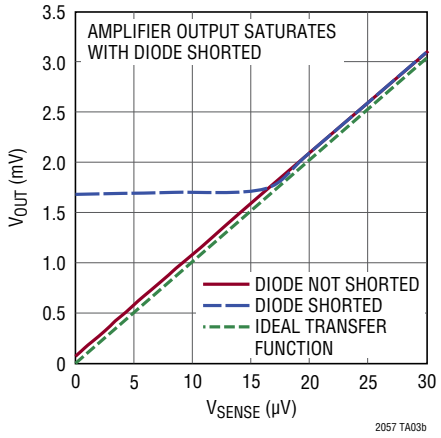
Input Voltage Noise Spectrum of Composite Amplifier



Low-Side Current Sense Amplifier

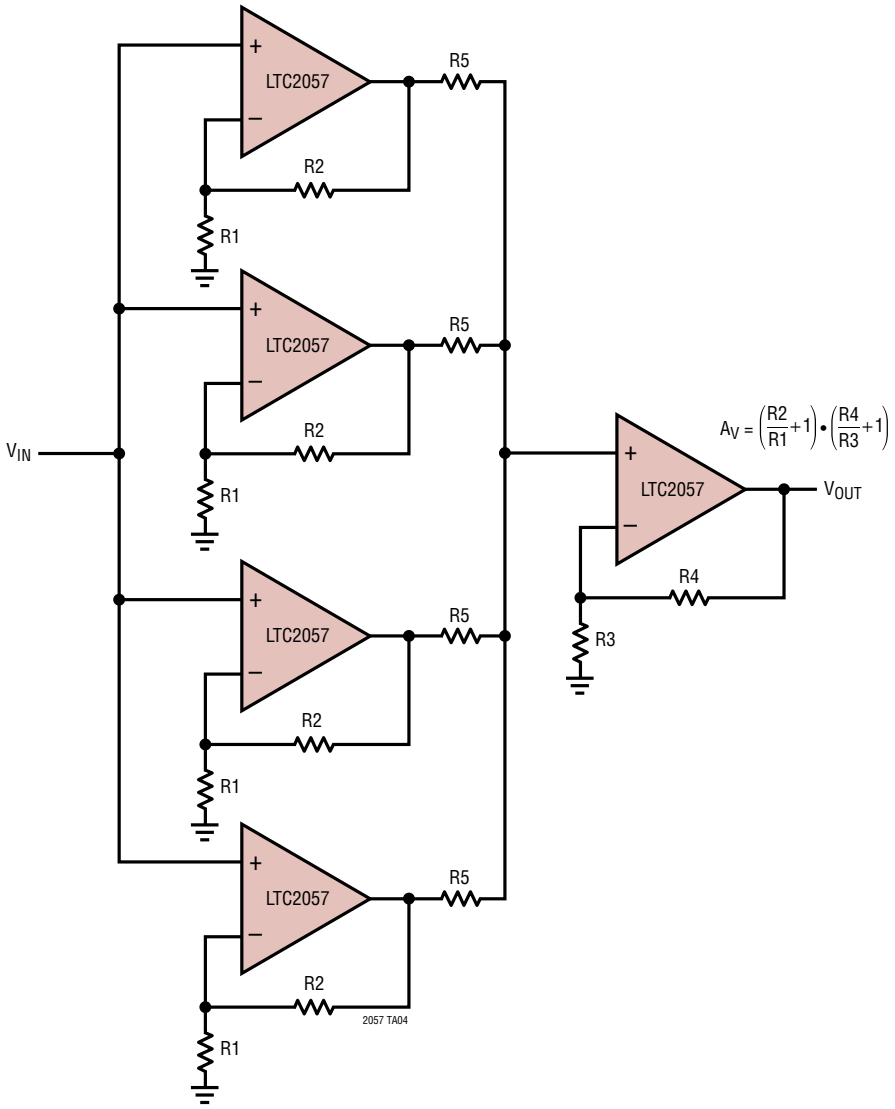


Low-Side Current Sense Amplifier Transfer Function



TYPICAL APPLICATIONS

Paralleling Choppers to Improve Noise



DC TO 10Hz NOISE = $\frac{200nV_{P-P}}{\sqrt{N}}$, $e_n = \frac{11nV/\sqrt{Hz}}{\sqrt{N}}$, $i_n = \sqrt{N} \bullet 170fA/\sqrt{Hz}$, $I_B < N \bullet 200pA$ (MAX)

WHERE N IS THE NUMBER OF PARALLELED INPUT AMPLIFIERS.

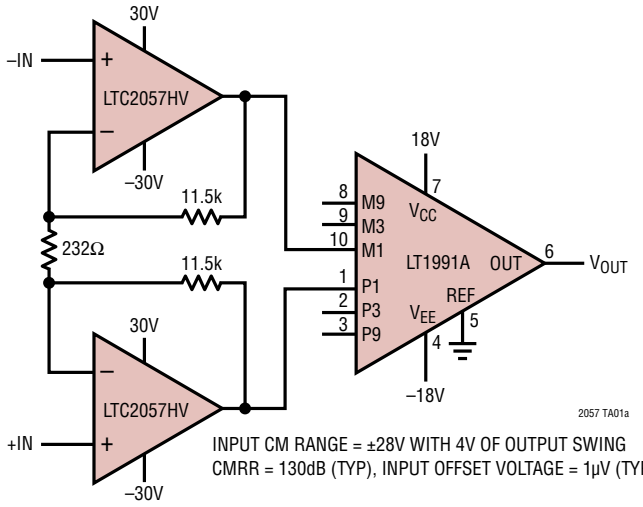
FOR N = 4, DC TO 10Hz NOISE = $100nV_{P-P}$, $e_n = 5.5nV/\sqrt{Hz}$, $i_n = 340fA/\sqrt{Hz}$, $I_B < 800pA$ (MAX).

R_5 SHOULD BE A FEW HUNDRED OHMS TO ISOLATE AMPLIFIER OUTPUTS WITHOUT CONTRIBUTING SIGNIFICANTLY TO NOISE OR I_B-INDUCED ERROR.

$\left(\frac{R2}{R1}+1\right) >> \sqrt{N}$ FOR OUTPUT AMPLIFIER NOISE TO BE INSIGNIFICANT.

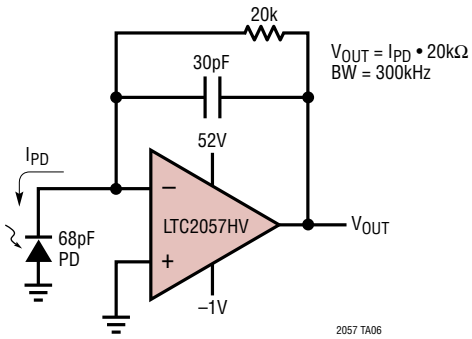
TYPICAL APPLICATIONS

Wide Input Range Precision Gain-of-100 Instrumentation Amplifier



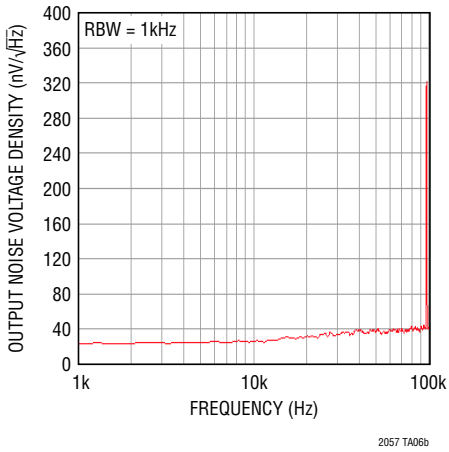
INPUT CM RANGE = ±28V WITH 4V OF OUTPUT SWING
CMRR = 130dB (TYP), INPUT OFFSET VOLTAGE = 1µV (TYP)

Ultra-Precision, 135dB Dynamic Range Photodiode Amplifier



OUTPUT RANGE 9µV TO 50V, LIMIT BW TO 1kHz
TO KEEP OUTPUT NOISE BELOW $5\mu V_{P-P}$

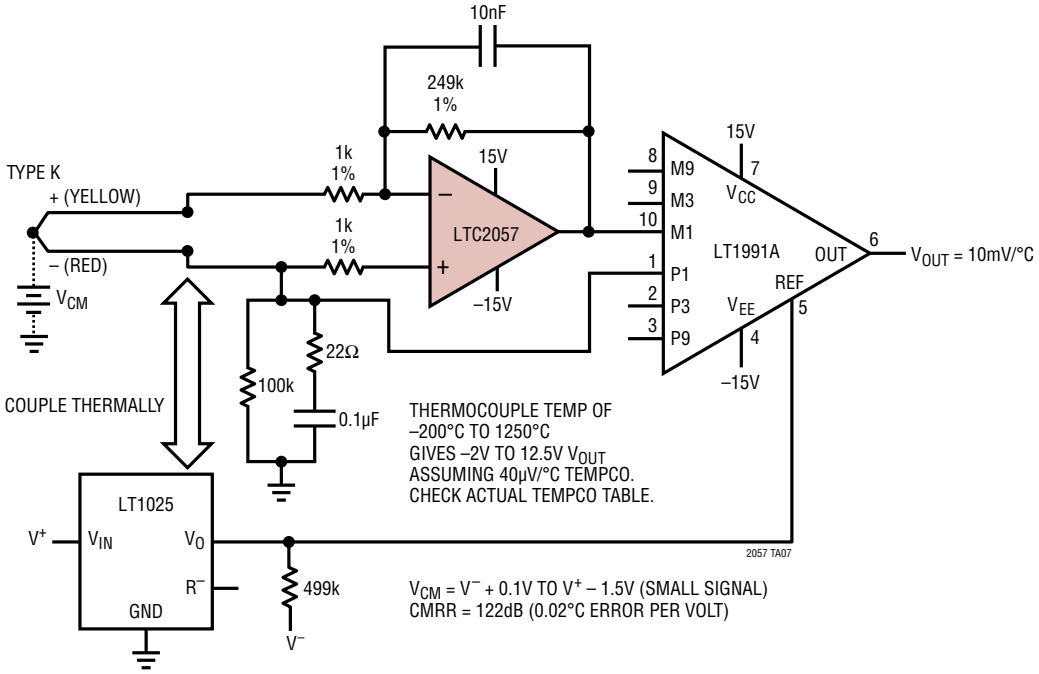
Output Noise Spectrum of Photodiode Amplifier



NOISE FLOOR IS ONLY SLIGHTLY ABOVE THE 20kΩ RESISTOR`S 18nV/√Hz.
CLOCK FEEDTHROUGH IS VISIBLE NEAR 100kHz WITH AMPLITUDE OF
$10\mu V_{RMS}$ OUTPUT REFERRED OR $0.5nA_{RMS}$ INPUT REFERRED.

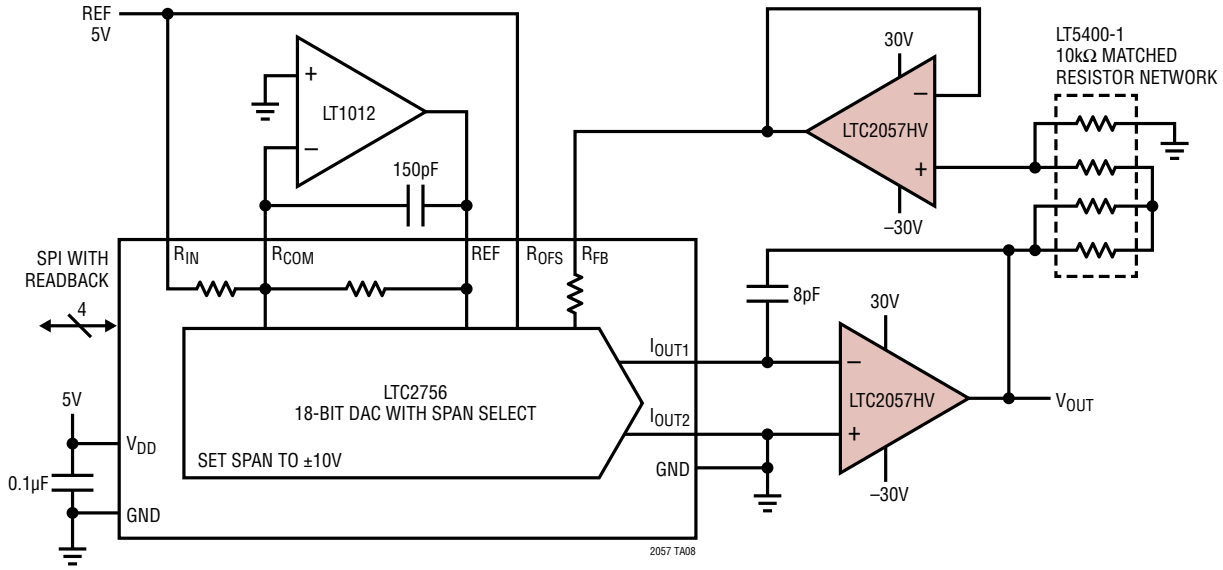
TYPICAL APPLICATIONS

Differential Thermocouple Amplifier

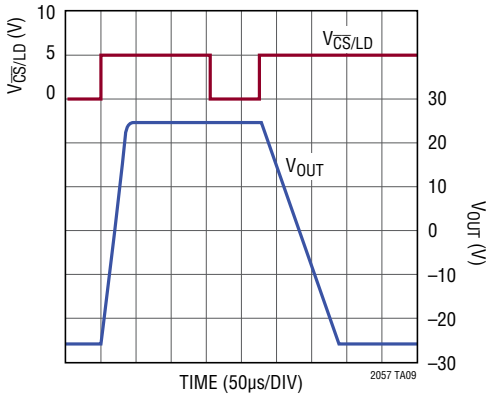


TYPICAL APPLICATIONS

18-Bit DAC with ±25V Output Swing



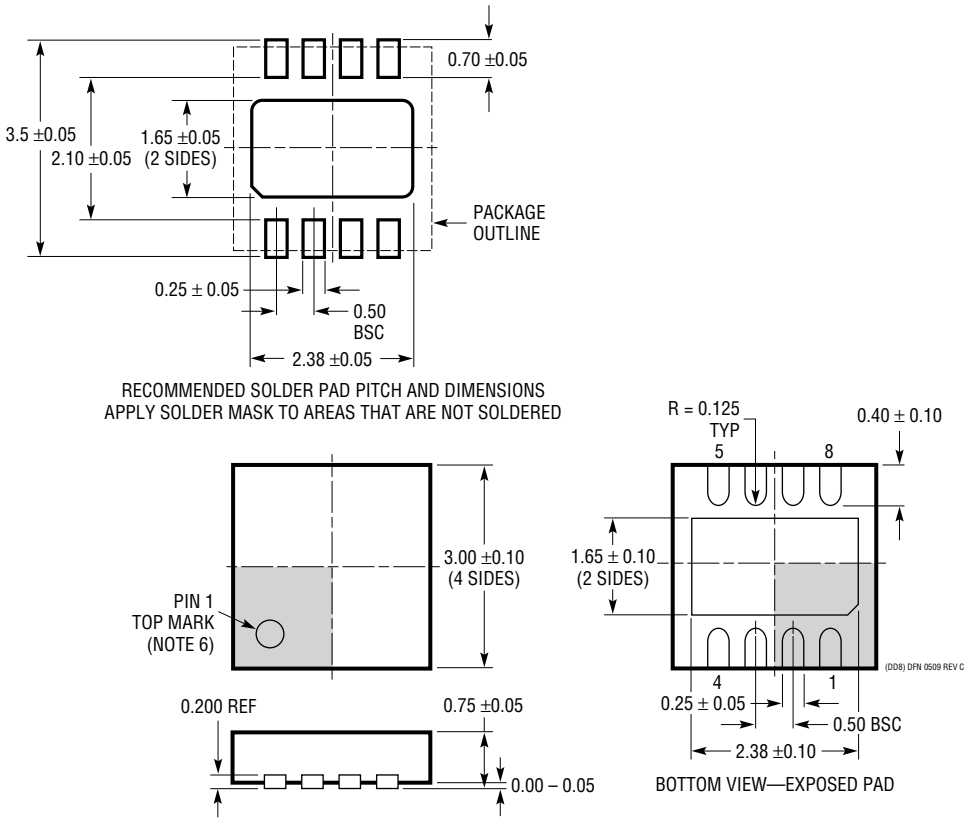
Time Domain Response



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD8 Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

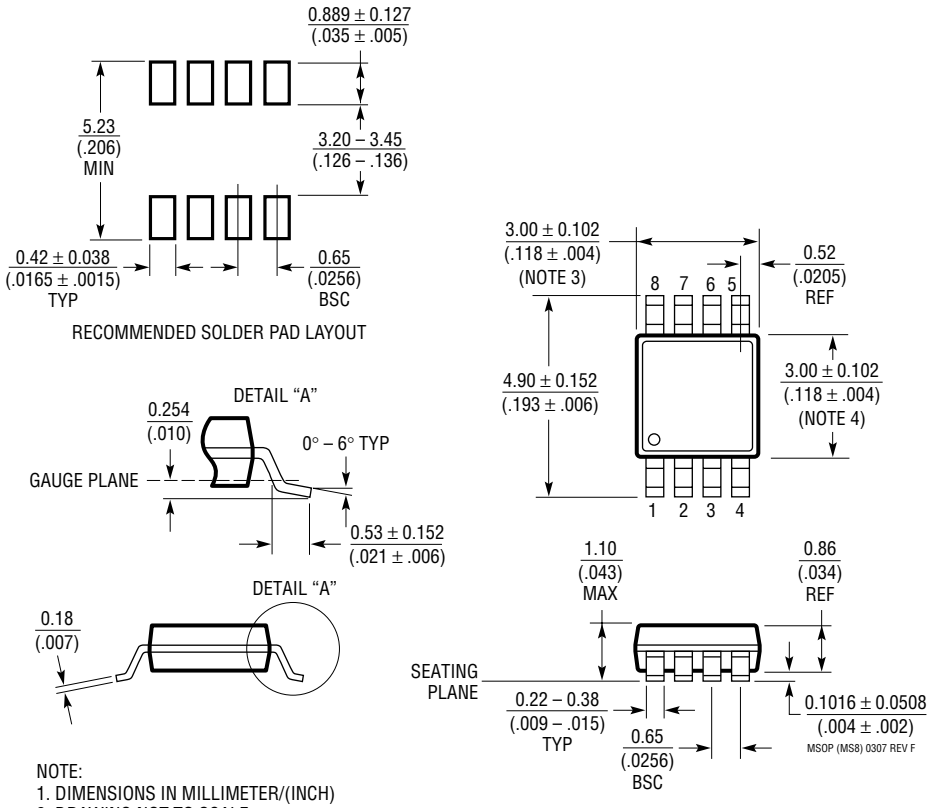


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

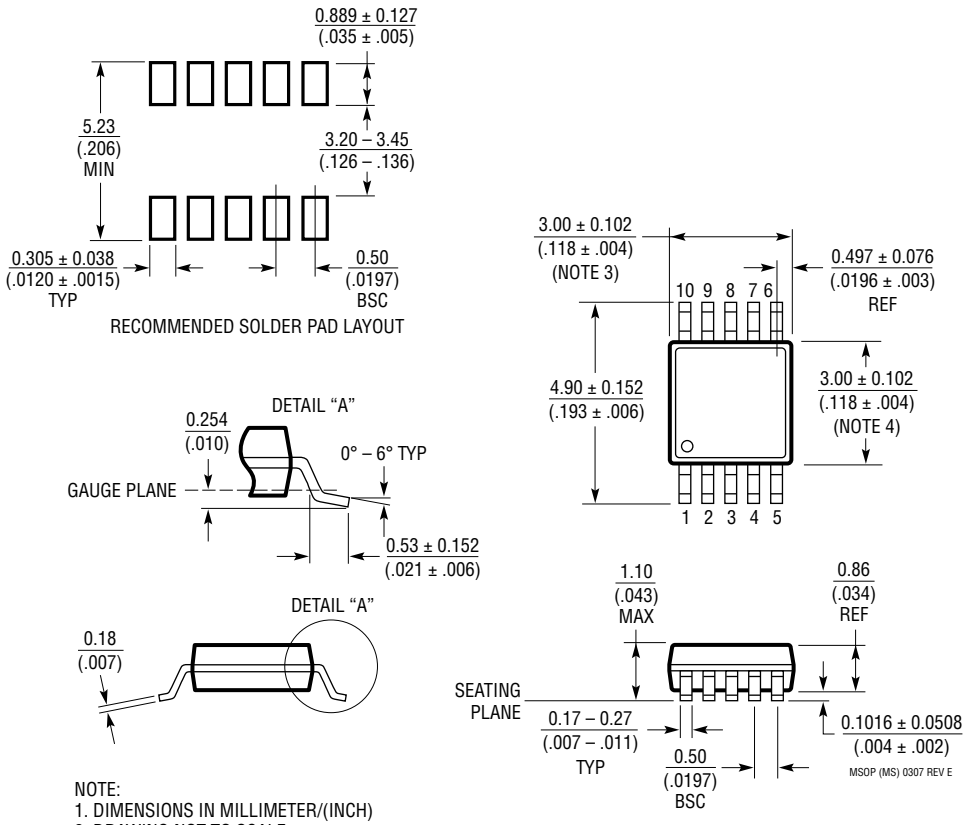


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)

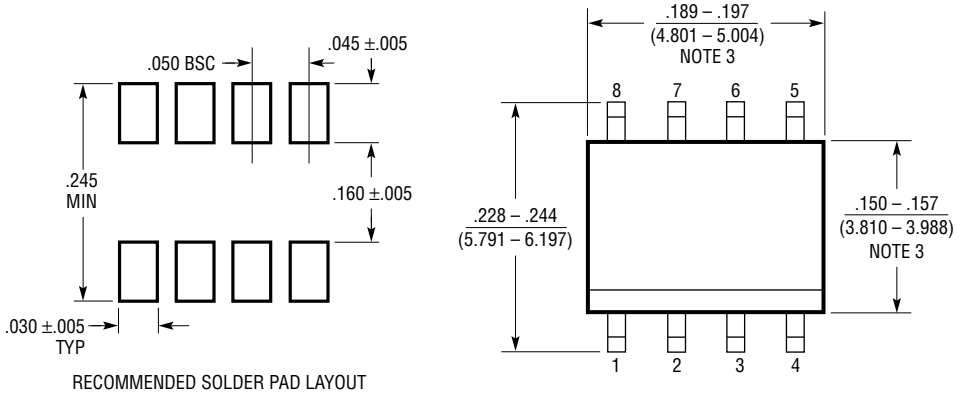


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



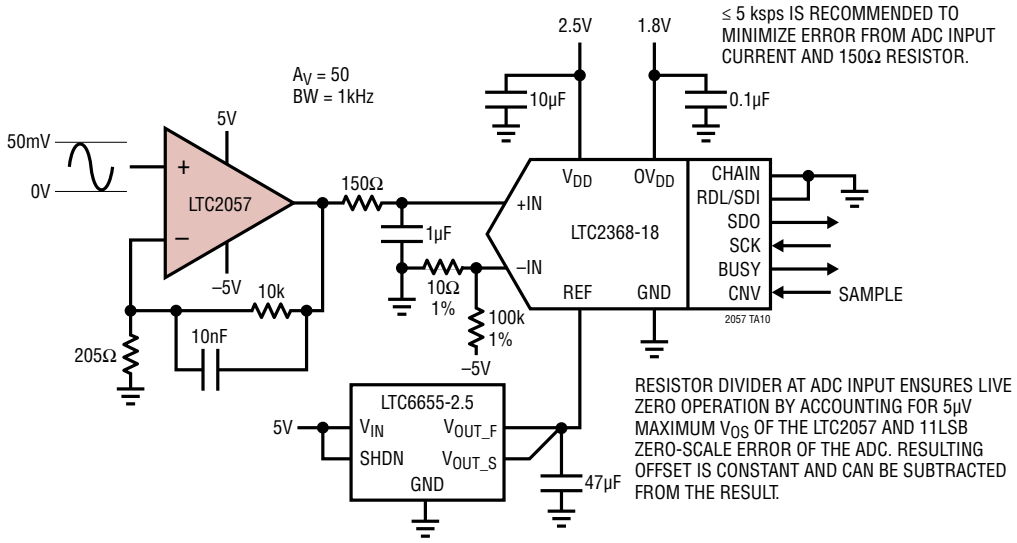
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Microvolt Precision 18-Bit ADC Driver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2050HV	Zero-Drift Operational Amplifier	3µV V_{OS}, 2.7V to 12V V_S, 1.5mA I_S, RR Output
LTC2051HV/ LTC2052HV	Dual/Quad, Zero-Drift Operational Amplifier	3µV V_{OS}, 2.7V to 12V V_S, 1.5mA I_S, RR Output
LTC2053	Precision, Rail-to-Rail, Zero-Drift, Resistor-Programmable Instrumentation Amplifier	10µV V_{OS}, 2.7V to 11V V_S, 1.3mA I_S, RRIO
LTC2054HV/ LTC2055HV	Micropower, Single/Dual, Zero-Drift Operational Amplifier	5µV V_{OS}, 2.7V to 12V V_S, 0.2mA I_S, RRIO
LTC6652	Precision, Low Drift, Low Noise, Buffered Reference	5ppm/°C, 0.05% Initial Accuracy, 2.1ppm$_{P-P}$ Noise
LT6654	Precision, Wide Supply, High Output Drive, Low Noise Reference	10ppm/°C, 0.05% Initial Accuracy, 1.6ppm$_{P-P}$ Noise
LTC6655	0.25ppm Noise, Low Drift, Precision, Buffered Reference Family	2ppm/°C, 0.025% Initial Accuracy, 0.25ppm$_{P-P}$ Noise
LT6016/LT6017	Dual/Quad, 76V Over-The-Top® Input Operational Amplifier	50µV V_{OS}, 3V to 50V V_S, 0.335mA I_S, RRIO
LTC6090	140V Operational Amplifier	50pA I_B, 1.6mV V_{OS}, 9.5V to 140V V_S, 4.5mA I_S, RR Output
LT5400	Quad Matched Resistor Network	±0.01%, ±0.2ppm/°C Matching

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