Dual 12-/10-/8-Bit I²C V_{OUT} DACs with 10ppm/°C Reference

FEATURES

- **Integrated Precision Reference**
  2.5V Full-Scale 10ppm/°C (LTC2633-L)
  4.096V Full-Scale 10ppm/°C (LTC2633-H)
- **Maximum INL Error: ±1LSB (LTC2633A-12)**
- Low Noise: 0.75mV$_{P-P}$ 0.1Hz to 200kHz
- Guaranteed Monotonic Over –40°C to 125°C Temperature Range
- Selectable Internal or External Reference
- 2.7V to 5.5V Supply Range (LTC2633-L)
- Low Power: 0.4mA at 3V
- Power-on-Reset to Zero-Scale/Mid-Scale/Hi-Z
- Double-Buffered Data Latches
- 8-Lead ThinSOT™ Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Power Supply Margining
- Portable Equipment
- Automotive

DESCRIPTION

The LTC®2633 is a family of dual 12-, 10-, and 8-bit voltage-output DACs with an integrated, high accuracy, low drift reference in an 8-lead TSOT-23 package. It has rail-to-rail output buffers and is guaranteed monotonic. The LTC2633-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2633-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. Each DAC can also operate with an external reference, which sets the full-scale output to the external reference voltage.

These DACs communicate via a 2-wire I²C-compatible serial interface. The LTC2633 operates in both the standard mode (clock rate of 100kHz) and the fast mode (clock rate of 400kHz). The LTC2633 incorporates a power-on reset circuit. Options are available for reset to zero-scale, reset to mid-scale in internal reference mode, reset to mid-scale in external reference mode, or reset with all DAC outputs in a high impedance state after power-up.

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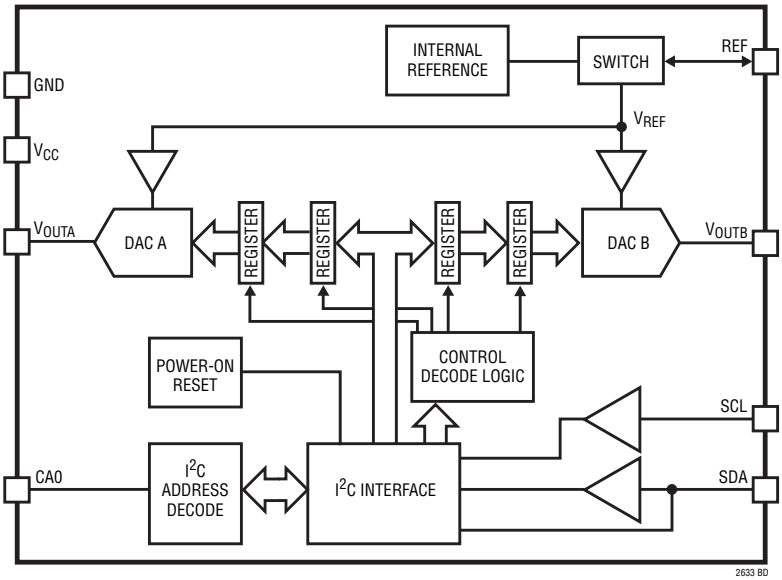
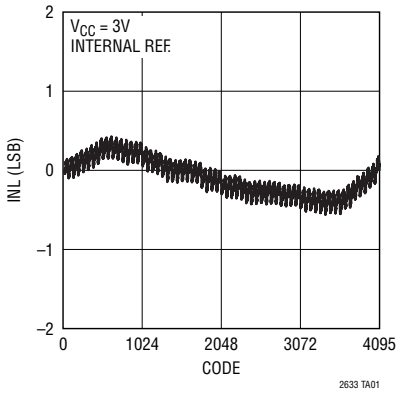
BLOCK DIAGRAM



Integral Nonlinearity (LTC2633A-LZ12) INL Curve

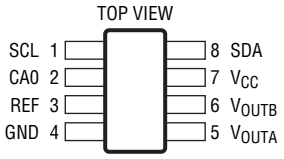


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
SCL, SDA ..... –0.3V to 6V
V_{OUTA}, V_{OUTB} ..... –0.3V to Min(V_{CC} + 0.3V, 6V)
CA0 ..... –0.3V to Min(V_{CC} + 0.3V, 6V)
REF ..... –0.3V to Min(V_{CC} + 0.3V, 6V)
Operating Temperature Range
  LTC2633C ..... 0°C to 70°C
  LTC2633H (Note 3) ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C (NOTE 6), θ_{JA} = 195°C/W

ORDER INFORMATION

LTC2633 A C TS8 –L Z 12 #TRM PBF

LEAD FREE DESIGNATOR

TAPE AND REEL
TR = 2,500-Piece Tape and Reel
TRM = 500-Piece Tape and Reel

RESOLUTION
12 = 12-Bit
10 = 10-Bit
8 = 8-Bit

POWER-ON RESET
I = Reset to Mid-Scale in Internal Reference Mode
X = Reset to Mid-Scale in External Reference Mode (2.5V Full-Scale Voltage, Internal Reference Mode Option Only)
O = Reset to Mid-Scale in Internal Reference Mode, DACs High Z (2.5V Full-Scale Voltage, Internal Reference Mode Option Only)
Z = Reset to Zero-Scale in Internal Reference Mode

FULL-SCALE VOLTAGE INTERNAL REFERENCE MODE
L = 2.5V
H = 4.096V

PACKAGE TYPE
TS8 = 8-Lead Plastic TSOT-23

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
H = Automotive Temperature Range (–40°C to 125°C)

ELECTRICAL GRADE (OPTIONAL)
A = ±1LSB Maximum INL (12-Bit)

PRODUCT PART NUMBER

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING**	VFS WITH INTERNAL REFERENCE	POWER-ON RESET TO CODE	POWER-ON REFERENCE MODE	RESOLUTION	V_{CC}	MAXIMUM INL
LTC2633A-LI12	LTFTC	2.5V • (4095/4096)	Mid-Scale	Internal	12-Bit	2.7V to 5.5V	±1LSB
LTC2633A-LX12	LTFTB	2.5V • (4095/4096)	Mid-Scale	External	12-Bit	2.7V to 5.5V	±1LSB
LTC2633A-LZ12	LTFSZ	2.5V • (4095/4096)	Zero-Scale	Internal	12-Bit	2.7V to 5.5V	±1LSB
LTC2633A-LO12*	LTFTV	2.5V • (4095/4096)	High Impedance	Internal	12-Bit	2.7V to 5.5V	±1LSB
LTC2633A-HI12	LTFTF	4.096V • (4095/4096)	Mid-Scale	Internal	12-Bit	4.5V to 5.5V	±1LSB
LTC2633A-HZ12	LTFTD	4.096V • (4095/4096)	Zero-Scale	Internal	12-Bit	4.5V to 5.5V	±1LSB
LTC2633-LI12	LTFTC	2.5V • (4095/4096)	Mid-Scale	Internal	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2633-LI10	LTFTJ	2.5V • (1023/1024)	Mid-Scale	Internal	10-Bit	2.7V to 5.5V	±1LSB
LTC2633-LI8	LTFTQ	2.5V • (255/256)	Mid-Scale	Internal	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2633-LX12	LTFTB	2.5V • (4095/4096)	Mid-Scale	External	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2633-LX10	LTFTH	2.5V • (1023/1024)	Mid-Scale	External	10-Bit	2.7V to 5.5V	±1LSB
LTC2633-LX8	LTFTP	2.5V • (255/256)	Mid-Scale	External	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2633-LZ12	LTFSZ	2.5V • (4095/4096)	Zero-Scale	Internal	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2633-LZ10	LTFTG	2.5V • (1023/1024)	Zero-Scale	Internal	10-Bit	2.7V to 5.5V	±1LSB
LTC2633-LZ8	LTFTN	2.5V • (255/256)	Zero-Scale	Internal	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2633-LO12*	LTFTV	2.5V • (4095/4096)	High Impedance	Internal	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2633-LO10*	LTFTW	2.5V • (1023/1024)	High Impedance	Internal	10-Bit	2.7V to 5.5V	±1LSB
LTC2633-LO8*	LTFTX	2.5V • (255/256)	High Impedance	Internal	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2633-HI12	LTFTF	4.096V • (4095/4096)	Mid-Scale	Internal	12-Bit	4.5V to 5.5V	±2.5LSB
LTC2633-HI10	LTFTM	4.096V • (1023/1024)	Mid-Scale	Internal	10-Bit	4.5V to 5.5V	±1LSB
LTC2633-HI8	LTFTS	4.096V • (255/256)	Mid-Scale	Internal	8-Bit	4.5V to 5.5V	±0.5LSB
LTC2633-HZ12	LTFTD	4.096V • (4095/4096)	Zero-Scale	Internal	12-Bit	4.5V to 5.5V	±2.5LSB
LTC2633-HZ10	LTFTK	4.096V • (1023/1024)	Zero-Scale	Internal	10-Bit	4.5V to 5.5V	±1LSB
LTC2633-HZ8	LTFTR	4.096V • (255/256)	Zero-Scale	Internal	8-Bit	4.5V to 5.5V	±0.5LSB

* Contact Linear Technology for other Hi-Z options.
**The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-LI12/-LI10/-LI8/-LX12/-LX10/-LX8/-LZ12/-LZ10/-LZ8/-LO12/-LO10/-LO8/LTC2633A-LI12/-LX12/-LZ12/-LO12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2633-8			LTC2633-10			LTC2633-12			LTC2633A-12			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 3V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero Scale Error	V_{CC} = 3V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 3V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 3V, Internal Ref.			±10			±10			±10			±10		μV/°C
GE	Gain Error	V_{CC} = 3V, Internal Ref.	●		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8	%FSR

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-LI12/-LI10/-LI8/-LX12/-LX10/-LX8/-LZ12/-LZ10/-LZ8/-LO12/-LO10/-LO8/LTC2633A-LI12/-LX12/-LZ12/-LO12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2633-8 MIN	LTC2633-8 TYP	LTC2633-8 MAX	LTC2633-10 MIN	LTC2633-10 TYP	LTC2633-10 MAX	LTC2633-12 MIN	LTC2633-12 TYP	LTC2633-12 MAX	LTC2633A-12 MIN	LTC2633A-12 TYP	LTC2633A-12 MAX	UNITS
GE_{TC}	Gain Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 10) C-Grade H-Grade			 10 10			 10 10			 10 10			 10 10		 ppm/°C ppm/°C
	Load Regulation	Internal Ref., Mid-Scale, V_{CC} = 3V ± 10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V ± 10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.009 0.009	 0.016 0.016		 0.035 0.035	 0.064 0.064		 0.14 0.14	 0.256 0.256		 0.14 0.14	 0.256 0.256	 LSB/mA LSB/mA
R_{OUT}	DC Output Impedance	Internal Ref., Mid-Scale, V_{CC} = 3V ± 10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V ± 10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156	 Ω Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 2.5		V V
PSR	Power Supply Rejection	V_{CC} = 3V ± 10% or 5V ± 10%			–80		dB
I_{SC}	Short Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero Scale; V_{OUT} shorted to V_{CC} Full Scale; V_{OUT} shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
DAC I_{SD}	DAC Output Current in High Impedance Mode	LO Options Only	●		0.01	±0.5	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 3V, V_{REF} = 2.5V, External Reference V_{CC} = 3V, Internal Reference V_{CC} = 5V V_{REF} = 2.5V, External Reference V_{CC} = 5V, Internal Reference	● ● ● ●		0.3 0.4 0.3 0.4	0.5 0.6 0.5 0.6	mA mA mA mA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V	●		0.5	2	µA
Reference Input							
	Input Voltage Range		●	1		V_{CC}	V
	Resistance		●	120	160	200	kΩ
	Capacitance				12		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.005	5	µA
Reference Output							
	Output Voltage		●	1.24	1.25	1.26	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short Circuit Current	V_{CC} = 5.5V, REF Shorted to GND			2.5		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-LI12/-LI10/-LI8/-LX12/-LX10/-LX8/-LZ12/-LZ10/-LZ8/-LO12/-LO10/-LO8/LTC2633A-LI12/-LX12/-LZ12/-LO12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)	(Note 14)	●	–0.5		0.3V_{CC}	V
V_{IH}	High Level Input Voltage (SDA and SCL)	(Note 11)	●	0.7V_{CC}			V
$V_{IL(CA0)}$	Low Level Input Voltage on CA0	See Test Circuit 1	●			0.15V_{CC}	V
$V_{IH(CA0)}$	High Level Input Voltage on CA0	See Test Circuit 1	●	0.85V_{CC}			V
R_{INH}	Resistance from CA0 to V_{CC} to Set CA0 = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA0 to GND to Set CA0 = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA0 to V_{CC} or GND to Set CA0 = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	$V_O = V_{IH(MIN)}$ to $V_O = V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 12)	●	20 + 0.1C_B		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			1	µA
C_{IN}	I/O Pin Capacitance	(Note 8)	●			8	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CA0}	External Capacitive Load on Address Pin CA0		●			10	pF
AC Performance							
t_s	Settling Time	V_{CC} = 3V (Note 9) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.4 4.0 4.5		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2.8		nV•s
	DAC-to-DAC Crosstalk	1 DAC Held at FS, 1 DAC Switch 0-FS			5.2		nV•s
	Multiplying Bandwidth	External Reference			320		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			180 160 200 180		nV/√Hz nV/√Hz nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference C_{REF} = 0.1µF			30 35 680 730		$µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V. (See Figure 1) (Note 13)

LTC2633-LI12/-LI10/-LI8/-LX12/-LX10/-LX8/-LZ12/-LZ10/-LZ8/-LO12/-LO10/-LO8/LTC2633A-LI12/-LX12/-LZ12/-LO12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-HI12/-HI10/-HI8/-HZ12/-HZ10/-HZ8/LTC2633A-HI12/-HZ12 (V_{FS} = 4.096V)

				LTC2633-8			LTC2633-10			LTC2633-12			LTC2633A-12			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 5V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero Scale Error	V_{CC} = 5V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 5V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 5V, Internal Ref.			±10			±10			±10			±10		µV/°C
GE	Gain Error	V_{CC} = 5V, Internal Ref.	●		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8	%FSR
GE_{TC}	Gain Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 10) C-Grade H-Grade			 10 10			 10 10			 10 10			 10 10		 ppm/°C ppm/°C
	Load Regulation	V_{CC} = 5V ± 10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.006	0.01		0.022	0.04		0.09	0.16		0.09	0.16	LSB/mA
R_{OUT}	DC Output Impedance	V_{CC} = 5V ± 10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.09	0.156		0.09	0.156		0.09	0.156		0.09	0.156	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-HI12/-HI10/-HI8/-HZ12/-HZ10/-HZ8/LTC2633A-HI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 4.096		V V
PSR	Power Supply Rejection	V_{CC} = 5V ± 10%			–80		dB
I_{SC}	Short Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero Scale; V_{OUT} shorted to V_{CC} Full Scale; V_{OUT} shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 5V, V_{REF} =4.096V, External Reference V_{CC} = 5V, Internal Reference	● ●		0.4 0.5	0.6 0.7	mA mA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V	●		0.5	2	µA
Reference Input							
	Input Voltage Range		●	1		V_{CC}	V
	Resistance		●	120	160	200	kΩ
	Capacitance				12		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.005	5	µA
Reference Output							
	Output Voltage		●	2.032	2.048	2.064	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short Circuit Current	V_{CC} = 5.5V, REF Shorted to GND			4		mA
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)	(Note 14)	●	–0.5		$0.3V_{CC}$	V
V_{IH}	High Level Input Voltage (SDA and SCL)	(Note 11)	●	$0.7V_{CC}$			V
$V_{IL(CA0)}$	Low Level Input Voltage on CA0	See Test Circuit 1	●			$0.15V_{CC}$	V
$V_{IH(CA0)}$	High Level Input Voltage on CA0	See Test Circuit 1	●	$0.85V_{CC}$			V
R_{INH}	Resistance from CA0 to V_{CC} to Set CA0 = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA0 to GND to Set CA0 = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA0 to V_{CC} or GND to Set CA0 = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	V_O = $V_{IH(MIN)}$ to V_O = $V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 12)	●	$20 + 0.1C_B$		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2633-HI12/-HI10/-HI8/-HZ12/-HZ10/-HZ8/LTC2633A-HI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	I/O Pin Capacitance	(Note 8)	●			8	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CA0}	External Capacitive Load on Address Pin CA0		●			10	pF
AC Performance							
t_s	Settling Time	V_{CC} = 5V (Note 9) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.7 4.0 4.7		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			3.0		nV•s
	DAC-to-DAC Crosstalk	1 DAC Held at FS, 1 DAC Switch 0-FS			6.7		nV•s
	Multiplying Bandwidth	External Reference			320		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			180 160 250 230		nV/√Hz nV/√Hz nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference C_{REF} = 0.1µF			30 40 680 750		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V. (See Figure 1) (Note 13)

LTC2633-HI12/-HI10/-HI8/-HZ12/-HZ10/-HZ8/LTC2633A-HI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltages are with respect to GND

Note 3. High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

Note 4. Linearity and monotonicity are defined from code k_L to code 2^N–1, where N is the resolution and k_L is given by $k_L = 0.016 \bullet (2^N / V_{FS})$, rounded to the nearest whole code. For V_{FS} = 2.5V and N = 12, k_L = 26 and linearity is defined from code 26 to code 4,095. For V_{FS} = 4.096V and N = 12, k_L = 16 and linearity is defined from code 16 to code 4,095.

Note 5. Inferred from measurement at code 16 (LTC2633-12), code 4 (LTC2633-10) or code 1 (LTC2633-8), and at full scale.

Note 6. This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7. Digital inputs at 0V or V_{CC}.

Note 8. Guaranteed by design and not production tested.

Note 9. Internal reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

Note 10. Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 11. Maximum $V_{IH} = V_{CC(MAX)} + 0.5V$

Note 12. C_B = capacitance of one bus line in pF

Note 13. All values refer to $V_{IH} = V_{IH(MIN)}$ and $V_{IL} = V_{IL(MAX)}$ levels.

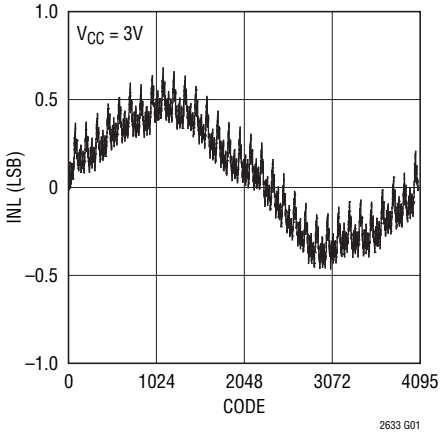
Note 14. Minimum V_{IL} exceeds the absolute maximum rating. This condition won't damage the IC, but could degrade performance.

TYPICAL PERFORMANCE CHARACTERISTICS

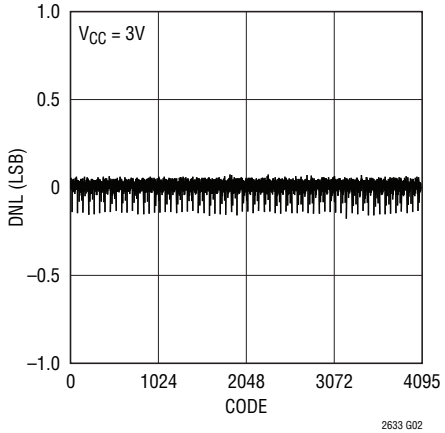
T_A = 25°C unless otherwise noted.

LTC2633-L12 (Internal Reference, V_{FS} = 2.5V)

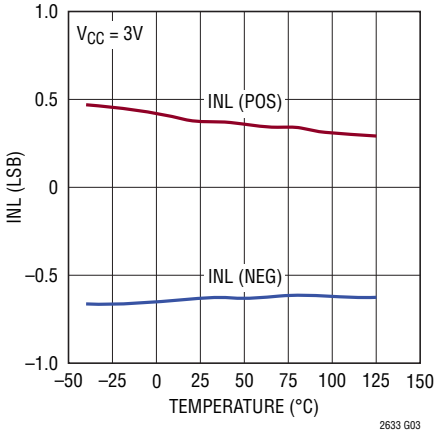
Integral Nonlinearity (INL)



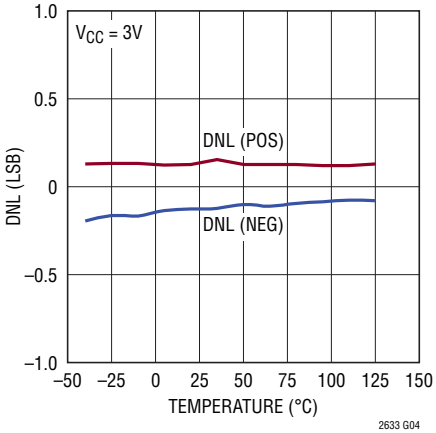
Differential Nonlinearity (DNL)



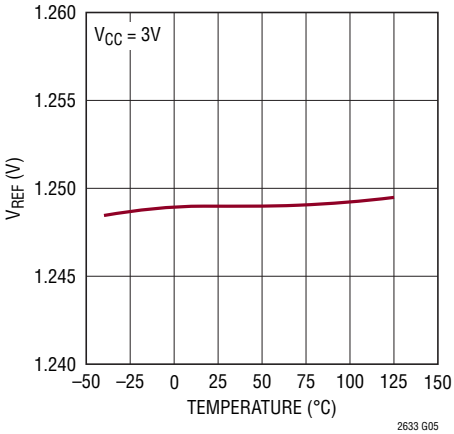
INL vs Temperature



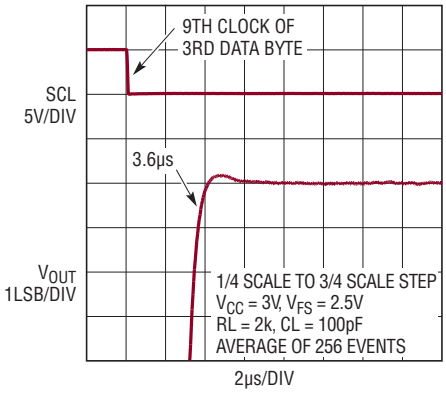
DNL vs Temperature



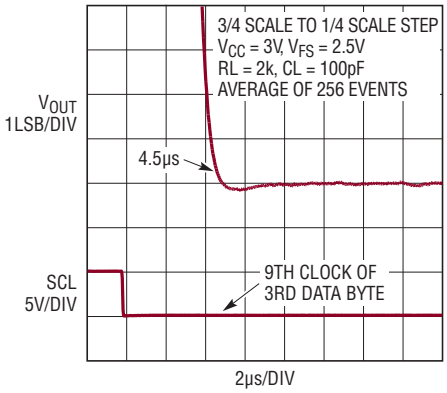
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



Settling to ±1LSB Falling

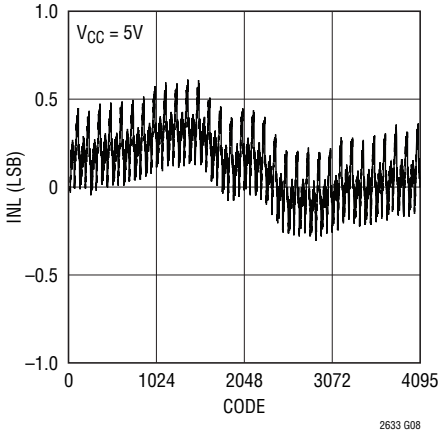


TYPICAL PERFORMANCE CHARACTERISTICS

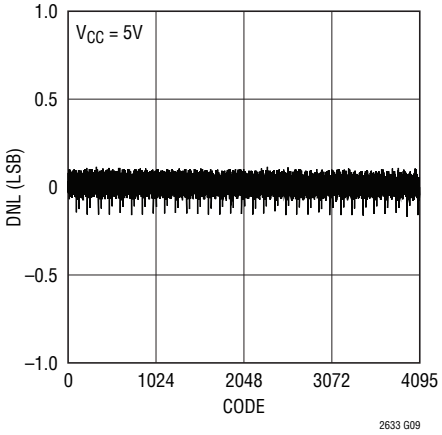
T_A = 25°C unless otherwise noted.

LTC2633-H12 (Internal Reference, V_{FS} = 4.096V)

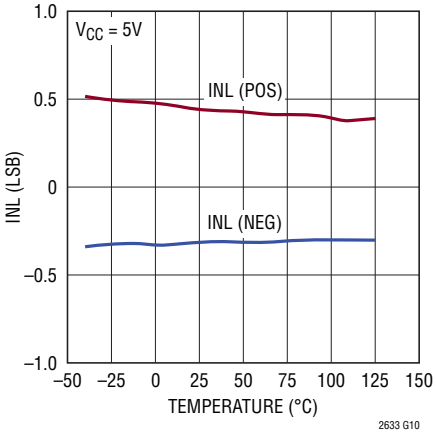
Integral Nonlinearity (INL)



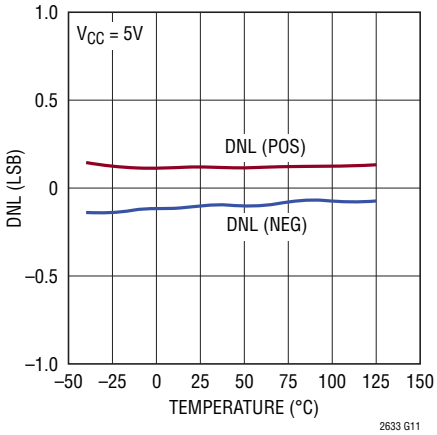
Differential Nonlinearity (DNL)



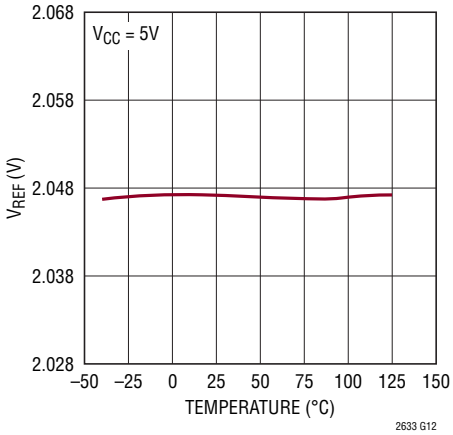
INL vs Temperature



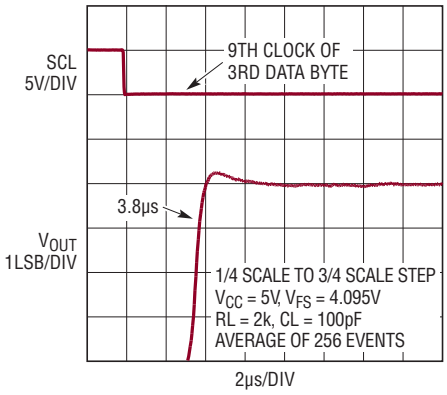
DNL vs Temperature



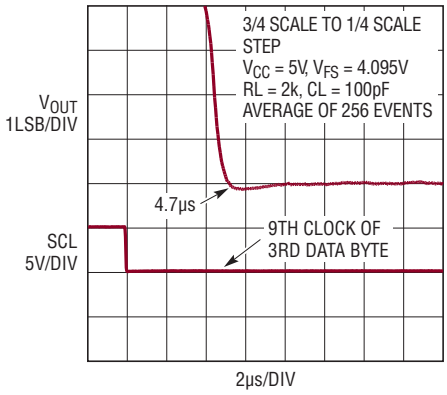
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



Settling to ±1LSB Falling

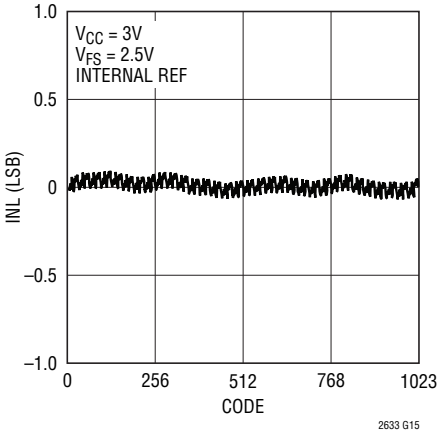


TYPICAL PERFORMANCE CHARACTERISTICS

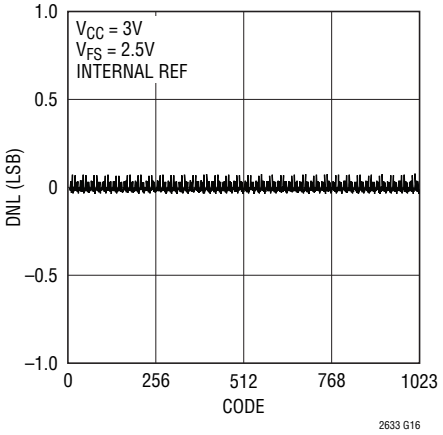
T_A = 25°C unless otherwise noted.

LTC2633-10

Integral Nonlinearity (INL)

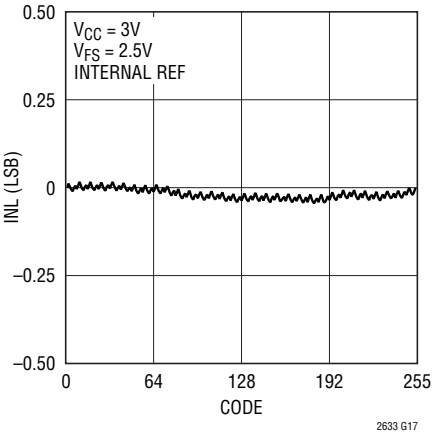


Differential Nonlinearity (DNL)

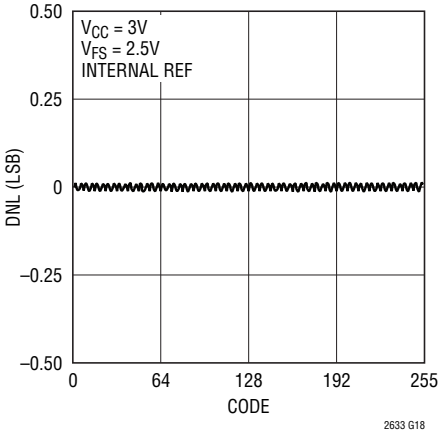


LTC2633-8

Integral Nonlinearity (INL)

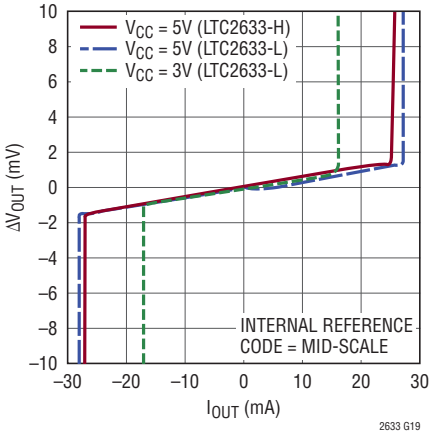


Differential Nonlinearity (DNL)

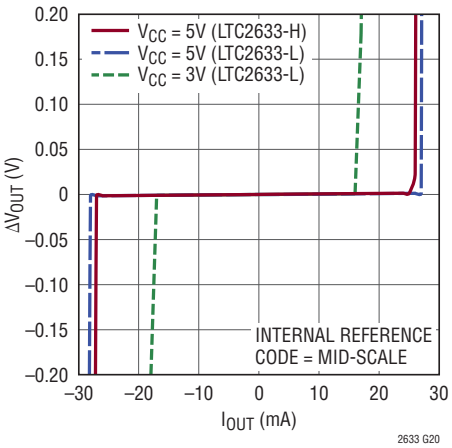


LTC2633

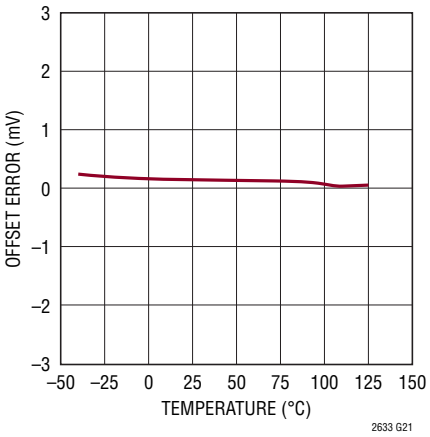
Load Regulation



Current Limiting



Offset Error vs Temperature

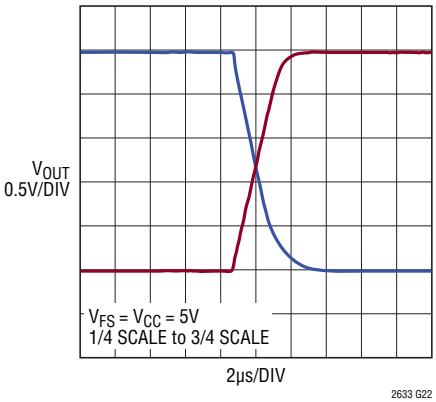


TYPICAL PERFORMANCE CHARACTERISTICS

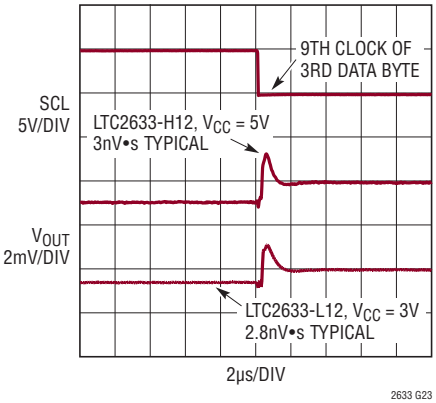
T_A = 25°C unless otherwise noted.

LTC2633

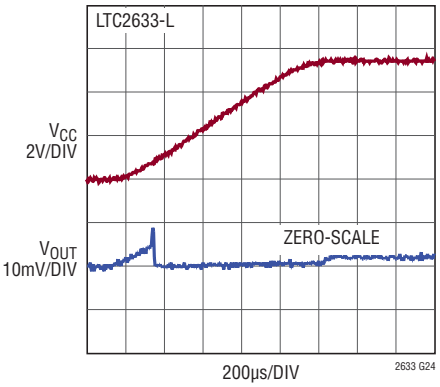
Large-Signal Response



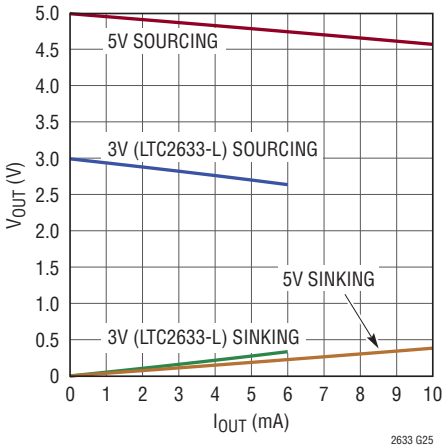
Mid-Scale-Glitch Impulse



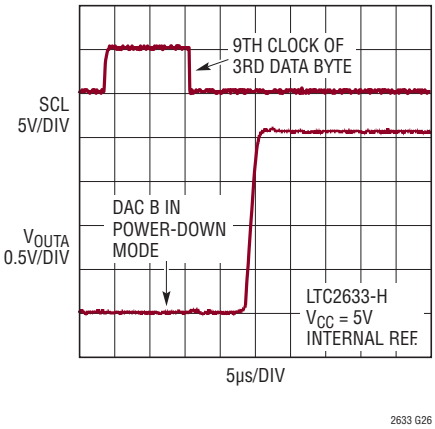
Power-On Reset Glitch



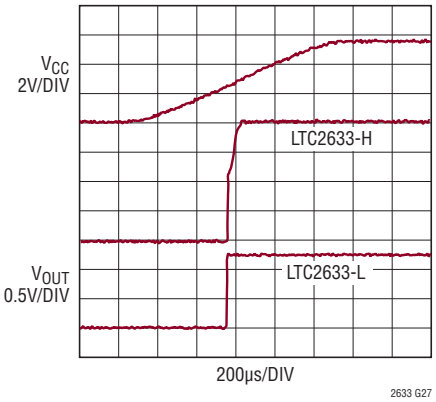
Headroom at Rails vs Output Current



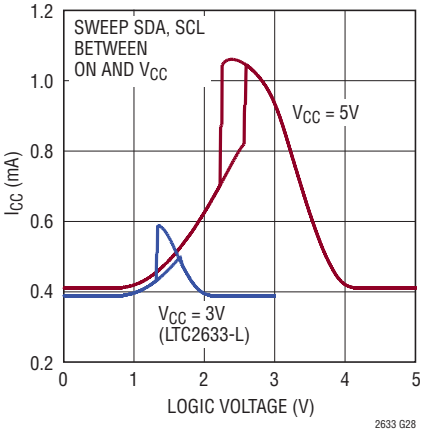
Exiting Power-Down to Mid-Scale



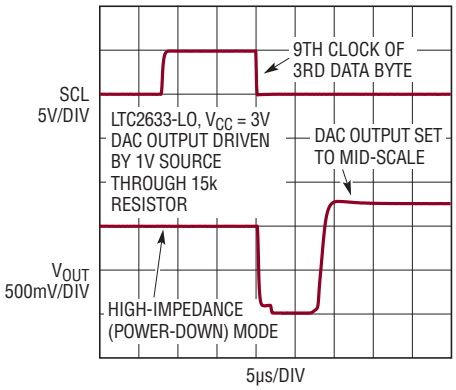
Power-On Reset to Mid-Scale



Supply Current vs Logic Voltage



Exiting Power-Down for Hi-Z Option

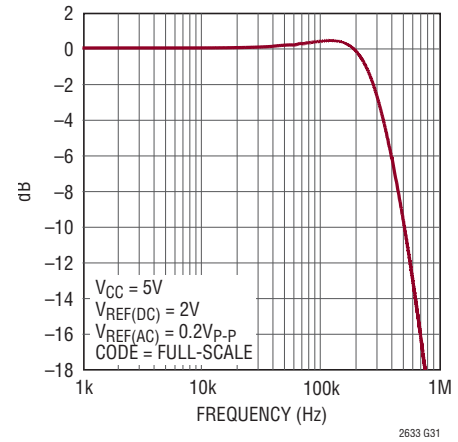


TYPICAL PERFORMANCE CHARACTERISTICS

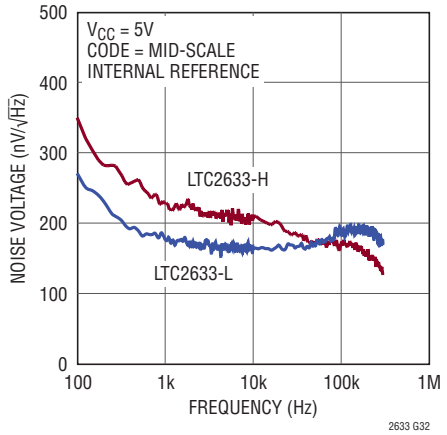
T_A = 25°C unless otherwise noted.

LTC2633

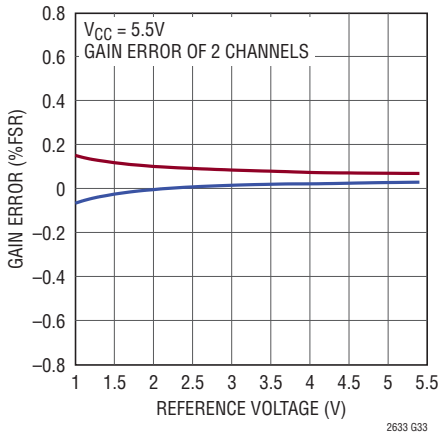
Multiplying Bandwidth



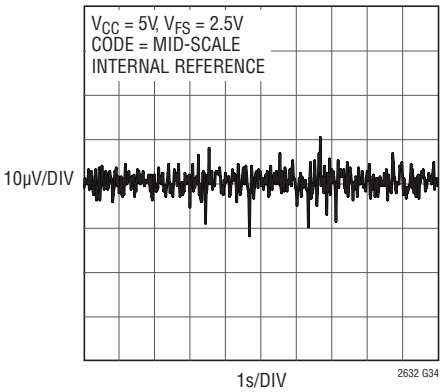
Noise Voltage vs Frequency



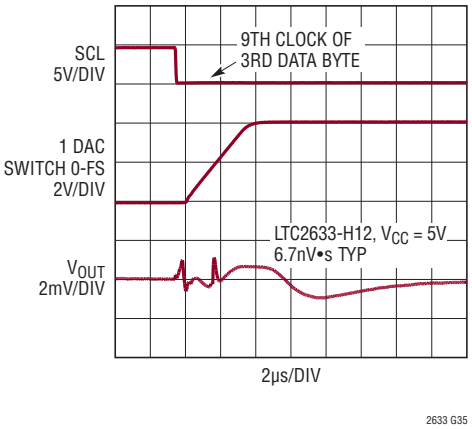
Gain Error vs Reference Input



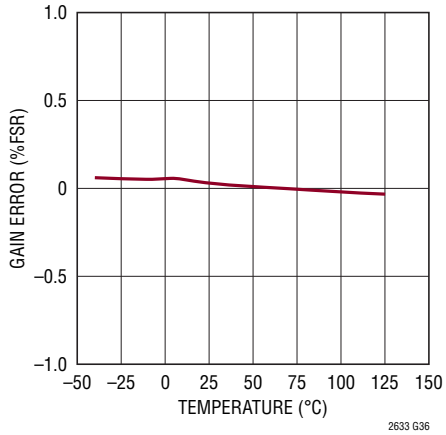
0.1Hz to 10Hz Voltage Noise



DAC to DAC Crosstalk (Dynamic)



Gain Error vs Temperature



PIN FUNCTIONS

SCL (Pin 1): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

CA0 (Pin 2): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (see Table 1).

REF (Pin 3): Reference Voltage Input or Output. When external reference mode is selected, REF is an input ($1V \leq V_{REF} \leq V_{CC}$) where the voltage supplied sets the full-scale DAC output voltage. When internal reference is selected, the 10ppm/°C 1.25V (LTC2633-L) or 2.048V (LTC2633-H) internal reference (half full-scale) is available at the pin. This output may be bypassed to GND with up to 10µF (0.1µF is recommended) and must be buffered when driving external DC load current.

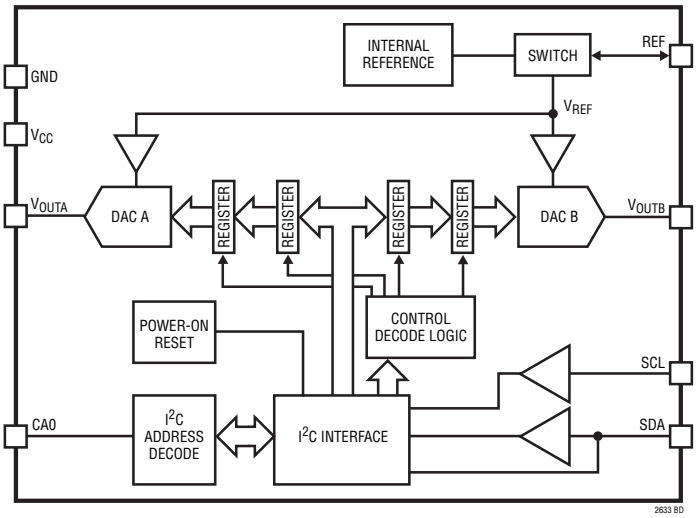
GND (Pin 4): Ground.

V_{OUTA}, V_{OUTB} (Pins 5,6): DAC Analog Voltage Output.

V_{CC} (Pin 7): Supply Voltage Input. $2.7V \leq V_{CC} \leq 5.5V$ (LTC2633-L) or $4.5V \leq V_{CC} \leq 5.5V$ (LTC2633-H). Bypass to GND with a 0.1µF capacitor.

SDA (Pin 8): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. This pin is high impedance while data is shifted in. Open drain N-channel output during acknowledgement. SDA requires a pull-up resistor or current source to V_{CC}.

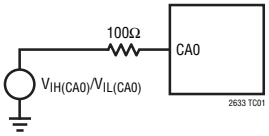
BLOCK DIAGRAM



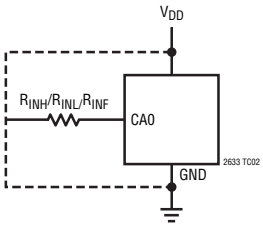
TEST CIRCUIT

Test circuits for I²C digital I/O (see Electrical Characteristics)

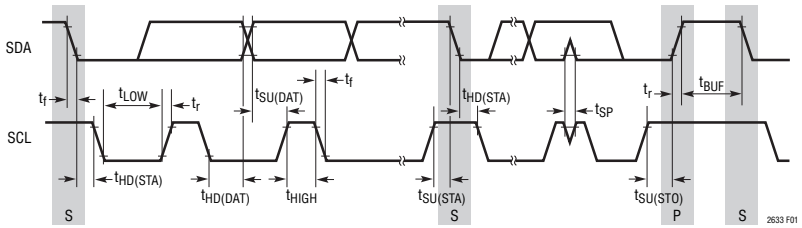
Test Circuit 1



Test Circuit 2



TIMING DIAGRAM



ALL VOLTAGE LEVELS REFER TO $V_{IH(MIN)}$ AND $V_{IL(MAX)}$ LEVELS

Figure 1. I²C Timing

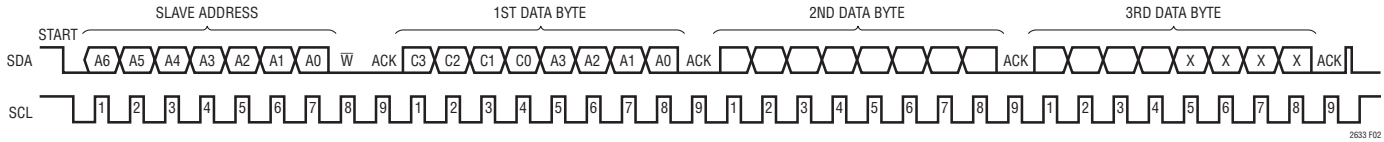


Figure 2. Typical LTC2633 Write Transaction

OPERATION

The LTC2633 is a family of dual voltage output DACs in an 8-lead TSOT package. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. Eighteen combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero-scale, mid-scale in internal reference mode, or mid-scale in external reference mode), DAC power-down output load (high impedance or 200kΩ), and full-scale voltage (2.5V or 4.096V) are available. The LTC2633 is controlled using a 2-wire I^2C interface.

Power-On Reset

The LTC2633-HZ/LTC2633-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2633 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 10mV above zero scale during power-on. In general, the glitch amplitude decreases as the power supply ramp time is increased. See power-on reset glitch in the Typical Performance Characteristics section.

The LTC2633-HI/LTC2633-LI/LTC2633-LX provide an alternative reset, setting the output to mid-scale when power is first applied. The LTC2633-LI/ and LTC2633-HI power up in internal reference mode, with the output set to a mid-scale voltage of 1.25V and 2.048V respectively. The LTC2633-LX power-up in external reference mode, with the output set to mid-scale of the external reference. The LTC2633-LO powers up in internal reference mode with all the DAC channels placed in the high impedance state (powered down). Input and DAC registers are set to the mid-scale code, and only the internal reference is powered up, causing supply current to be typically 180µA upon power up. Default reference mode selection is described in the Reference Modes section.

Power Supply Sequencing

The voltage at REF (Pin 3) must be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and V_{REF} is either 2.5V (LTC2633-LI/LTC2633-LX/LTC2633-LO/LTC2633-LZ) or 4.096V (LTC2633-HI/LTC2633-HZ) when in internal reference mode, and the voltage at REF when in external reference mode.

I^2C Serial Interface

The LTC2633 communicates with a host using the standard 2-wire I^2C interface. The Timing Diagram (Figures 1 and 2) show the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be necessary if the bus capacitance is greater than 200pF.

The LTC2633 is a receive-only (slave) device. The master can write to the LTC2633. The LTC2633 will not acknowledge (NAK) a read request from the master.

OPERATION

START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Acknowledge

The acknowledge (ACK) signal is used for handshaking between the master and the slave. An ACK generated by the slave lets the master know that the latest byte of information was properly received. The ACK related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the ACK clock pulse. The slave-receiver must pull down the SDA bus line during the ACK clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2633 responds to a write by a master in this manner but does not acknowledge a read operation; in that case, SDA is retained HIGH during the period of the ACK clock pulse.

Chip Address

The state of pin CA0 determines the slave address of the part. This pin can be set to any one of three states: V_{CC}, GND or float. This results in 3 selectable addresses for the part. The slave address assignments is shown in Table 1.

Table 1. Slave Address Map

CA0	A6	A5	A4	A3	A2	A1	A0
GND	0	0	1	0	0	0	0
FLOAT	0	0	1	0	0	0	1
V_{CC}	0	0	1	0	0	1	0
GLOBAL ADDR	1	1	1	0	0	1	1

In addition to the address selected by the address pin, the part also responds to a global address. This address allows a common write to all LTC2633 parts to be accomplished using one 3-byte write transaction on the I^2C bus. The global address, listed at the end of Tables 1, is a 7-bit hardwired address not selectable by CA0. If another address is required, please consult the factory.

The maximum capacitive load allowed on the address pin (CA0) is 10pF, as these pins are driven during address detection to determine if they are floating.

Write Word Protocol

The master initiates communication with the LTC2633 with a START condition and a 7-bit slave address followed by the write bit (W) = 0. The LTC2633 acknowledges by pulling the SDA pin low at the 9th clock if the 7-bit slave address matches the address of the part (set by CA0) or the global address. The master then transmits three bytes of data. The LTC2633 acknowledges each byte of data by pulling the SDA line low at the 9th clock of each data byte transmission. After receiving three complete bytes of data, the LTC2633 executes the command specified in the 24-bit input word.

If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2633 does not acknowledge the extra bytes of data (SDA is high during the 9th clock).

OPERATION

The format of the three data bytes is shown in Figure 3. The first byte of the input word consists of the 4-bit command, followed by the 4-bit DAC address. The next two bytes contain the 16-bit data word, which consists of the 12-, 10- or 8-bit input code, MSB to LSB, followed by 4, 6 or 8 don't-care bits (LTC2633-12, LTC2633-10 and LTC2633-8 respectively). A typical LTC2633 write transaction is shown in Figure 4.

The command bit assignments (C3-C0) and address (A3-A0) assignments are shown in Tables 3 and 4. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register. In an update operation, the data word is copied from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 12-, 10-, or 8-bit input code, and is converted to an analog voltage at the DAC output. Write to and update combines the first two commands. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

Table 3. Command Codes

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power-Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power-Up) All
0	0	1	1	Write to and Update (Power-Up) DAC Register n
0	1	0	0	Power-Down n
0	1	0	1	Power-Down Chip (All DAC's and Reference)
0	1	1	0	Select Internal Reference (Power-Up Reference)
0	1	1	1	Select External Reference (Power-Down Internal Reference)
1	1	1	1	No Operation

*Command codes not shown are reserved and should not be used.

Table 4. Address Codes

ADDRESS (n)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
1	1	1	1	All DACs

* Address codes not shown are reserved and should not be used.

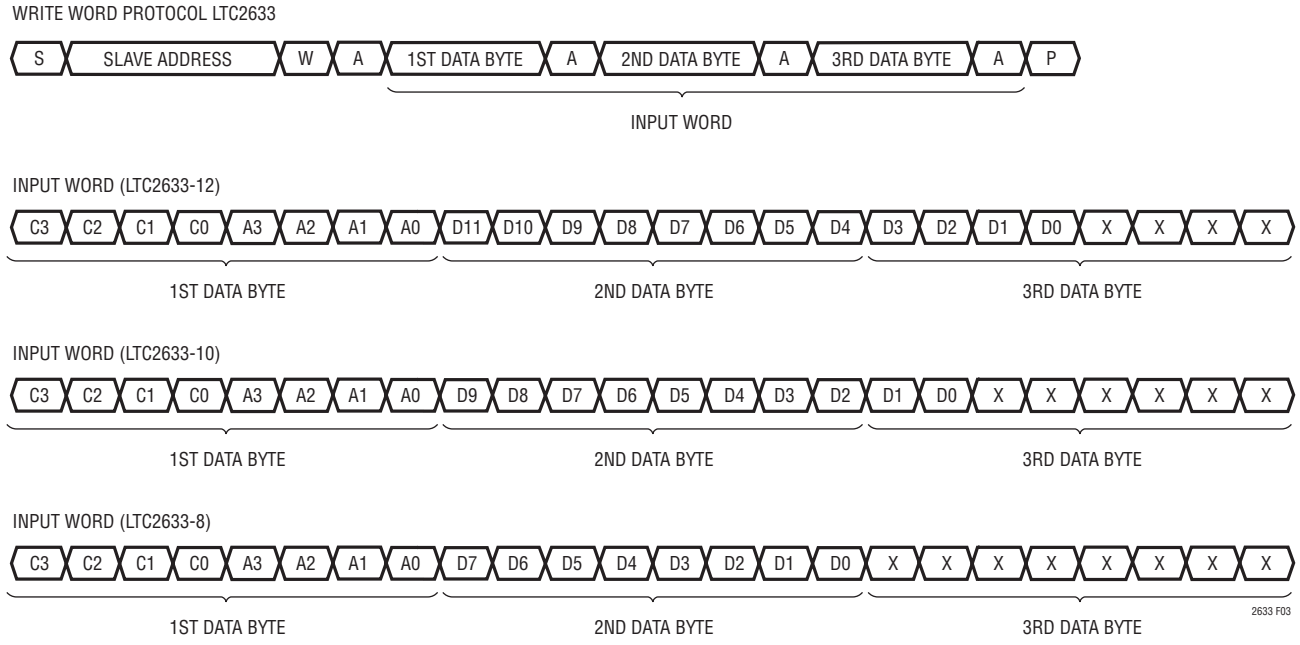


Figure 3. Command and Data Input Format

OPERATION

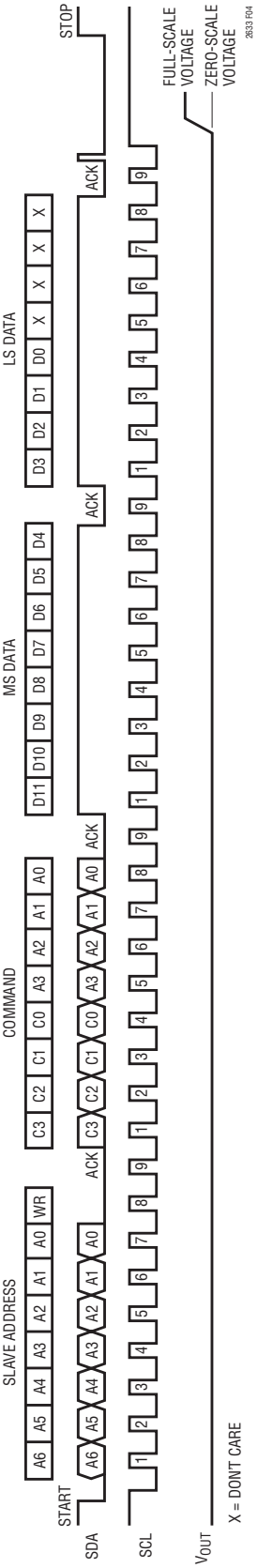


Figure 4. Typical LTC2633 Input Waveform—Programming DAC Output for Full Scale

OPERATION

Reference Modes

For applications where an accurate external reference is either not available, or not desirable due to limited space, the LTC2633 has a user-selectable, integrated reference. The integrated reference voltage is internally amplified by 2x to provide the full-scale DAC output voltage range. The LTC2633-LI/LTC2633-LX/LTC2633-LO/LTC2633-LZ provides a full-scale output of 2.5V. The LTC2633-HI/LTC2633-HZ provides a full-scale output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal reference mode can be selected by using command 0110b, and is the power-on default for LTC2633-HZ/LTC2633-LZ, as well as for LTC2633-HI/LTC2633-LI/LTC2633-LO.

The 10ppm/°C, 1.25V (LTC2633-LI/LTC2633-LX/LTC2633-LO/LTC2633-LZ) or 2.048V (LTC2633-HI/LTC2633-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; 0.1µF is recommended and up to 10µF can be driven without oscillation. This output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in external reference mode using command 0111b. In this mode, an input voltage supplied externally to the REF pin provides the reference ($1V \le V_{REF} \le V_{CC}$) and the supply current is reduced. The external reference voltage supplied sets the full-scale DAC output voltage. External reference mode is the power-on default for LTC2633-LX.

The reference mode of LTC2633-HZ/LTC2633-LZ/LTC2633-HI/LTC2633-LI/LTC2633-LO (internal reference power-on default), can be changed by software command after power up. The same is true for LTC2633-LX (external reference power-on default).

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than two DAC outputs are needed. When in power-down, the buffer amplifiers, bias circuits, and integrated reference circuits are disabled, and draw essentially zero current. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 200kΩ resistors (LTC2633-LI/LTC2633-LX/LTC2633-LO/LTC2633-LZ/LTC2633-HI/LTC2633-HZ). For the LTC2633-LO options, the output pins are not passively pulled to ground, but are also placed in a high impedance state (open-circuited state) during power-down, typically drawing less than 0.1µA. The LTC2633-LO options power-up with all DAC outputs in this high impedance state. They remain that way until given a software update command. For all LTC2633 options, Input- and DAC-register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (n). The supply current is reduced approximately 30% for each DAC powered down. The integrated reference is automatically powered down when external reference is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using Power Down Chip command 0101b. When the integrated reference is in power-down mode, the REF pin becomes high impedance (typically > 1GΩ). For all power-down commands the 16-bit data word is ignored.

Normal operation resumes after executing any command that includes a DAC update, (as shown in Table 1). The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than two DACs are in a powered-down state prior to the update command, the power-up delay time is 10µs. However, if both DACs and the integrated reference are powered down, then the main bias generation circuit block has been automatically shut down in addition to the DAC amplifiers and reference buffers. In this case, the power up delay time is 12µs. The power-up of the integrated reference depends on the command that powered it down. If the reference is powered down using the select external reference command (0111b), then it can only be powered back up using select internal reference command (0110b). However, if the reference was powered down using power down chip command (0101b), then in addition to select

OPERATION

internal reference command (0110b), any command in software that powers up the DACs will also power up the integrated reference.

Voltage Output

The LTC2633's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ω. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit for the lowest codes as shown in Figure 5b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC}, as shown in Figure 5c. No full-scale limiting can occur if V_{REF} is less than V_{CC}–FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

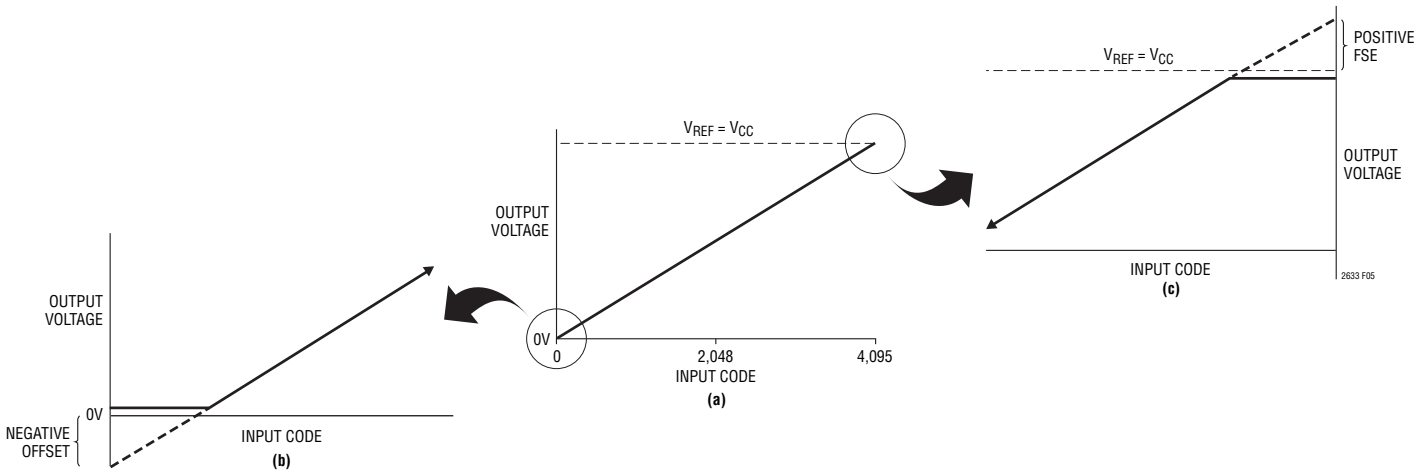


Figure 5. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown for 12 Bits).
(a) Overall Transfer Function
(b) Effect of Negative Offset for Codes Near Zero
(c) Effect of Positive Full-Scale Error for Codes Near Full Scale

OPERATION

Board Layout

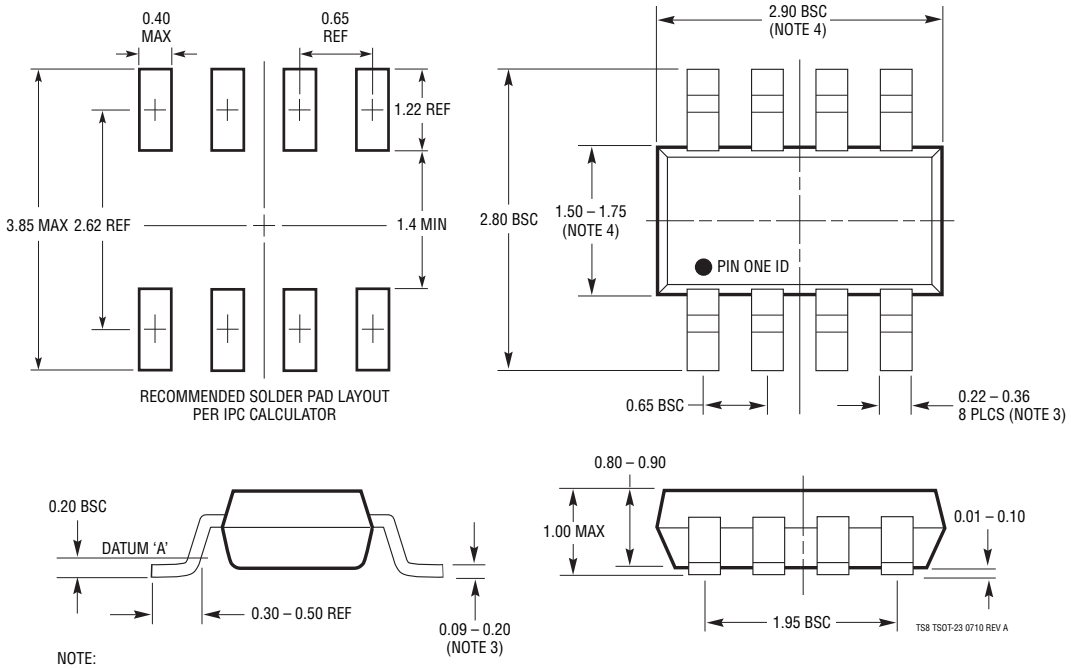
The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2633 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2633 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2633 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

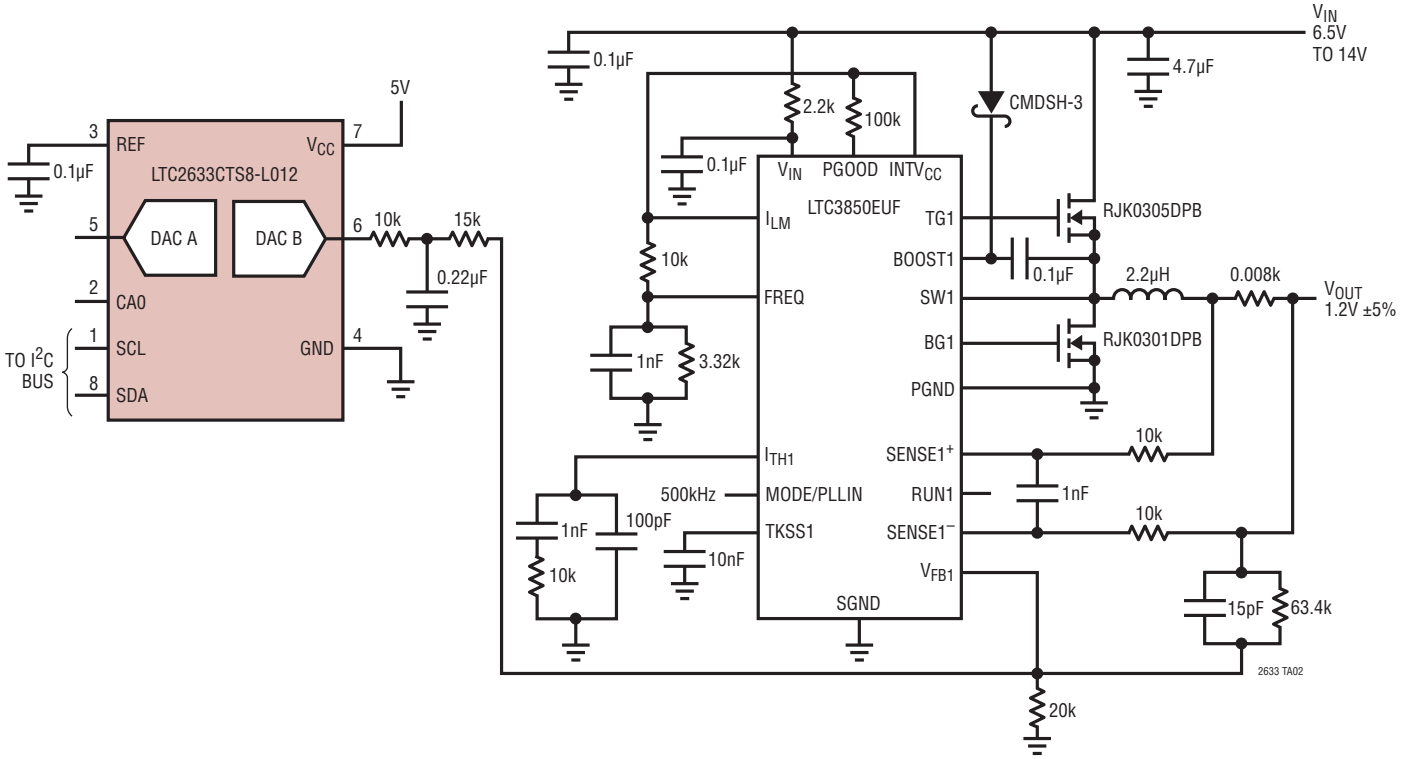
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/11	Revised part numbering.	2 to 9, 13, 16, 20, 26
B	3/11	Revised title of Typical Application.	24

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Voltage Margining Application with LTC3850 (1.2V ±5%) LTC2633-LO Option Only



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2607/LTC2617/ LTC2627	Dual 16-/14-/12-Bit, I^2C V_{OUT} DACs with External Reference	260µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 16-Lead SSOP Package
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
LTC1662	Dual 10-Bit, SPI V_{OUT} DAC with External Reference	1.5µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
LTC2630/LTC2631	Single 12-/10-/8-Bit, SPI/ I^2C V_{OUT} DACs with 10ppm/°C Reference	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, in SC70 (LTC2630)/ ThinSOT (LTC2631)
LTC2640	Single 12-/10-/8-Bit, SPI V_{OUT} DACs with 10ppm/°C Reference	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, in ThinSOT
LTC2634/LTC2635	Quad 12-/10-/8-Bit SPI/I^2C V_{OUT} DACs with 10ppm/°C Reference	±2.5LSB INL, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, 16-Pin 3mm × 3mm QFN and 10-Lead MSOP Packages
LTC2636/LTC2637	Octal 12-/10-/8-Bit, SPI/I^2C V_{OUT} DACs with 10ppm/°C Reference	125µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 14-Lead 4mm × 3mm DFN and 16-Lead MSOP Packages
LTC2654/LTC2655	Quad 16-/12 Bit, SPI/I^2C V_{OUT} DACs with 10ppm/°C Max Reference	±4LSB INL Max at 16-Bits and ±2mV Offset Error, Rail-to-Rail Output, 20-Lead 4mm × 4mm QFN and 16-Lead Narrow SSOP Packages
LTC2656/LTC2657	Octal 16-/12 Bit, SPI/I^2C V_{OUT} DACs with 10ppm/°C Max Reference	±4LSB INL Max at 16-Bits and ±2mV Offset Error, Rail-to-Rail Output, 20-Lead 4mm × 5mm QFN and 16-Lead TSSOP Packages

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