40V, 1A Synchronous Step-Down Converter

FEATURES

- **Wide Input Voltage Range: 4.0V to 40V**
- **1A Guaranteed Output Current**
- **High Efficiency: Up to 95%**
- **Wide Output Voltage Range**
  - **LTC3646: 2.0V to 30V**
  - **LTC3646-1: 0.6V to 15V**
- **±1% Accurate Reference Voltage**
- Internal or External Compensation
- Switching Frequency Adjustable and Synchronizable: 200kHz to 3MHz
- Selectable High Efficiency Burst Mode® Operation or Forced Continuous Mode
- 14 Lead 3mm × 4mm DFN or Thermally Enhanced 16-Lead MSOP Packages

APPLICATIONS

- Point of Load Power Supplies
- Intermediate Bus Power
- Automotive Applications

DESCRIPTION

The LTC®3646 is a high efficiency, step-down DC/DC converter with internal high side and synchronous power FETs. It draws only 140μA typical DC supply current in Burst Mode operation at no load while maintaining output voltage regulation.

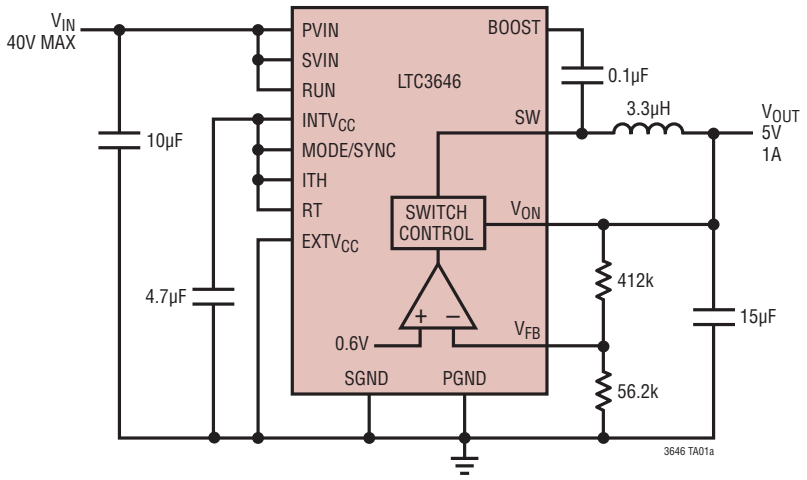
The LTC3646 can supply up to a 1A load, and its combination of Burst Mode operation, integrated power switches and low quiescent current provides high efficiency over a broad range of load currents. Alternatively, it can be used in forced continuous mode for ripple sensitive applications.

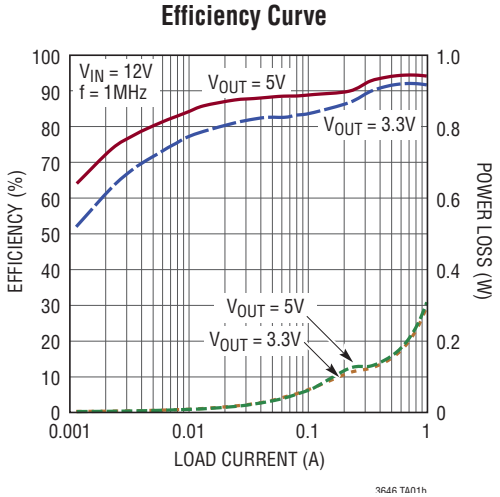
The LTC3646 has a wide 4.0V to 40V input range and its patented controlled on-time architecture and 0.6V reference voltage allow for large step-down ratios without the risk of output overvoltage. The frequency may be set between 200kHz and 3.0MHz with a program resistor or synchronized to an external clock.

The internal soft-start, short-circuit protection and voltage rating make the LTC3646 a robust part ideal for high voltage applications.

, LT, LTC, LTM, Linear Technology, the Linear logo and Burst Mode are registered trademarks and Hot Swap is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents, including 6580258, 5481178, 5994885, 6304066, 5847554, 6476589, 6774611.

TYPICAL APPLICATION

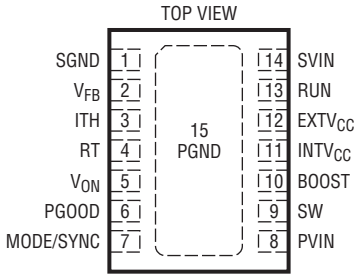




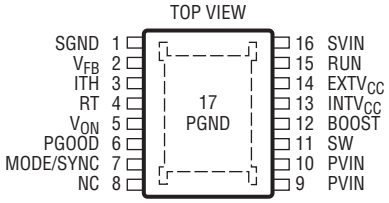
ABSOLUTE MAXIMUM RATINGS (Notes 1, 7)

PVIN, SVIN Supply Voltage ..... –0.3V to 45V
SW Voltage (DC) ..... –0.3V to PVIN + 0.3V
BOOST – SW Voltage ..... –0.3V to 6V
V_{ON} Voltage ..... –0.3V to 33V
MODE/SYNC, RT, ITH,
V_{FB} Voltage ..... –0.3V to $INTV_{CC}$ + 0.3V
$INTV_{CC}$ Voltage ..... –0.3V to 6V
$EXTV_{CC}$ Voltage ..... –0.3V to 6V
RUN Voltage ..... –0.3V to 45V
PGOOD ..... –0.3V to $INTV_{CC}$ + 0.3V
Operating Junction Temperature Range
(Notes 2, 7) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) MSE ..... 300°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 15) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3646EDE#PBF	LTC3646EDE#TRPBF	3646	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3646IDE#PBF	LTC3646IDE#TRPBF	3646	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3646HDE#PBF	LTC3646HDE#TRPBF	3646	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3646EMSE#PBF	LTC3646EMSE#TRPBF	3646	16-Lead Plastic MSOP	–40°C to 85°C
LTC3646IMSE#PBF	LTC3646IMSE#TRPBF	3646	16-Lead Plastic MSOP	–40°C to 125°C
LTC3646HMSE#PBF	LTC3646HMSE#TRPBF	3646	16-Lead Plastic MSOP	–40°C to 150°C
LTC3646EDE-1#PBF	LTC3646EDE-1#TRPBF	36461	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3646IDE-1#PBF	LTC3646IDE-1#TRPBF	36461	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3646HDE-1#PBF	LTC3646HDE-1#TRPBF	36461	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3646EMSE-1#PBF	LTC3646EMSE-1#TRPBF	36461	16-Lead Plastic MSOP	–40°C to 85°C
LTC3646IMSE-1#PBF	LTC3646IMSE-1#TRPBF	36461	16-Lead Plastic MSOP	–40°C to 125°C
LTC3646HMSE-1#PBF	LTC3646HMSE-1#TRPBF	36461	16-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), PVIN = SVIN = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (PVIN, SVIN)							
V_{IN}	Input Voltage Operating Range		●	4.0		40	V
$V_{IN(OV)}$	Input Supply Overvoltage Lockout	V_{IN} Rising Hysteresis (V_{IN} Falling)	● ●	43.5 2.0	46 2.5	 2.9	V V
$V_{IN(UV)}$	Input Supply Undervoltage Lockout	V_{IN} Falling Hysteresis (V_{IN} Rising)		3.2	3.35 250	3.5	V mV
I_Q	DC Supply Current (Note 3) Forced Continuous Sleep Mode Shutdown Mode	 V_{RUN} = 0V			 620 140 8	 875 190	 µA µA µA
Main Control Loop							
V_{OUT}	Output Voltage Range (Note 4)	LTC3646 LTC3646-1		2.0 0.6		30 15	V V
V_{FB}	Feedback Reference Voltage	–40°C < T_A < 85°C	 ●	0.594 0.591	0.6 0.6	0.606 0.609	V V
	Feedback Voltage Line Regulation	V_{IN} = 4.0V to 40V, I_{TH} = 1.5V				0.05	%/V
	Feedback Voltage Load Regulation	I_{TH} = 1.0V to 1.8V				0.12	%
	Feedback Input Current	V_{FB} = 0.6V	●		0	±20	nA
$g_{m(EA)}$	Error Amplifier Transconductance	External Comp			300		µS
$t_{ON(MIN)}$	Minimum On-Time	V_{IN} = 40V, R_{RT} = 30k, V_{ON} = 2V			30		ns
$t_{OFF(MIN)}$	Minimum Off-Time				80		ns
I_{LIM}	Valley Switch Current Limit		●	0.9	1.2	1.5	A
	Negative Valley Switch Current Limit				–0.3		A
	Internal Oscillator Frequency	V_{RT} = V_{INTVCC} R_{RT} = 450kΩ R_{RT} = 60kΩ R_{RT} = 30kΩ		1.6 0.19 1.25 2.55	2.25 0.2 1.5 3.0	2.95 0.27 1.75 3.45	MHz MHz MHz MHz
	External Clock Frequency Range			0.2		3.0	MHz
$R_{DS(ON)}$	Top Switch On-Resistance (Note 5) Bottom Switch On-Resistance (Note 5)	V_{IN} = 5.5V V_{IN} = 5.5V			200 120		mΩ mΩ
	Switch Leakage	V_{IN} = V_{SW} = 40V, V_{RUN} = 0V V_{IN} = 40V, V_{SW} = 0V, V_{RUN} = 0V				±1 ±1	µA µA
Internal V_{CC} Regulator							
V_{INTVCC}	$INTV_{CC}$ Voltage	I_{INTVCC} = 5mA	●	4.8	5.0	5.2	V
	$INTV_{CC}$ Load Regulation (Note 6)	I_{INTVCC} = 0mA to 5mA			0.5		%
	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling			3.0		V
	$INTV_{CC}$ UVLO Hysteresis				0.3		V
	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising		4.25	4.5	4.65	V
	$EXTV_{CC}$ Hysteresis				200		mV
Operation							
V_{RUN}	RUN Pin Threshold	RUN Rising RUN Falling Hysteresis		1.17 1.06	1.21 1.10 110	1.26 1.14	V V mV
	RUN Pin Leakage Current	RUN = 1.3V			0	±1	µA
$V_{PGOOD(UT)}$	PGOOD Overvoltage Threshold	FB Rising FB Falling		5.0 3.5	7.5 5	10	$\%V_{FB}$ $\%V_{FB}$
$V_{PGOOD(LT)}$	PGOOD Undervoltage Threshold	FB Falling FB Rising		–5.0 –3.5	–7.5 –5	–10	$\%V_{FB}$ $\%V_{FB}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), PVIN = SVIN = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PGOOD}	PGOOD Filter Time	RT = $INTV_{CC}$		15	30		µs
R_{PGOOD}	PGOOD Pull-Down Resistance	I_{PGOOD} = 10mA			63		Ω
	PGOOD Leakage	V_{PGOOD} = V_{INTVCC}				1.0	µA
t_{SS}	Internal Soft-Start Time				250	500	µs
$V_{MODE/SYNC}$	Mode Threshold Voltage	Mode V_{IH}	●	1.2			V
		Mode V_{IL}	●			0.3	V
	SYNC Threshold Voltage	$SYNC_{IH}$	●	1.2			V
		$SYNC_{IL}$	●			0.3	V
	MODE/SYNC Input Current				1	2	µA
	Internal ITH Voltage Threshold		●	$INTV_{CC}$ – 0.3V			V
	V_{ON} Pin Input Impedance	LTC3646			520		kΩ
		LTC3646-1			600		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3646 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3646E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3646I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3646H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures derate operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Dynamic supply current is higher due to gate charging being delivered at the switch frequency.

Note 4: Limits to V_{OUT} are a subject to PVIN, SVIN, $t_{ON(MIN)}$, $t_{OFF(MIN)}$, and frequency constraints. See the Applications Information section for a further discussion. These items are tested with appropriate combinations of V_{IN}, V_{ON} and frequency.

Note 5: $R_{DS(ON)}$ is guaranteed by correlation to wafer level measurements.

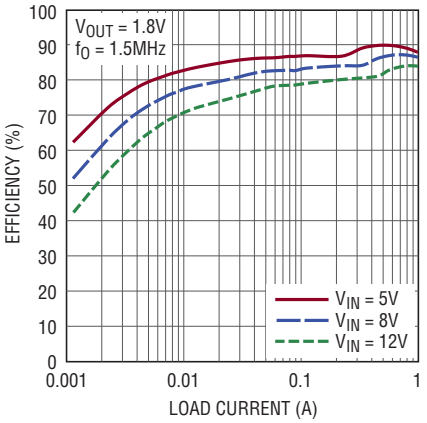
Note 6: Maximum allowed current draw when used as a regulated output is 5mA. This supply is only intended to provide additional DC load current as needed and not to regulate large transient or AC behavior as such waveforms may impact LTC3646 operation.

Note 7: This IC includes overtemperature protection intended to protect the device during momentary overload conditions. The maximum junction temperature may be exceeded when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

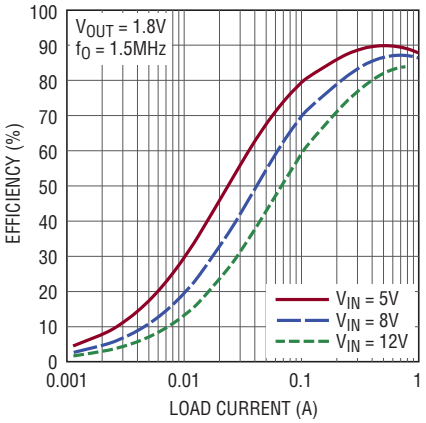
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, SVIN/PVIN = 12V, f_O = 1MHz unless otherwise noted.

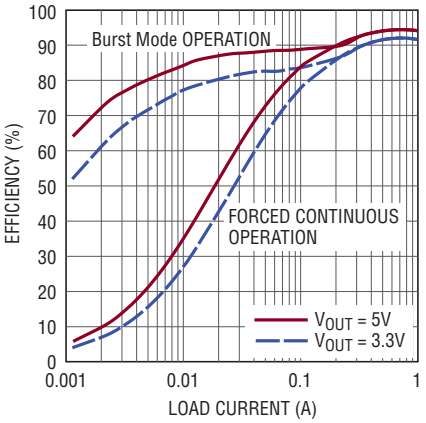
Efficiency vs Load Current, Burst Mode Operation



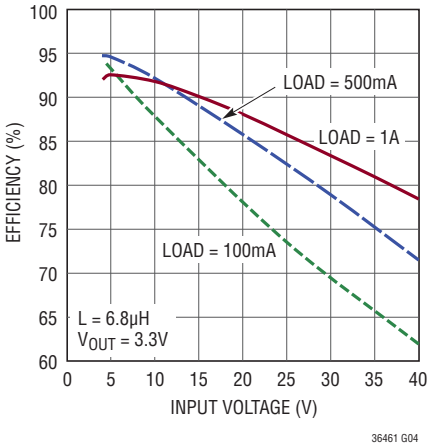
Efficiency vs Load Current, Forced Continuous Mode Operation



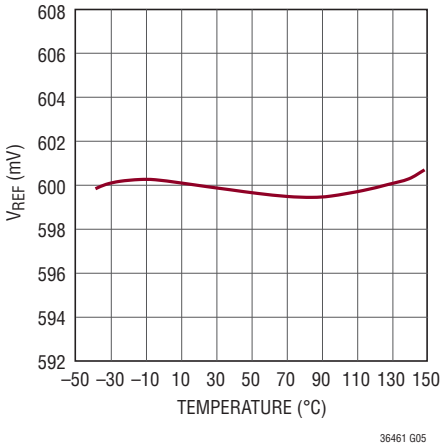
Efficiency vs Load Current



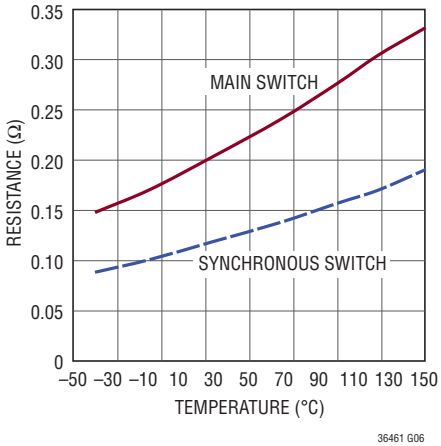
Efficiency vs Input Voltage, Burst Mode Operation



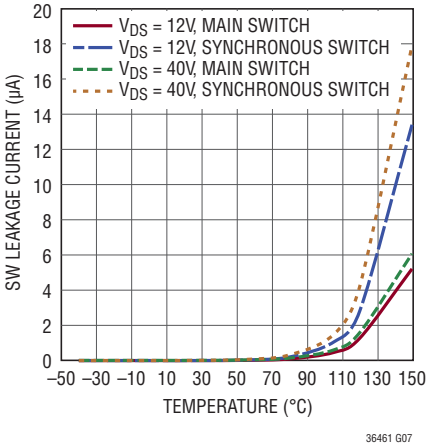
Reference Voltage vs Temperature



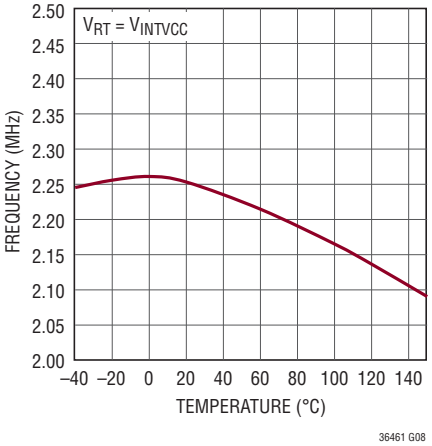
$R_{DS(ON)}$ vs Temperature



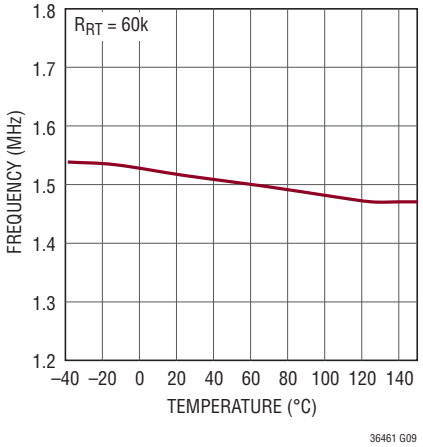
Switch Pin Leakage vs Temperature and Supply



Oscillator Internal Set Frequency vs Temperature



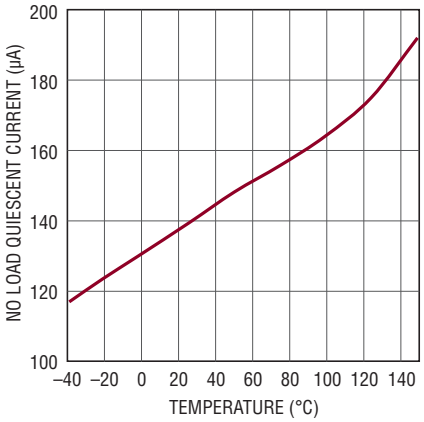
Oscillator Externally Set Frequency vs Temperature



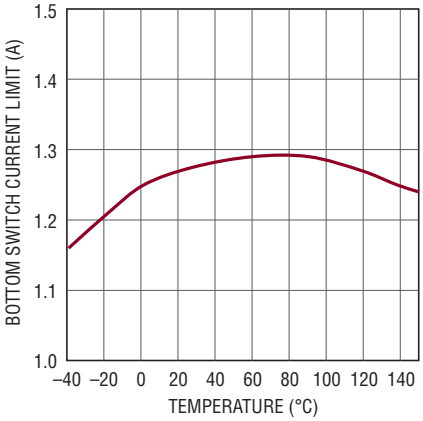
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, SVIN/PVIN = 12V, f_O = 1MHz unless otherwise noted.

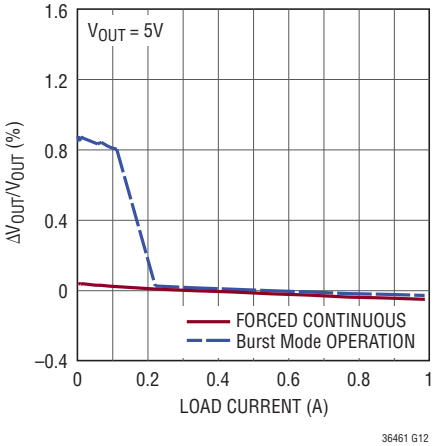
No Load Quiescent Current vs Temperature, Burst Mode Operation



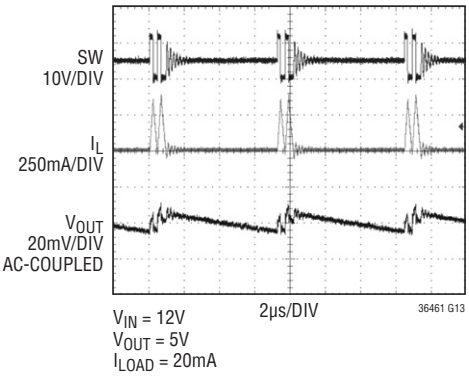
Bottom Switch Current Limit vs Temperature



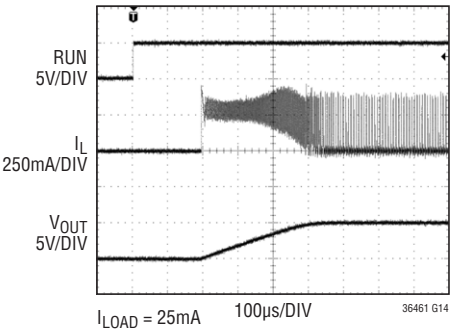
Load Regulation



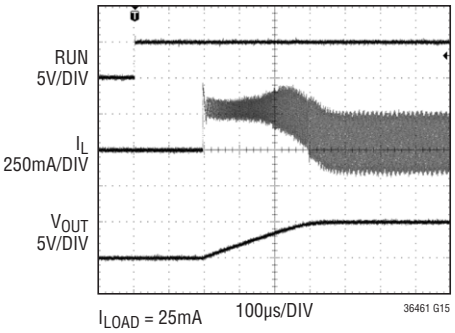
Output Voltage vs Time, Burst Mode Operation



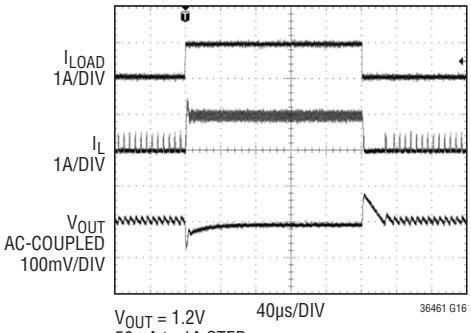
Start-Up from Shutdown, Burst Mode Operation



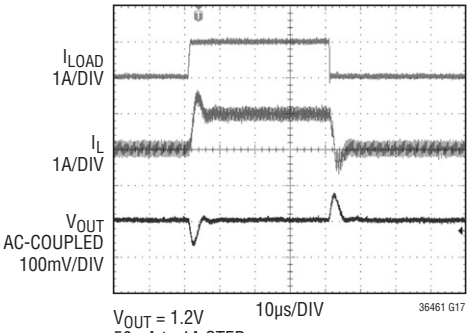
Start-Up from Shutdown, Forced Continuous Mode



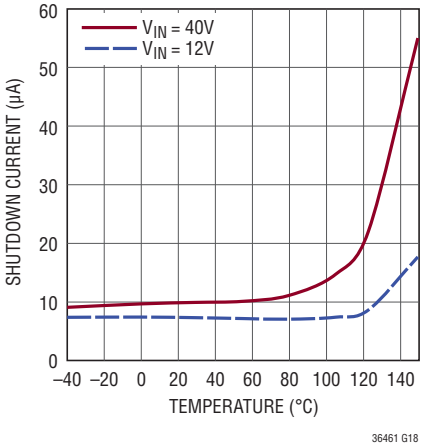
Load Step, Burst Mode Operation



Load Step, Forced Continuous Operation



I_Q Shutdown vs Supply and Temperature



PIN FUNCTIONS (DFN/MSOP)

SGND (Pin 1/Pin 1): Analog Ground Pin. This pin should have a low noise connection to the reference ground.

V_{FB} (Pin 2/Pin 2): Output Voltage Feedback Pin. Input to the error amplifier that compares the feedback voltage with the internal 0.6V reference. Connect this pin to a resistor divider network to program the desired output voltage.

ITH (Pin 3/Pin 3): Error Amplifier Output and Switching Regulator Compensation Point. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

RT (Pin 4/Pin 4): Oscillator Frequency Program Pin. Connect an external resistor between 450k and 30k from this pin to SGND to program the switching frequency from 200kHz to 3.0MHz. When RT is connected to $INTV_{CC}$, the switching frequency will be 2.25MHz. Do not float RT.

V_{ON} (Pin 5/Pin 5): On-Time Voltage Input Pin. This pin provides information about the output voltage (V_{OUT}) to the on-time control loop. Connect this pin to the regulated output to make the on-time proportional to the output voltage.

PGOOD (Pin 6/Pin 6): Power Good Output Pin. PGOOD is pulled to ground when the voltage at the V_{FB} pin is not within 7.5% (typical) of the internal 0.6V reference. PGOOD becomes high impedance once the voltage at the V_{FB} pin returns to within 5% of the internal reference.

MODE/SYNC (Pin 7/Pin 7): Mode Selection and External Clock Input Pin. This pin forces the LTC3646 into forced continuous operation when tied to ground, and high efficiency Burst Mode operation when tied to $INTV_{CC}$. When driven with an external clock, the LTC3646 will adjust the top switch on-time to match the switching frequency to the applied clock frequency and the part will operate in forced continuous mode. During start-up or external clock synchronization, the operating mode will be as described in the Applications Information section.

PVIN (Pin 8/Pins 9, 10): Supply Pin for the Power Switch. This pin connects directly to top switch. Closely decouple this pin to PGND with a 10µF or greater, low ESR capacitor.

SW (Pin 9/Pin 11): Switch Node Output Pin. Connect this pin to the switch side of the external inductor and boost capacitor.

BOOST (Pin 10/Pin 12): Boosted Supply Pin. A boosted voltage is generated at this pin by connecting a capacitor between this pin and the SW pin. The normal operation voltage swing of this pin ranges from $INTV_{CC}$ to PVIN + $INTV_{CC}$. When necessary, connect the cathode of an external boost diode to this pin. See the Boost Capacitor and Diode section.

$INTV_{CC}$ (Pin 11/Pin 13): Internal 5.0V Regulator Output Pin. This pin should be decoupled to PGND with a 4.7µF or greater low ESR capacitor. When necessary, connect the anode of an external boost diode to this pin. The internal regulator is disabled when the RUN pin is low.

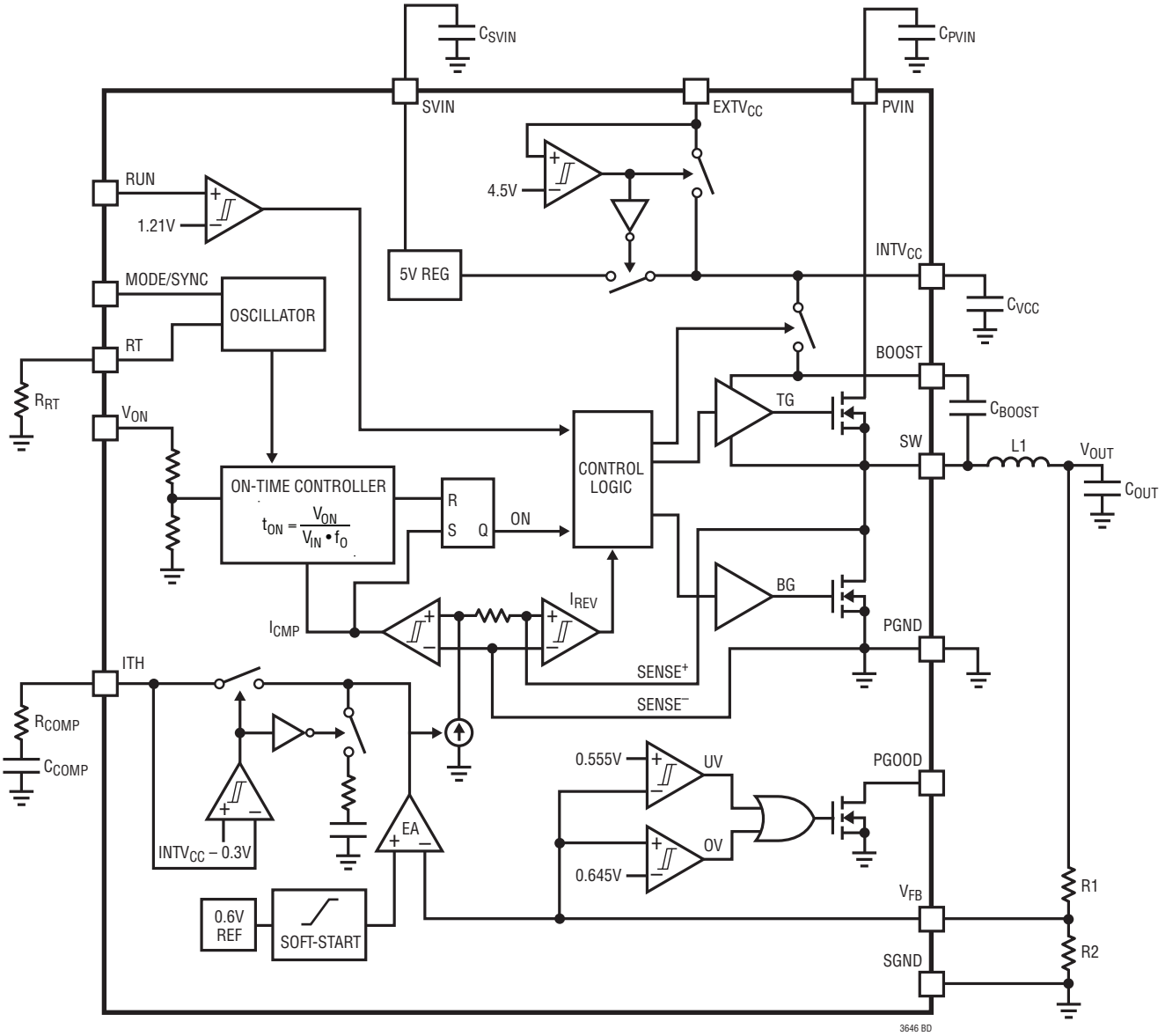
$EXTV_{CC}$ (Pin 12/Pin 14): Use this input pin to power the chip's low voltage control circuitry if a high efficiency supply between 4.5V and 6.0V is available. Otherwise, connect this pin to SGND. See the Applications Information section for further information.

RUN (Pin 13/Pin 15): Regulator Enable Pin. Enables chip operation by applying a voltage greater than V_{RUN}.

SVIN (Pin 14/Pin 16): Power Supply Input for Internal Circuitry. Closely decouple this pin to SGND with a greater than 1µF low ESR capacitor. SVIN pin voltage should equal PVIN in order to correctly calculate on the on time and maintain constant frequency operation.

PGND (Exposed Pad Pin 15/Exposed Pad Pin 17): Power Ground Pin. The exposed pad must be well soldered to the PCB ground to provide a low impedance electrical connection to ground and rated thermal performance.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The LTC3646 and LTC3646-1 are current mode, monolithic, synchronous, step-down regulators capable of 40V input operation, and extremely high step down ratios while maintaining constant frequency. (Both will be referred to as the LTC3646 except as specifically noted.) Part operation is enabled by raising the voltage of the RUN pin above 1.21V.

Main Control Loop

In normal operation a switching cycle is initiated by a signal from the inductor valley current comparator (I_{CMP} in the Block Diagram). The top power MOSFET is turned on, and a timer is simultaneously started in the on-time controller. The on-time controller computes the correct on time (subject to $t_{ON(MIN)}$) based on the desired switching frequency f_O, and step-down ratio V_{ON}/V_{IN}, according to the formula shown in the Block Diagram. In a typical application, the V_{ON} pin should be connected to the output voltage, V_{OUT}. When the timer expires, the top power MOSFET is turned off and the bottom power MOSFET is turned on until the current comparator (I_{CMP}) trips, restarting the timer and initiating the next cycle. The inductor current is monitored by sensing the voltage drop across the SW and PGND nodes of the bottom power MOSFET. The voltage at the ITH node sets the I_{CMP} comparator threshold corresponding to the inductor valley current. The error amplifier (EA) adjusts the ITH voltage by comparing an internal 0.6V reference voltage to the feedback signal, V_{FB}, derived from the output voltage. If, for example, the load current increases, the output voltage will decrease relative to the 0.6V reference. The ITH voltage will rise until the average inductor current increases to match the load current.

At low load currents, the inductor current can drop to zero or become negative. If the LTC3646 is configured for Burst Mode operation, this inductor current condition is detected by the current reversal comparator (I_{REV}) which then shuts off the bottom power MOSFET and places the part into a low quiescent current sleep state, resulting in discontinuous operation and increased efficiency at low load currents. Both power MOSFETs will remain off with the part in sleep and the output capacitor supplying the load current until the ITH voltage rises sufficiently to initiate another cycle. Discontinuous operation is disabled by tying the MODE/SYNC pin to ground, placing the LTC3646 into forced continuous mode. During forced continuous mode operation, synchronous operation occurs regardless of the output load current, and the inductor current trough levels are allowed to become negative.

The operating frequency is determined by the value of the R_{RT} resistor, which programs the current for the internal oscillator. An internal phase-locked loop adjusts the switching regulator on-time so that the switching frequency matches the programmed frequency, subject to t_{ON} and t_{OFF} time constraints shown in the Electrical Characteristics table. Alternatively, the RT pin can be connected to the $INTV_{CC}$ pin which causes the internal oscillator to run at the default frequency of 2.25MHz.

A clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external source. When operating in this configuration, connect a resistor to the RT pin with a value corresponding to the applied clock frequency. With an external clock supplied to the MODE/SYNC pin, the part will operate in forced continuous mode.

Power Good Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits the V_{PGOOD} window around the regulation point. This condition is released once regulation within the specified window is achieved. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3646 PGOOD falling edge includes a filter time of approximately 70 clock cycles.

OPERATION

SVIN/PVIN Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3646 continuously monitors the SVIN pin for an overvoltage condition. When SVIN rises above $V_{IN(OV)}$, the regulator suspends operation by shutting off both power MOSFETs and resetting the soft-start level. Once V_{IN} drops to below the specified range of $V_{IN(OV)}$, the regulator immediately restarts normal operation.

Short-Circuit Protection

The LTC3646 is designed to withstand output short circuits. In this situation the part will source I_{LIM} (approximately 1.2A) plus half the inductor current ripple. Since V_{OUT} is at or near 0V, the on-time will shorten and the off-time will lengthen considerably, resulting in a lower switching frequency.

APPLICATIONS INFORMATION

A general LTC3646 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and begins with the selection of the inductor L. Once the inductor is chosen, the input capacitor, C_{IN}, the output capacitor, C_{OUT}, the internal regulator capacitor, C_{VCC}, and the boost capacitor, C_{BOOST}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, externally programmed oscillator frequency and PGOOD.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The operating frequency, f_O, of the LTC3646 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{RT} = \frac{9E10}{f_O}$$

where R_{RT} is in Ω and f_O is in Hz.

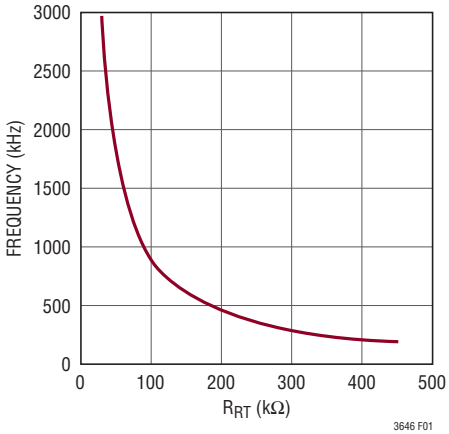


Figure 1

Connecting the RT pin to $INTV_{CC}$ will assert the internal default f_O = 2.25MHz; however, this switching frequency will be more sensitive to process and temperature variations than using a resistor on RT (see the Typical Performance Characteristics section).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_O \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_L = inductor ripple current (A), f_O = operating frequency (Hz) and L = inductor value (H). A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple. Generally, the highest efficiency operation is obtained at low operating frequency with small ripple current.

The inductor value should be chosen to give a peak-to-peak ripple current of between 30% and 40% of $I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ equals the maximum average output current. Note that the largest ripple current occurs at the highest V_{IN}. Further, the inductor ripple current must not be so large that the trough or valley reaches the negative valley current limit of –0.3A (typical) when operating in forced-continuous mode. If the inductor current trough reaches the negative current limit while the average inductor current is positive, V_{OUT} may exceed the target regulation voltage. To guarantee the ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f_O \bullet \Delta I_L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size

APPLICATIONS INFORMATION

for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire leading to increased copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate "hard," meaning the inductance collapses abruptly when the peak design current is exceeded. This collapse will result in an abrupt increase in inductor ripple current, so it is important to ensure the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroidal or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, Coilcraft, TDK and Wurth Electronik. Table 1 gives a sampling of available surface mount inductors.

Table 1. Inductor Selection

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Würth Elektronik, TPC MH, L, LH Series				
3.3 (MH)	35	1.8	4.8 × 4.8	2.8
3.9 (L)	55	2.1	5.8 × 5.8	1.8
6.2 (LH)	45	1.7	5.8 × 5.8	2.8
Sumida, CDRH3d23/HP Series				
1.2	40	3.5	3.92 × 3.92	2.5
3.3	70	2.2	3.92 × 3.92	2.5
TDK, SLF10145 Series				
22	59	2.1	10.1 × 10.1	4.5
33	82	1.6	10.1 × 10.1	4.5
Coilcraft MSS7341 Series				
10	32	1.64	7.3 × 7.3	4.1
15	47	1.36	7.3 × 7.3	4.1

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor or choose a capacitor rated at a higher temperature than required.

Several capacitors may be paralleled to meet the requirements of the design. For low input voltage applications sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3646 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is primarily determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \bullet f_O \bullet C_{OUT}} \right)$$

When using low-ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is

APPLICATIONS INFORMATION

usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3 \bullet \Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in small case sizes. Their high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors choose the X5R or X7R dielectric formulations. These dielectrics provide the best temperature and voltage characteristics for a given value and size.

$INTV_{CC}$ Regulator and $EXTV_{CC}$

An internal low dropout (LDO) regulator produces a 5V supply voltage used to power much of the internal LTC3646 circuitry including the power MOSFET gate drivers. The $INTV_{CC}$ pin connects to the output of this regulator and should have 4.7µF of decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the $INTV_{CC}$ and PGND pins to provide the transient currents required by the LTC3646. The user may draw a maximum load current of 5mA from this pin but must take into account the increased power dissipation and die temperature that results. Furthermore, this supply is intended only to supply additional DC load currents as desired; it is not intended to regulate large transient or AC behavior as this may impact LTC3646 operation.

Alternatively, if a suitable supply is available or can be generated, the power required to operate the low voltage circuitry of the LTC3646 can be supplied through the $EXTV_{CC}$ pin. When the voltage on the $EXTV_{CC}$ pin is below 4.5V, the chip power is supplied by the internal LDO. As shown in the Block Diagram, when $EXTV_{CC}$ is above 4.5V, the internal LDO is shut off, and an internal switch is closed between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Connect $EXTV_{CC}$ to SGND if an external supply meeting these constraints is not available.If the voltage on the $EXTV_{CC}$ pin is efficiently generated, this will result in the highest overall system efficiency and the least amount of heat generated by the LTC3646. This effectively decreased the no-load quiescent current by a factor of V_{OUT}/V_{IN}. This topic is further discussed in the Thermal Considerations section.

Boost Capacitor and Diode

The boost capacitor, C_{BOOST}, is used to create a voltage rail above the applied input voltage V_{IN}. Specifically, the boost capacitor is charged to a voltage equal to approximately $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V_{IN} + $INTV_{CC}$. For most applications a 0.1µF ceramic capacitor will provide adequate performance.

An internal switch is used to charge the boost capacitor when the synchronous MOSFET is turned on. An external Schottky diode can be connected between BOOST and $INTV_{CC}$ in parallel with this switch in order to improve the capacitor refresh. For best performance and sufficient design margin an external diode must be used in circuits where V_{OUT} is programmed to be above 12V or the IC operates at a die temperature above 85°C. Forward currents through this diode are small, on the order of 10mA to 20mA, but the diode chosen must have low reverse leakage current at the expected voltage and temperature.

APPLICATIONS INFORMATION

The design example on the back page uses a DFLS1200 based on its low reverse leakage over the voltage and temperature ratings of the LTC3646.

Output Voltage Programming

The LTC3646 will adjust the output voltage such that V_{FB} equals the reference voltage of 0.6V according to:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

The desired output voltage is set by the appropriate selection of resistors R1 and R2 as shown in Figure 2. Choosing large values for R1 and R2 will result in improved efficiency but may lead to undesired noise coupling or phase margin reduction due to stray capacitance at the V_{FB} node. Care should be taken to route the FB line away from any noise source, such as the SW line.

When programming output voltages above 12V, a Schottky diode connected between BOOST and $INTV_{CC}$ is needed (see the Boost Capacitor and Diode section.)

To improve the frequency response of the main control loop a feedforward capacitor, C_F, may be used as shown in Figure 2.

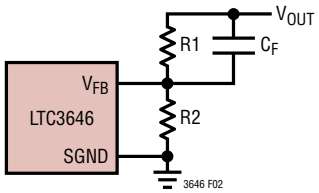


Figure 2. Optional Feedforward Capacitor

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3646 can turn on the bottom power MOSFET, trip the current comparator and turn off the power MOSFET. This time is typically 80ns. For the controlled on-time current mode control architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{(MAX)} = 1 - (f_O \bullet t_{OFF(MIN)})$$

where f_O is the switching frequency and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1-\left(f_O \bullet t_{OFF(MIN)}\right)}$$

If there is concern about operating near the minimum off-time limits, consider reducing the frequency to add margin to the design.

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its “on” state. This time is typically 30ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{(MIN)} = (f_O \bullet t_{ON(MIN)})$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in some cases, and high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor and Capacitor Selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

APPLICATIONS INFORMATION

Minimum on-time can be affected by the output load current and the trough current level. During the transition between the top switch turn-off and the synchronous switch turn-on, the inductor current discharges the SW pin capacitance. When the inductor trough current level is low, or reversing in forced continuous operation, the minimum on-time can increase by approximately 20nS.

Output Voltage Limits

The Block Diagram shows that a sample of the output voltage (taken through the V_{ON} pin) is used to servo the correct on-time for a given application duty cycle and frequency. This circuit limits the range of V_{OUT} over which the LTC3646 will be able to adjust the on-time in order to match the selected frequency at a given duty cycle. The valid output range for the LTC3646 is 2.0V to 30V. For output voltage below 2.0V, use the LTC3646-1 which has a valid output range of between 0.6V and 15V.

It is important to note that the LTC3646 will maintain output voltage regulation if these limits are exceeded, but the $t_{ON(MIN)}$ limit may be reached resulting in the part switching at a frequency lower than the programmed switching frequency.

Choosing Compensation Components

Loop compensation is a complicated subject and Application Note 76 is recommended reading for a full discussion on maximizing loop bandwidth in a current mode switching regulator. This section will provide a quick method on choosing proper components to compensate the LTC3646 regulators.

Figure 3 shows the recommended components to be connected to the ITH pin, and Figure 4 shows an approximate bode plot of the buck regulator loop using these components. It is assumed that the major poles in the system (the output capacitor pole and the error amplifier output pole) are located at a frequency lower than the crossover frequency.

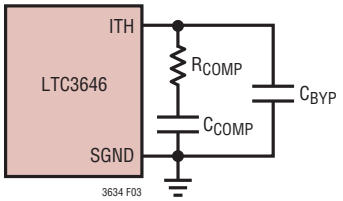


Figure 3. Compensation and Filtering Components

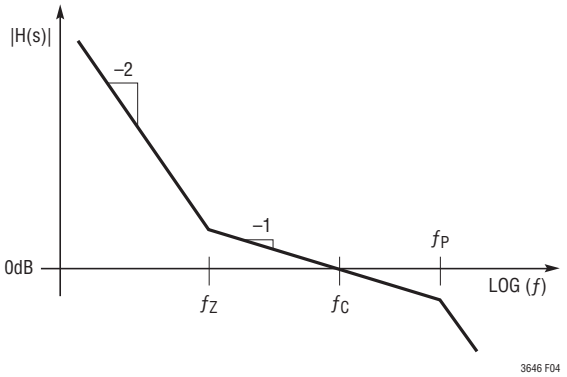


Figure 4. Bode Plot of Regulator Loop

The first step is to choose the crossover frequency f_C. Higher crossover frequencies will result in a faster loop transient response; however, in order to avoid higher order loop dynamics from the switching power stage, it is recommended that f_C not exceed one-tenth the switching frequency (f_O).

Once f_C is chosen, the value of R_{COMP} that sets this crossover frequency can be calculated by the following equation:

$$R_{COMP} = \left(\frac{2\pi \bullet f_C \bullet C_{OUT}}{g_{m(EA)} \bullet g_{m(MOD)}}\right)\left(\frac{V_{OUT}}{V_{FB}}\right)$$

where $g_{m(EA)}$ is the error amplifier transconductance (see the Electrical Characteristics section), and $g_{m(MOD)}$ is the modulator transconductance (the transfer function from ITH voltage to current comparator threshold). For the LTC3646, this transconductance is nominally $1\Omega^{-1}$ at room temperature.

APPLICATIONS INFORMATION

Once R_{COMP} is determined, C_{COMP} can be chosen to set the zero frequency (f_Z):

$$f_Z = \frac{1}{2\pi \bullet C_{COMP} \bullet R_{COMP}}$$

For maximum phase margin, f_Z should be chosen to be less than one-tenth of f_C.

Since the ITH node is sensitive to noise coupling, a small bypass capacitor (C_{BYP}) may be used to filter out board noise. However, this cap contributes a pole at f_P and may introduce some phase loss at the crossover frequency:

$$f_P = \frac{1}{2\pi \bullet C_{BYP} \bullet R_{COMP}}$$

For best results, f_P should be set high enough such that phase margin is not significantly affected.

If necessary, a capacitor C_F (as shown in Figure 2) may be used to add some phase lead.

Though better load transient response can generally be achieved with external compensation, at switching frequencies above 1MHz, component count can be reduced by connecting the ITH pin to $INTV_{CC}$ enabling internal compensation. When using internal compensation, a reasonable starting point for the minimum amount of output capacitance necessary for stability can be found as the greater of 15µF or C_{OUT} defined by the equation:

$$C_{OUT} > 3 \bullet 10^{-5}/V_{OUT}$$

Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling behavior at this test point reflect the system's closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated by observing the percentage of overshoot seen at this pin. Use a high impedance, low capacitance probe (>50MΩ, <5pF). The ITH external components shown in Figure 3 will provide an adequate starting point for most applications. The series R-C filter sets the pole-zero loop compensation. The values can be modified from their suggested values once the final PC layout is done, and the particular switching frequency, output capacitor type and value have been chosen. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current with a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop. As a result, the standard second order overshoot/DC ratio cannot be used to estimate phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76. As shown in Figure 2 a feed-forward capacitor, C_F, may be added across feedback resistor R1 to improve the high frequency response of the system. Capacitor C_F provides phase lead by creating a high frequency zero with R1.

In some applications severe transients can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this output droop if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection and soft-start functions.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Connecting this pin to $INTV_{CC}$ enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is pulled to ground, forced continuous mode

APPLICATIONS INFORMATION

operation is selected creating the lowest fixed output ripple at the expense of light load efficiency.

The LTC3646 will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place the LTC3646 into forced continuous mode operation. For proper on-time, connect a resistor corresponding to the SYNC frequency between the RT pin and SGND (see the Operating Frequency section). The user should be aware that a clock with fast edges may drive this pin below the –0.3V rating of this pin and an R-C filter may be needed to prevent this condition.

Soft-Start

Soft-start on the LTC3646 is implemented by internally ramping the reference signal fed to the error amplifier over approximately a 250µs period. Figure 5 shows the behavior of the regulator during start-up.

During the soft-start period, the inductor current is not allowed to reverse and discontinuous operation may occur under light load conditions.

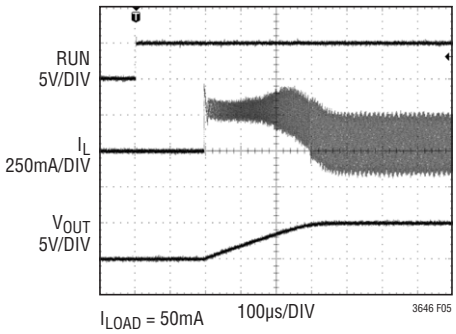


Figure 5. Start-Up Waveform

Output Power Good

The PGOOD output of the LTC3646 is driven by a 63Ω (typical) open-drain pull-down device. This pin will become high impedance once the output voltage is within 5% (see V_{PGOOD} thresholds) of the target regulation point allowing the voltage at PGOOD to rise via an external pull-up resistor (100k typical). If the output voltage exits a 7.5% (see V_{PGOOD} thresholds) regulation window around the target regulation point the open-drain output will pull down with 63Ω output resistance to ground, thus dropping the PGOOD pin voltage. A filter time of 30µs (typical at f_O = 2.25MHz) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. This filter time varies as a function of programmed switching period. The output voltage must exit the 7.5% regulation window for approximately 70 switching cycles before the PGOOD pin pulls to ground (see Figure 6).

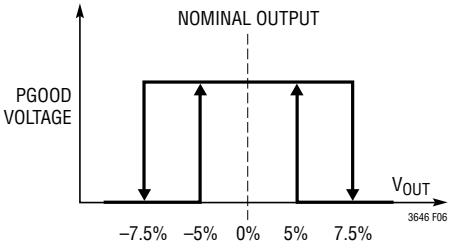


Figure 6. PGOOD Pin Behavior

APPLICATIONS INFORMATION

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources account for the majority of the losses in the LTC3646: 1) I^2R loss, 2) switching losses and quiescent current loss, 3) transition losses and other system losses.

1. I^2R loss is calculated from the DC resistance of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current will flow through inductor L but is chopped between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET's $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the curves in the Typical Performance Characteristics section. Thus to obtain I^2R loss:

   $$I^2R \text{ Loss} = I_{OUT}^2 \bullet (R_{SW} + R_L)$$

2. The internal LDO supplies the power to the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

   Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f_O is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on the LTC3646 is approximately 5nC. To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by V_{IN}:

   $$P_{LDO} = (I_{GATECHG} + I_Q) \bullet SVIN$$

   As will be discussed below, in certain cases the overall efficiency can be improved by supplying the gate and quiescent current through the $EXTV_{CC}$ pin.

3. Other hidden losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. Other losses, including diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

Transition loss can become significant at high V_{IN} or high switching frequencies. Transition loss for the LTC3646 can be approximated by the following formula:

$$\text{Loss (Watts)} = I_{OUT} \bullet V_{IN}^2 \bullet f_O \bullet 10^{-10}$$

APPLICATIONS INFORMATION

Thermal Considerations

The LTC3646 requires the exposed package backplane metal (PGND) to be well soldered to the PC board to provide good thermal contact. This gives the DFN and MSOP packages exceptional thermal properties, compared to other packages of similar size, making it difficult in normal operation to exceed the maximum junction temperature of the part. In many applications, the LTC3646 does not generate much heat due to its high efficiency. However, in applications in which the LTC3646 is running at a high ambient temperature, high input voltage, high switching frequency, and maximum output current, the heat dissipated may cause the part to exceed the maximum allowed junction temperature. If the junction temperature reaches approximately 175°C, both power switches will be turned off until temperature decreases approximately 10°C.

Thermal analysis should always be performed by the user to ensure the LTC3646 does not exceed the maximum junction temperature.

The temperature rise is given by:

$$t_{RISE} = P_D\,\theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient. Consider the example in which an LTC3646IDE-1 is operating with I_{OUT} = 1.0A, SVIN = 12V, f = 3MHz, V_{OUT} = 1.8V, and a board temperature of 85°C. From the Typical Performance Characteristics section, the $R_{DS(ON)}$ of the top switch is found to be nominally 200mΩ while that of the bottom switch is nominally 120mΩ yielding an equivalent power MOSFET resistance R_{SW} of:

$$\frac{R_{DS(ON)TOP} \bullet 1.8}{12} + \frac{R_{DS(ON)BOT} \bullet 10.2}{12} = 132\text{m}\Omega$$

From the previous section, $I_{GATECHG} + I_Q$ is ~15mA when f = 3MHz. Therefore, the total power dissipation due to resistive losses and LDO losses is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + \text{SVIN} \bullet (I_{GATECHG} + I_Q)$$

$$P_D = (1.0)^2 \bullet (0.132) + 12\text{V} \bullet 15\text{mA} = 312\text{mW}$$

and the transition loss is:

$$P_T = 1.0 \bullet 12^2 \bullet 10^{-10} \bullet 3.0 \bullet 10^6 = 43\text{mW}$$

The DFN 4mm × 3mm package junction-to-ambient thermal resistance, θ_{JA}, is approximately 43°C/W. Therefore, the junction temperature of the regulator operating in a 85°C ambient temperature is approximately:

$$T_J = (0.312 + 0.043) \bullet 43 + 85 = 100°\text{C}$$

which is below the specified maximum junction temperature of 125°C.

High input voltage, high frequency applications may cause the internal LDO to generate significant heat. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the SVIN LDO or through the $EXTV_{CC}$ pin. When the voltage on the $EXTV_{CC}$ pin is less than 4.5V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to SVIN • I_{INTVCC}. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. For example, the LTC3646 $INTV_{CC}$ current is approximately 15mA at 3MHz operation. If V_{IN} is at the 40V maximum, the loss in the on-chip LDO is:

$$40\text{V} \bullet 0.015\text{A} = 0.60\text{W}$$

In these situations it will be advantageous to bias the part through the $EXTV_{CC}$ pin if a suitable voltage source is available. When the voltage applied to $EXTV_{CC}$ rises above 4.5V (maximum 6.0V), the SVIN LDO is turned off and an internal switch between the $EXTV_{CC}$ and $INTV_{CC}$ pins is closed. This voltage is unregulated and so in this situation, $INTV_{CC} = EXTV_{CC}$.

Using $EXTV_{CC}$ allows the control power to be derived from the output if the output voltage is between 4.5V and 6.0V during normal operation and from the SVIN LDO when the output is out of regulation (e.g., start-up, short-circuit). Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the power needed for the driver and control currents will be supplied from the buck converter instead of the internal linear regulator.

For 4.5V to 6V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to a 5.5V supply reduces the dissipated power in the previous example from 0.60W to approximately:

$$5.5\text{V} \bullet 0.015\text{A} = 82.5\text{mW}$$

APPLICATIONS INFORMATION

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.0V regulator.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 4.5V to 6V regulated output and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 4.5V to 6V range, it may be used to power $EXTV_{CC}$. Ensure that $EXTV_{CC} < V_{IN}$.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3646.

1. Does the capacitor C_{PVIN} connect to PVIN and PGND as close to the pins as possible? These capacitors provide the AC current to the internal power MOSFETs and drivers. The (–) plate of C_{PVIN} should be closely connected to PGND and the (–) plate of C_{OUT}.
2. The output capacitor, C_{OUT}, and inductor L1 should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to PGND and the (–) plate of C_{IN}.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal, V_{FB}, should be routed away from noisy components and traces such as the SW line, and its trace length should be minimized. In addition, RT and the loop compensation components should be terminated to SGND.
4. Keep sensitive components away from the SW pin. The R_{RT} resistor, the feedback resistors, the compensation components, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor.
5. A ground plane is preferred, but if not available the signal and power grounds should be segregated with both connecting to a common, low noise reference point. The point at which the ground terminals of the V_{IN} and V_{OUT} bypass capacitors are connected makes a good, low noise reference point. The connection to the PGND pin should be made with a minimal resistance trace from the reference point.
6. Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside connection of the IC.

APPLICATIONS INFORMATION

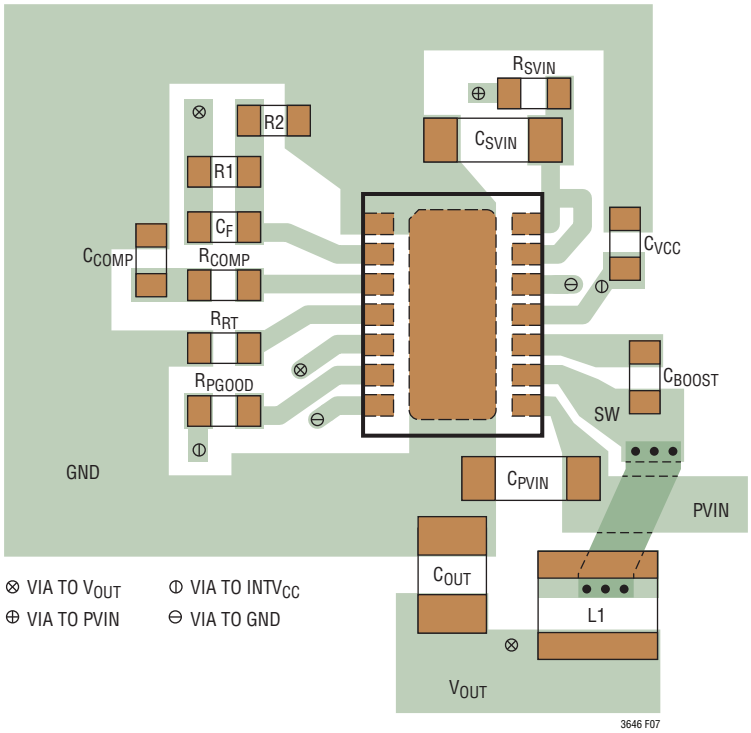


Figure 7. Example of Power Component Layout for DFN Package. Because of the Similar Pinout, MSE Package Layout is Similar

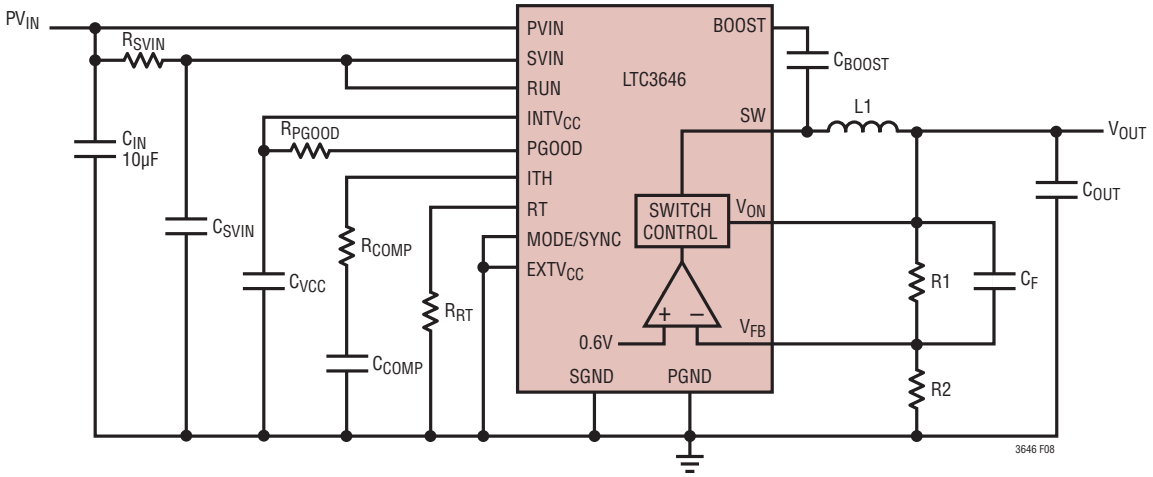


Figure 8. Board Layout Schematic

APPLICATIONS INFORMATION

Design Example

As a design example, consider using the LTC3646-1 in an application with the following specifications: V_{IN} = 12V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 1A, $I_{OUT(MIN)}$ = 10mA.

Because efficiency is important at both high and low load currents, Burst Mode operation and 1MHz operation is chosen.

First the correct R_{RT} resistor value for 1MHz switching frequency must be chosen. Based on the equation discussed previously, the closest standard resistor value for R_{RT} is 90.9k.

Next, determine the inductor value for approximately 35% ripple current using:

$$L = \left(\frac{1.8V}{1MHz \bullet 350mA}\right)\left(1 - \frac{1.8V}{12V}\right) = 4.37\mu H$$

A standard 4.7µH inductor would work well for this application.

Next C_{OUT} is selected based on the required output transient performance and the required ESR to satisfy the output voltage ripple. Using a 15µF ceramic capacitor with an ESR of 5mΩ will result in approximately 5mV of ripple.

Decoupling the PVIN pin with a 22µF capacitor and the SVIN pin with a 1µF capacitor should be adequate for most applications. A 0.1µF boost capacitor should also work for most applications.

To save board space the ITH pin is connected to $INTV_{CC}$ to select internal compensation. Since the switching and Q current drawn from the 12V supply is not a significant source of loss or heat, $EXTV_{CC}$ is disabled by tying the pin to SGND.

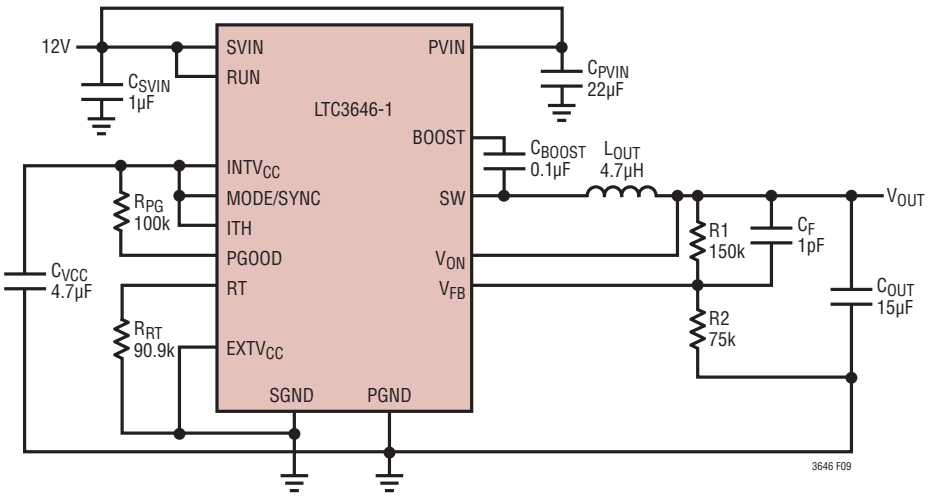
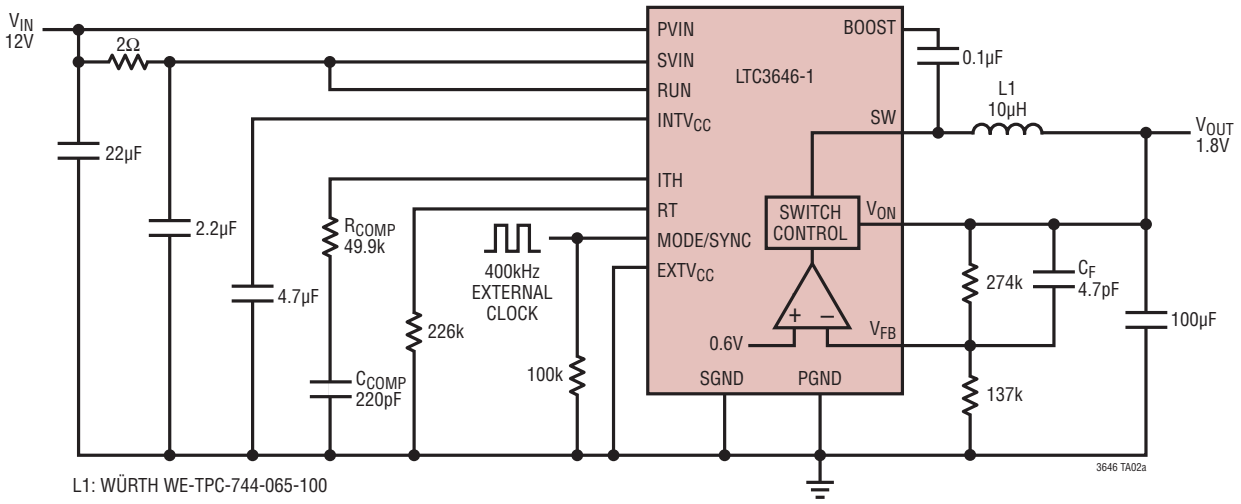


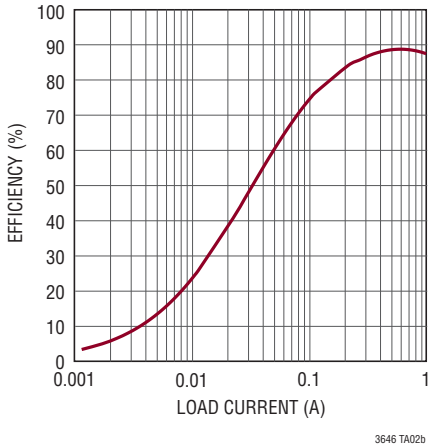
Figure 9

TYPICAL APPLICATIONS

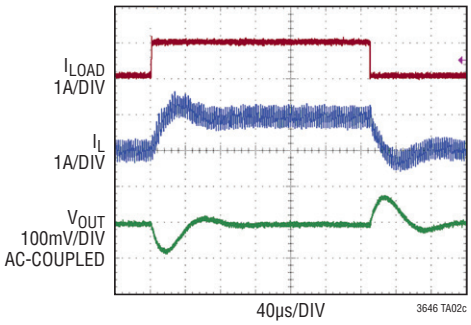
12V to 1.8V Output with 400kHz External Sync



Efficiency Curve

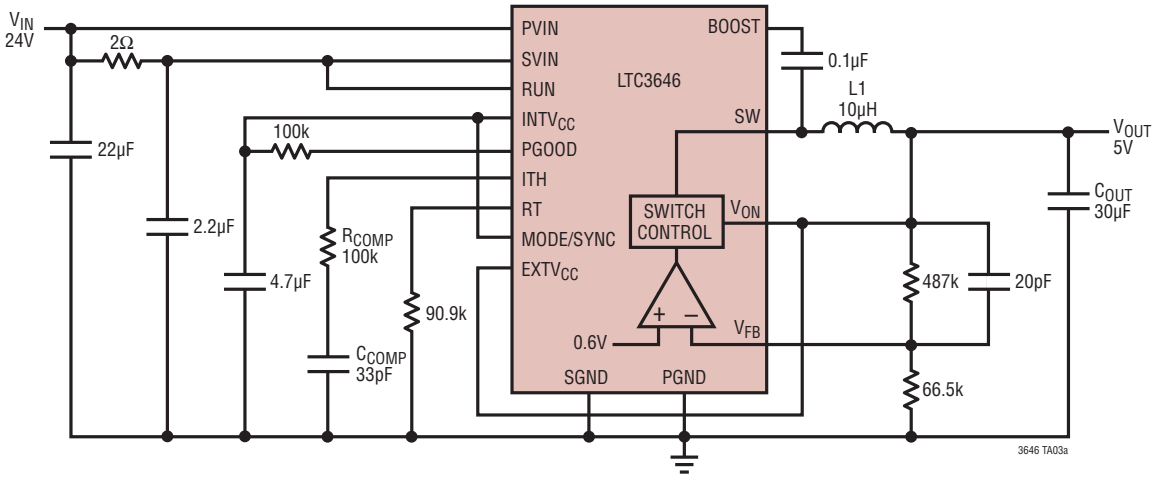


50mA to 1A Load Step

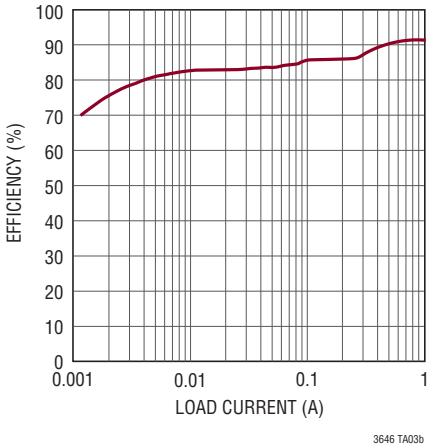


TYPICAL APPLICATIONS

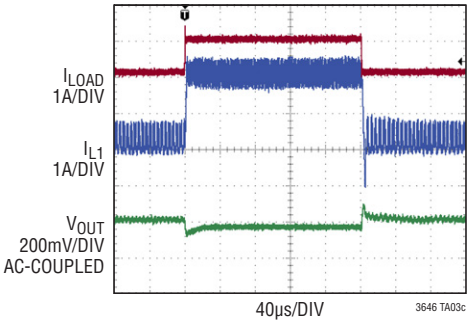
24V Input to 5V Output at 1MHz Frequency and $EXTV_{CC}$



Efficiency Curve



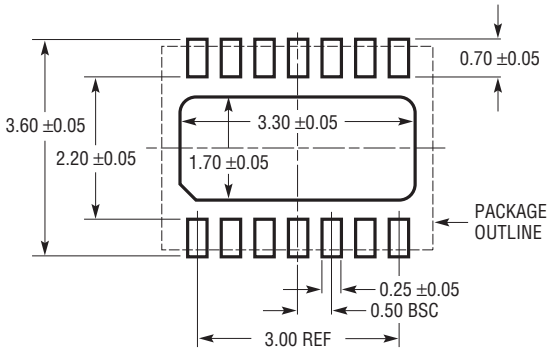
50mA to 1A Load Step



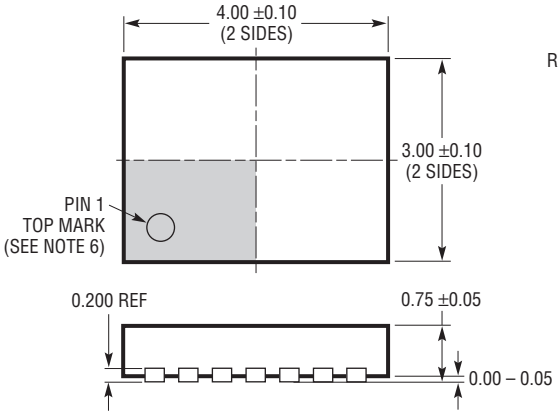
PACKAGE DESCRIPTION

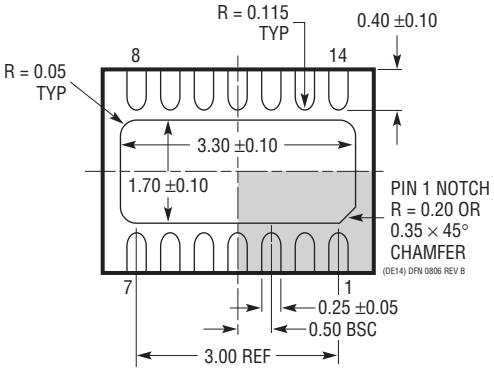
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





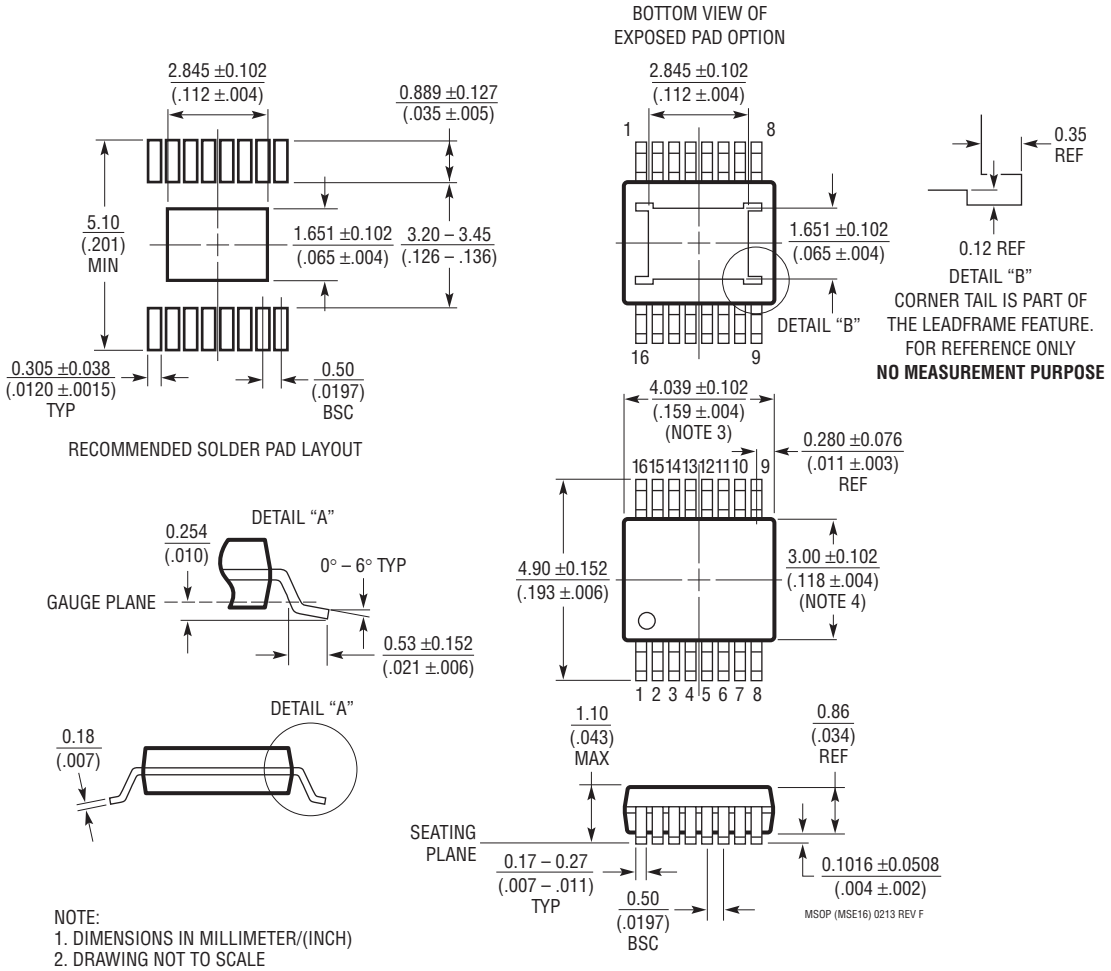
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

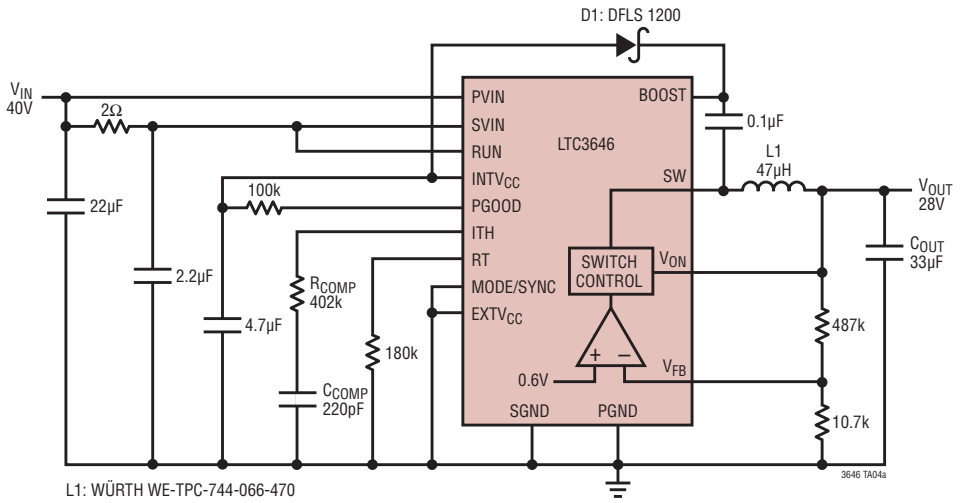
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/13	Changed '%' to '%/V' regarding V_{REF} Line Regulation in the Electrical Characteristics Table.	3
B	03/14	Clarified Description	1
		Clarified Operating Junction Temperature	2, 3, 4
		Clarified specifications	3
		Clarified graph	5
		Clarified formula	11
		Clarified description	19
		Clarified Application drawings	22, 28
C	08/15	Clarified Valley Switch Current Limit	3
		Clarified Inductor Selection paragraph	11
		Clarified Related Parts list	28

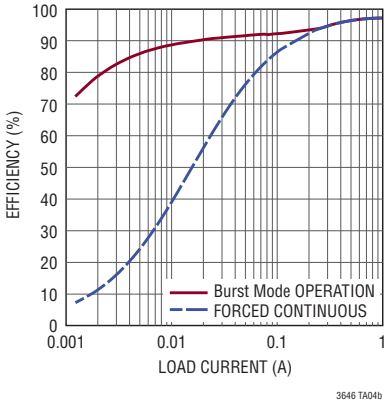
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

28V Output at 500kHz Operating Frequency



Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	V_{IN} MIN (V)	V_{IN} MAX (V)	V_{OUT} MIN (V)	I_Q	ISD	PACKAGE
LT8609	42V, 2A, 95% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	3	42	0.8	2.5µA	<1µA	MSOP-10E
LTC3642	45V Input Capable with 60V Transient Protection, 50mA, Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 12µA	4.5	45, 60 Transient	0.8	12µA	<1µA	3 × 3 DFN-8, MSOP-8E
LTC3631	45V Input Capable with 60V Transient Protection, 100mA, Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 12µA	4.5	45, 60 Transient	0.8	12µA	<1µA	3 × 3 DFN-8, MSOP-8E
LTC3632	50V Input Capable with 60V Transient Protection, 20mA, Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 12µA	4.5	45, 60 Transient	0.8	12µA	<1µA	3 × 3 DFN-8, MSOP-8E
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	3.4	42	0.97	2.5µA	<1µA	MSOP-16E
LT8610A/AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	3.4	42	0.97	2.5µA	<1µA	MSOP-16E
LT8610AC-1	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	3	42	0.8	2.5µA	<1µA	MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	3.4	42	0.97	2.5µA	<1µA	3 × 5 QFN-24
LT8620	65V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	3.4	65	0.97	2.5µA	<1µA	MSOP-16E 3 × 5 QFN-24
LT3991	55V, 1.2A, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with I_Q = 2.8µA	4.3	38	1.2	2.8µA	<1µA	3 × 3 DFN-10, MSOP-10E
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	3.6	58, Transient to 80	0.78	85µA	<1µA	3 × 4 DFN-16, MSOP-16E

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0815 REV C • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2012