10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver

FEATURES

- **10GHz Gain-Bandwidth Product**
- **88dB SFDR at 100MHz, $2V_{P-P}$**
- **1.1nV/√Hz Input Noise Density**
- Input Range Includes Ground
- External Resistors Set Gain (Min 1V/V)
- 3300V/µs Differential Slew Rate
- 52mA Supply Current
- 2.7V to 5.25V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- Low Power Shutdown
- Small 10-Lead 3mm × 2mm × 0.75mm QFN Package

APPLICATIONS

- Differential Pipeline ADC Driver
- High-Speed Data-Acquisition Cards
- Automated Test Equipment
- Time Domain Reflexometry
- Communications Receivers

DESCRIPTION

The LTC®6409 is a very high speed, low distortion, differential amplifier. Its input common mode range includes ground, so that a ground-referenced input signal can be DC-coupled, level-shifted, and converted to drive an ADC differentially.

The gain and feedback resistors are external, so that the exact gain and frequency response can be tailored to each application. For example, the amplifier could be externally compensated in a no-overshoot configuration, which is desired in certain time-domain applications.

The LTC6409 is stable in a differential gain of 1. This allows for a low output noise in applications where gain is not desired. It draws 52mA of supply current and has a hardware shutdown feature which reduces current consumption to 100µA.

The LTC6409 is available in a compact 3mm × 2mm 10-pin leadless QFN package and operates over a –40°C to 125°C temperature range.

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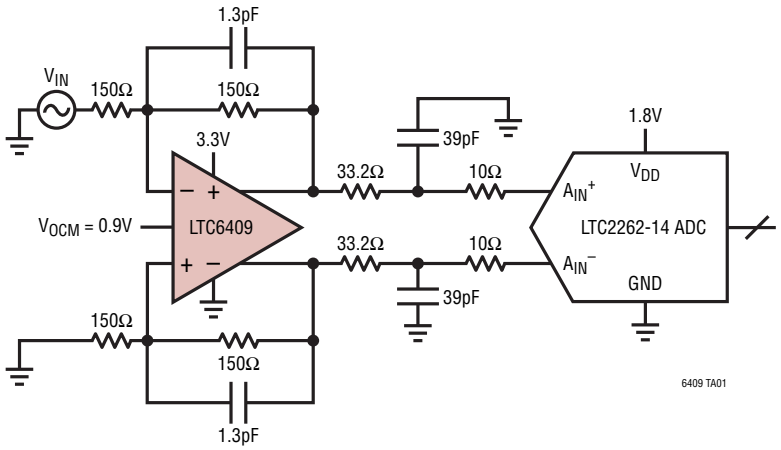
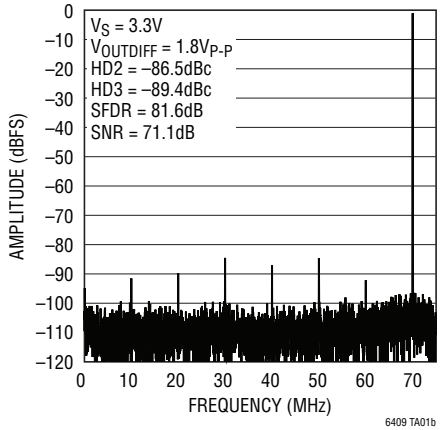
TYPICAL APPLICATION

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2262-14 ADC



LTC6409 Driving LTC2262-14 ADC, f_{IN} = 70MHz, –1dBFS, f_S = 150MHz, 4096-Point FFT

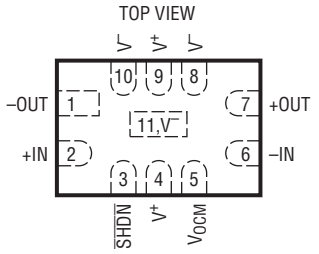


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ($V^+ – V^–$) 5.5V
Input Current (+IN, –IN, V_{OCM}, $\overline{SHDN}$)
(Note 2).....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range
(Note 4).....–40°C to 125°C
Specified Temperature Range
(Note 5).....–40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 138°C/W, θ_{JC} = 5.2°C/W
EXPOSED PAD (PIN 11) CONNECTED TO $V^–$

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6409CUDB#TRMPBF	LTC6409CUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	0°C to 70°C
LTC6409IUDB#TRMPBF	LTC6409IUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	–40°C to 85°C
LTC6409HUDB#TRMPBF	LTC6409HUDB#TRPBF	LFPF	10-Lead (3mm × 2mm) Plastic QFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, $V^–$ = 0V, $V_{CM} = V_{OCM} = V_{ICM}$ = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^–$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 3V V_S = 3V V_S = 5V V_S = 5V	 ● ●		±300 ±300 	±1000 ±1200 ±1100 ±1400	µV µV µV µV
$\frac{\Delta V_{OSDIFF}}{\Delta T}$	Differential Offset Voltage Drift (Input Referred)	V_S = 3V V_S = 5V	● ●		2 2		µV/°C µV/°C
I_B	Input Bias Current (Note 6)	V_S = 3V V_S = 5V	● ●	–140 –160	–62 –70	0 0	µA µA
I_{OS}	Input Offset Current (Note 6)	V_S = 3V V_S = 5V	● ●		±2 ±2	±10 ±10	µA µA
R_{IN}	Input Resistance	Common Mode Differential Mode			165 860		kΩ Ω
C_{IN}	Input Capacitance	Differential Mode			0.5		pF
e_n	Differential Input Noise Voltage Density	f = 1MHz, Not Including R_I/R_F Noise			1.1		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1MHz, Not Including R_I/R_F Noise			8.8		$pA/\sqrt{Hz}$
NF	Noise Figure at 100MHz	Shunt-Terminated to 50Ω, R_S = 50Ω, R_I = 25Ω, R_F = 10kΩ			6.9		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
e_{nVOCM}	Common Mode Noise Voltage Density	f = 10MHz			12		nV/√Hz
V_{ICMR} (Note 7)	Input Signal Common Mode Range	V_S = 3V V_S = 5V	● ●	0 0		1.5 3.5	V V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{ICM} from 0V to 1.5V V_S = 5V, V_{ICM} from 0V to 3.5V	● ●	75 75	90 90		dB dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●	55 60	80 85		dB dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.7V to 5.25V	●	60	85		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.7V to 5.25V	●	55	70		dB
V_S	Supply Voltage Range (Note 10)		●	2.7		5.25	V
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●		1 1		V/V V/V
ΔG_{CM}	Common Mode Gain Error, 100 × (G_{CM} – 1)	V_S = 3V, V_{OCM} from 0.5V to 1.5V V_S = 5V, V_{OCM} from 0.5V to 3.5V	● ●		±0.1 ±0.1	±0.3 ±0.3	% %
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●		 –65 –70	 –50 –50	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} - V_{OCM}$)	V_S = 3V V_S = 5V	● ●		±1 ±1	±5 ±6	mV mV
$\frac{\Delta V_{OSCM}}{\Delta T}$	Common Mode Offset Voltage Drift		●		4		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V V_S = 5V	● ●	0.5 0.5		1.5 3.5	V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	30	40	50	KΩ
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_S = 3V, V_{OCM} = Open V_S = 5V, V_{OCM} = Open	 ●	 0.9	0.85 1.25	 1.6	V V
V_{OUT}	Output Voltage, High, Either Output Pin	V_S = 3V, I_L = 0 V_S = 3V, I_L = –20mA V_S = 5V, I_L = 0 V_S = 5V, I_L = –20mA	● ● ● ●	1.85 1.8 3.85 3.8	2 1.95 4 3.95		V V V V
	Output Voltage, Low, Either Output Pin	V_S = 3V, 5V; I_L = 0 V_S = 3V, 5V; I_L = 20mA	● ●		0.06 0.2	0.15 0.4	V V
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 3V V_S = 5V	● ●	±50 ±70	±70 ±95		mA mA
A_{VOL}	Large-Signal Open Loop Voltage Gain				65		dB
I_S	Supply Current		 ●		52	56 58	mA mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	$V_{\overline{SHDN}} \le 0.6V$	●		100	500	µA
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	$V_{\overline{SHDN}}$ = 0V to 0.5V	●	115	150	185	KΩ
V_{IL}	$\overline{SHDN}$ Input Logic Low		●			0.6	V
V_{IH}	$\overline{SHDN}$ Input Logic High		●	1.4			V
t_{ON}	Turn-On Time				160		ns
t_{OFF}	Turn-Off Time				80		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 1.25V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	Differential Output, $V_{OUTDIFF}$ = $4V_{P-P}$ +OUT Rising (–OUT Falling) +OUT Falling (–OUT Rising)			3300 1720 1580		V/µs V/µs V/µs
GBW	Gain-Bandwidth Product	R_I = 25Ω, R_F = 10kΩ, f_{TEST} = 100MHz	 ●	9.5 8	10		GHz GHz
f_{-3dB}	–3dB Frequency	R_I = R_F = 150Ω, R_{LOAD} = 400Ω, C_F = 1.3pF			2		GHz
$f_{0.1dB}$	Frequency for 0.1dB Flatness	R_I = R_F = 150Ω, R_{LOAD} = 400Ω , C_F = 1.3pF			600		MHz
FPBW	Full Power Bandwidth	$V_{OUTDIFF}$ = $2V_{P-P}$			550		MHz
HD2 HD3	25MHz Distortion	Differential Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –104 –106		 dBc dBc
	100MHz Distortion	Differential Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –93 –88		 dBc dBc
HD2 HD3	25MHz Distortion	Single-Ended Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –101 –103		 dBc dBc
	100MHz Distortion	Single-Ended Input, $V_{OUTDIFF}$ = $2V_{P-P}$, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 2nd Harmonic 3rd Harmonic			 –88 –93		 dBc dBc
IMD3	3rd Order IMD at 25MHz f1 = 24.9MHz, f2 = 25.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–110		dBc
	3rd Order IMD at 100MHz f1 = 99.9MHz, f2 = 100.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–98		dBc
	3rd Order IMD at 140MHz f1 = 139.9MHz, f2 = 140.1MHz	$V_{OUTDIFF}$ = $2V_{P-P}$ Envelope, R_I = R_F = 150Ω, R_{LOAD} = 400Ω			–88		dBc
OIP3	Equivalent OIP3 at 25MHz (Note 12) Equivalent OIP3 at 100MHz (Note 12) Equivalent OIP3 at 140MHz (Note 12)				59 53 48		dBm dBm dBm
t_S	Settling Time	$V_{OUTDIFF}$ = $2V_{P-P}$ Step, R_I = R_F = 150Ω, R_{LOAD} = 400Ω 1% Settling			 1.9		 ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN, V_{OCM}, and $\overline{SHDN}$) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6409C/LTC6409I are guaranteed functional over the temperature range of –40°C to 85°C. The LTC6409H is guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LTC6409C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6409C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LTC6409I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6409H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into the inputs (–IN and +IN). Input offset current is defined as the difference between the input currents (I_{OS} = $I_B^+ - I_B^-$).

ELECTRICAL CHARACTERISTICS

Note 7: Input common mode range is tested by testing at both V_{ICM} = 1.25V and at the Electrical Characteristics table limits to verify that the differential offset (V_{OSDIFF}) and the common mode offset (V_{OSCM}) have not deviated by more than ±1mV and ±2mV respectively from the V_{ICM} = 1.25V case.

The voltage range for the output common mode range is tested by applying a voltage on the V_{OCM} pin and testing at both V_{OCM} = 1.25V and at the Electrical Characteristics table limits to verify that the common mode offset (V_{OSCM}) has not deviated by more than ±6mV from the V_{OCM} = 1.25V case.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred offset voltage. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs and it is difficult to measure actual amplifier performance (See Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet). For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 9: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the output common mode offset voltage.

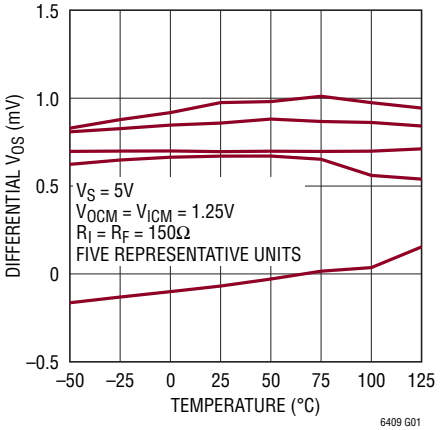
Note 10: Supply voltage range is guaranteed by power supply rejection ratio test.

Note 11: Extended operation with the output shorted may cause the junction temperature to exceed the 150°C limit.

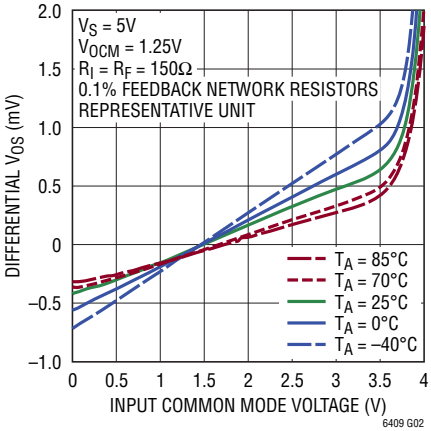
Note 12: Refer to Relationship Between Different Linearity Metrics in the Applications Information section of this data sheet for information on how to calculate an equivalent OIP3 from IMD3 measurements.

TYPICAL PERFORMANCE CHARACTERISTICS

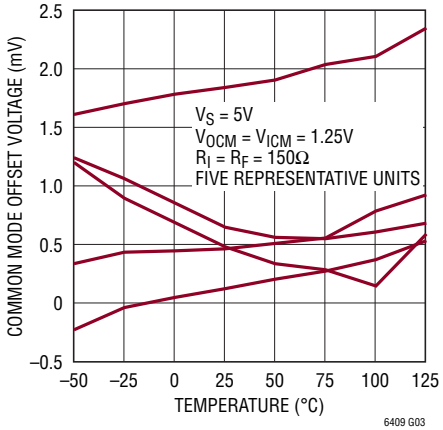
Differential Input Offset Voltage vs Temperature



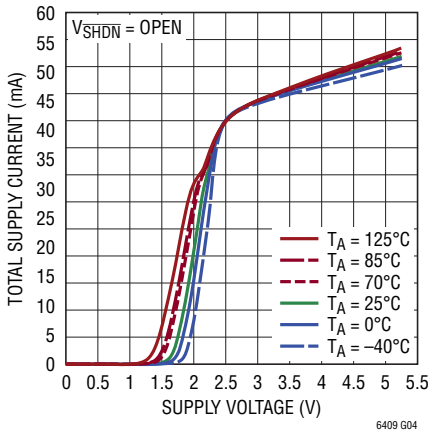
Differential Input Offset Voltage vs Input Common Mode Voltage



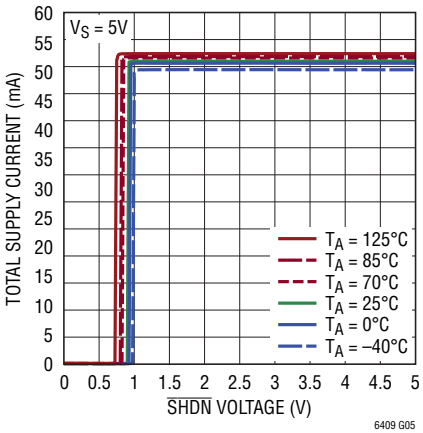
Common Mode Offset Voltage vs Temperature



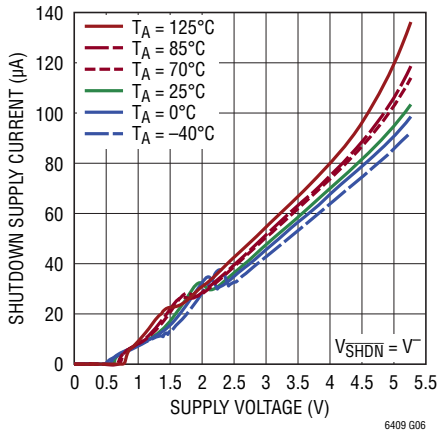
Supply Current vs Supply Voltage



Supply Current vs $\overline{SHDN}$ Voltage

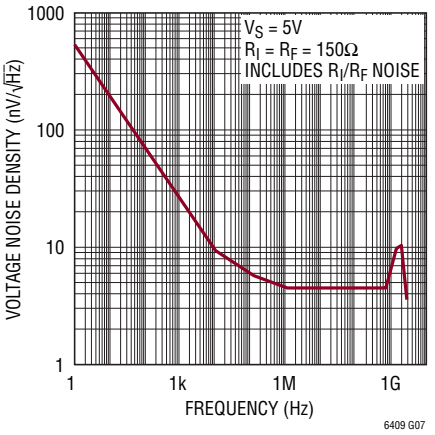


Shutdown Supply Current vs Supply Voltage

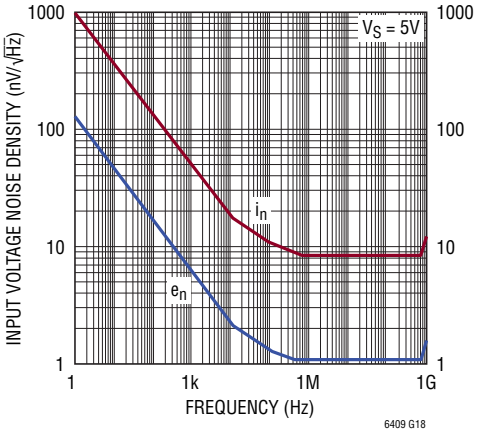


TYPICAL PERFORMANCE CHARACTERISTICS

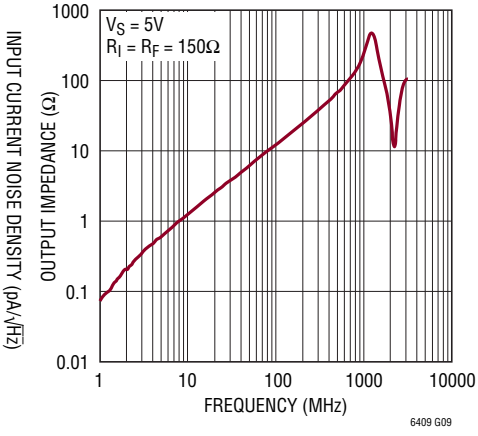
Differential Output Voltage Noise vs Frequency



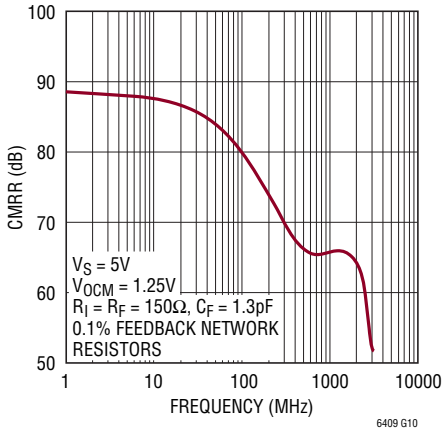
Input Noise Density vs Frequency



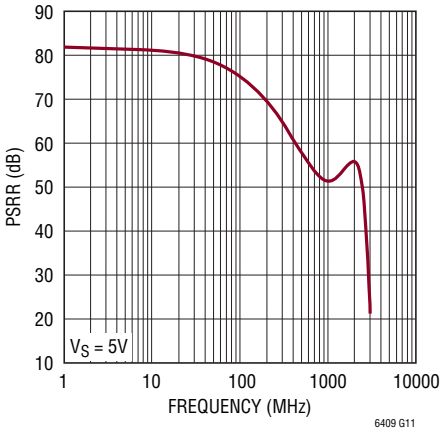
Differential Output Impedance vs Frequency



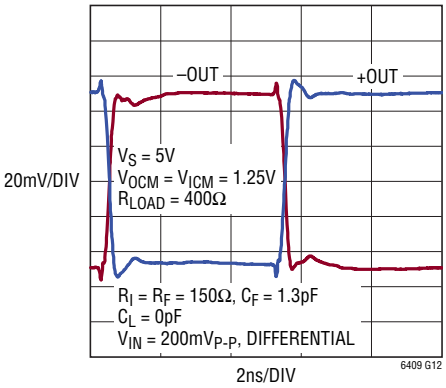
CMRR vs Frequency



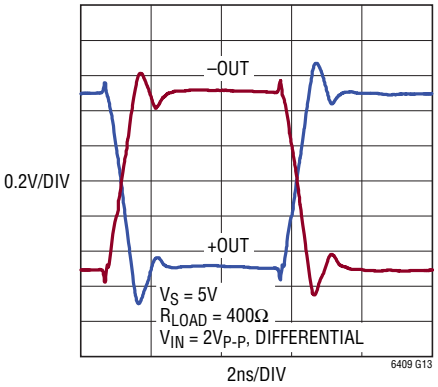
Differential PSRR vs Frequency



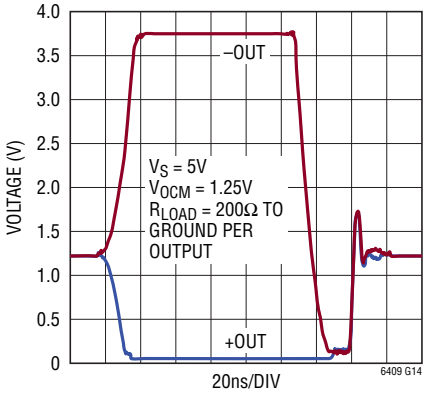
Small Signal Step Response



Large Signal Step Response

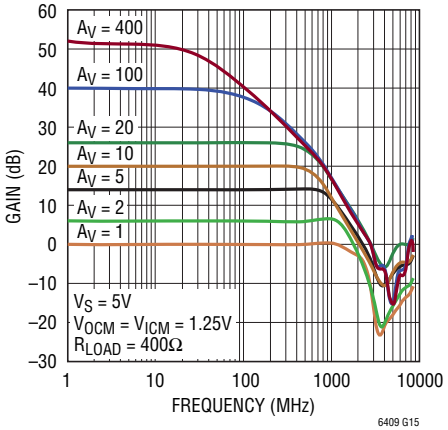


Overdriven Output Transient Response



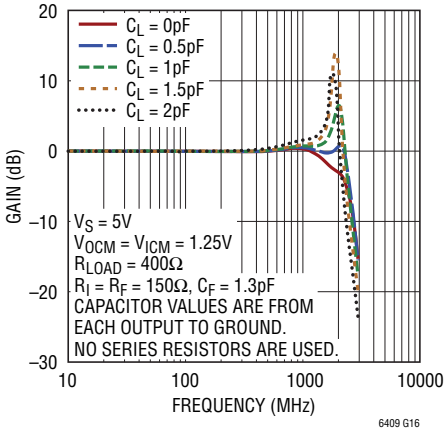
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response vs Closed Loop Gain

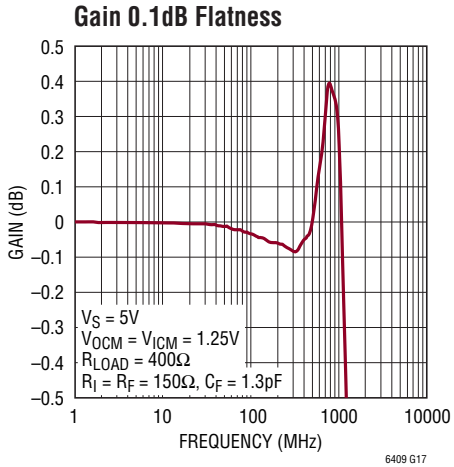


A_V (V/V)	R_I (Ω)	R_F (Ω)	C_F (pF)
1	150	150	1.3
2	100	200	1
5	50	250	0.8
10	50	500	0.4
20	25	500	0.4
100	25	2.5k	0
400	25	10k	0

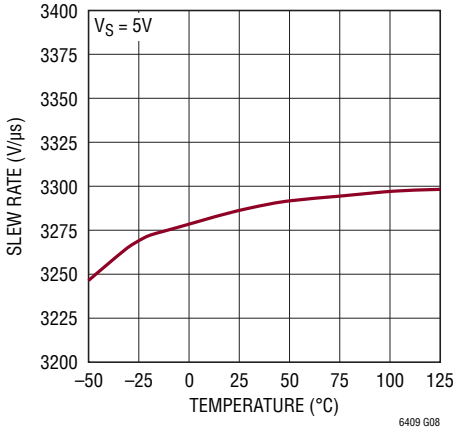
Frequency Response vs Load Capacitance



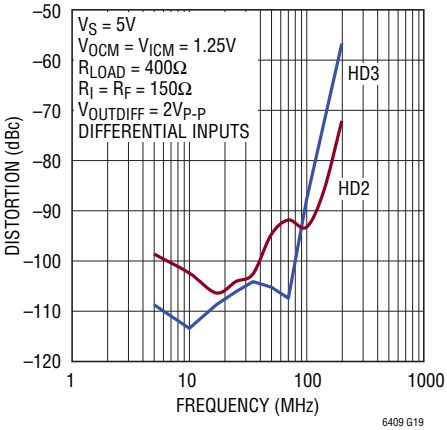
Gain 0.1dB Flatness



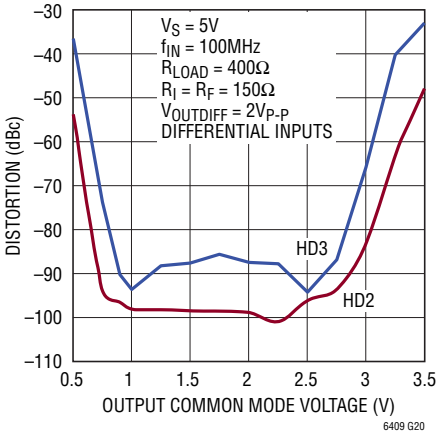
Slew Rate vs Temperature



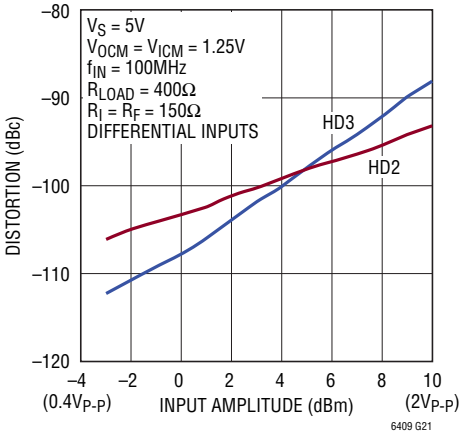
Harmonic Distortion vs Frequency



Harmonic Distortion vs Output Common Mode Voltage

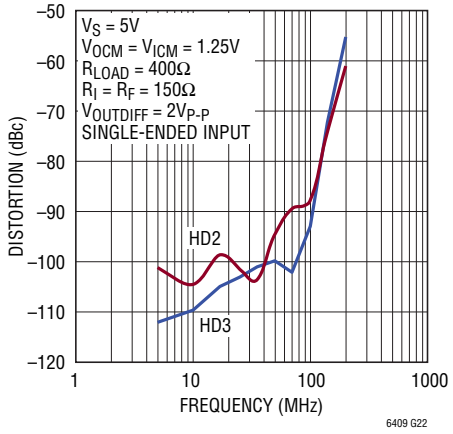


Harmonic Distortion vs Input Amplitude

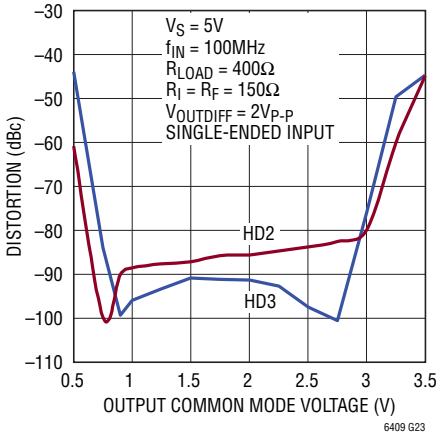


TYPICAL PERFORMANCE CHARACTERISTICS

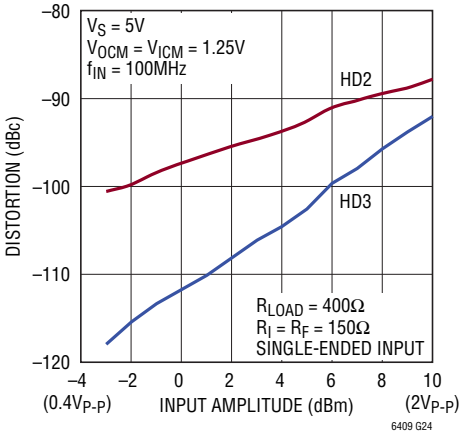
Harmonic Distortion vs Frequency



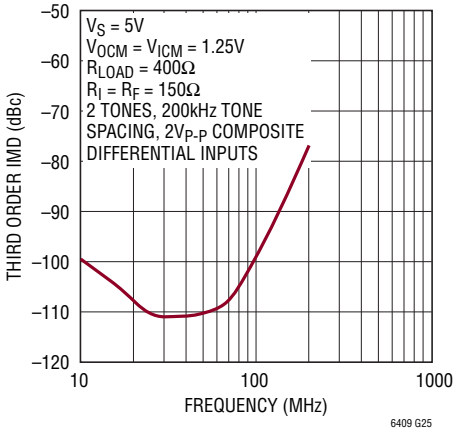
Harmonic Distortion vs Output Common Mode Voltage



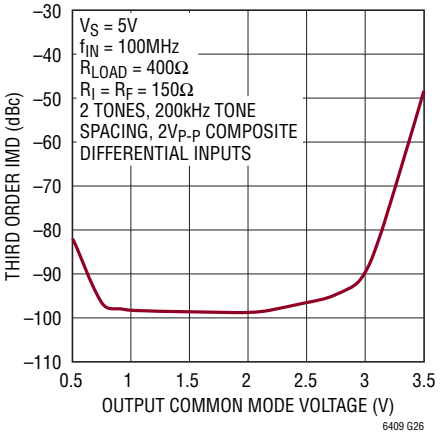
Harmonic Distortion vs Input Amplitude



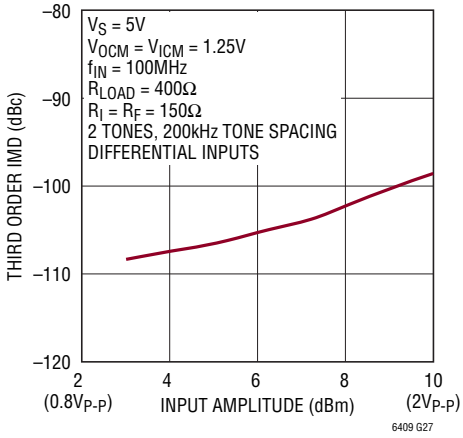
Intermodulation Distortion vs Frequency



Intermodulation Distortion vs Output Common Mode Voltage



Intermodulation Distortion vs Input Amplitude



PIN FUNCTIONS

+IN, –IN (Pins 2, 6): Non-Inverting and Inverting Input Pins.

$\overline{\text{SHDN}}$ (Pin 3): When $\overline{\text{SHDN}}$ is floating or directly tied to V^+, the LTC6409 is in the normal (active) operating mode. When the $\overline{\text{SHDN}}$ pin is connected to V^-, the part is disabled and draws approximately 100µA of supply current.

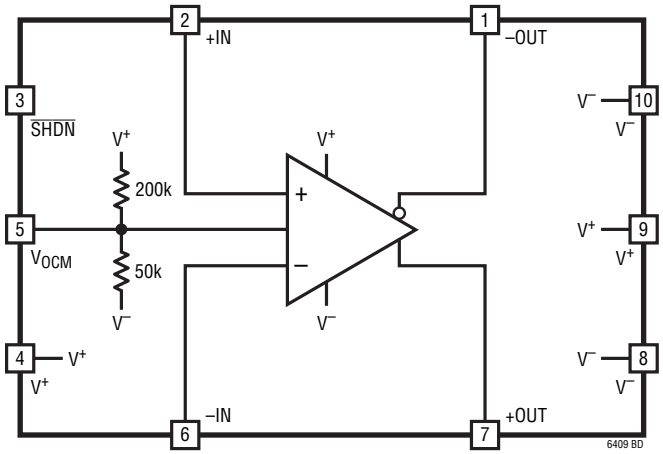
V^+, V^- (Pins 4, 9 and Pins 8, 10): Positive and Negative Power Supply Pins. Similar pins should be connected to the same voltage.

V_{OCM} (Pin 5): Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. If left floating, an internal resistor divider develops a default voltage of 1.25V with a 5V supply.

+OUT, –OUT (Pins 7, 1): Differential Output Pins.

Exposed Pad (Pin 11): Tie the bottom pad to V^-. If split supplies are used, DO NOT tie the pad to ground.

BLOCK DIAGRAM



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Functional Description

The LTC6409 is a small outline, wideband, high speed, low noise, and low distortion fully-differential amplifier with accurate output phase balancing. The amplifier is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6409 input common mode range includes ground, which makes it ideal to DC-couple and convert ground-referenced, single-ended signals into differential signals that are referenced to the user-supplied output common mode voltage. This is ideal for driving these differential ADCs. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). The LTC6409 can operate with a single-ended input and differential output, or with a differential input and differential output.

The outputs of the LTC6409 are capable of swinging from close-to-ground to 1V below V^+. They can source or sink up to approximately 70mA of current. Load capacitances should be decoupled with at least 10Ω of series resistance from each output.

Input Pin Protection

The LTC6409 input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back to back between +IN and –IN. Moreover, the input pins, as well as V_{OCM} and $\overline{SHDN}$ pins, have clamping diodes to either power supply. If these pins are driven to voltages which exceed either supply, the current should be limited to 10mA to prevent damage to the IC.

$\overline{SHDN}$ Pin

The $\overline{SHDN}$ pin is a CMOS logic input with a 150k internal pull-up resistor. If the pin is driven low, the LTC6409 powers down. If the pin is left unconnected or driven high, the part is in normal active operation. Some care should be taken to control leakage currents at this pin to prevent inadvertently putting the LTC6409 into shutdown. The turn-on and turn-off time between the shutdown and active states is typically less than 200ns.

General Amplifier Applications

In Figure 1, the gain to $V_{OUTDIFF}$ from V_{INP} and V_{INM} is given by:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \bullet \left(V_{INP} - V_{INM}\right) \quad (1)$$

Note from Equation (1), the differential output voltage (V_{+OUT} – V_{-OUT}) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6409 ideally

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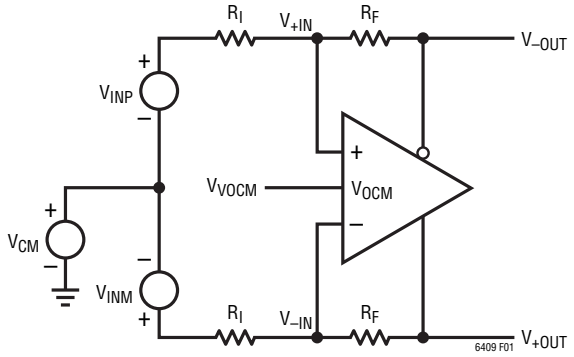

Figure 1. Circuit for Common Mode Range

suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop.

If the V_{OCM} pin is left open, an internal resistor divider develops a default voltage of 1.25V with a 5V supply. The V_{OCM} pin can be overdriven to another voltage if desired. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 40k input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

Input Common Mode Voltage Range

The LTC6409's input common mode voltage (V_{ICM}) is defined as the average of the two input pins, V_{+IN} and V_{-IN}. The valid range that can be used for V_{ICM} has been specified in the Electrical Characteristics table (V_{ICMR}). However, due to external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is even wider. The input common mode range at the op amp inputs depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 1). For fully differential input applications, where $V_{INP} = -V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + V_{CM} \bullet \frac{R_F}{R_I + R_F}$$

With single-ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common mode voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \bullet \frac{R_I}{R_I + R_F} + \quad (2)$$

$$V_{CM} \bullet \frac{R_F}{R_I + R_F} + \frac{V_{INP}}{2} \bullet \frac{R_F}{R_I + R_F}$$

This means that if, for example, the input signal (V_{INP}) is a sine, an attenuated version of that sine signal also appears at the op amp inputs.

Input Impedance and Loading Effects

The low frequency input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on how the inputs are driven. For fully differential input sources ($V_{INP} = -V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{1 - \frac{1}{2} \bullet \frac{R_F}{R_I + R_F}}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated. If input impedance matching is required by the source,

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a termination resistor R_T should be chosen (see Figure 2) such that:

$$R_T = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 2, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, given above. Also, R2 is chosen as:

$$R2 = R_T \,||\, R_S = \frac{R_T \bullet R_S}{R_T + R_S}$$

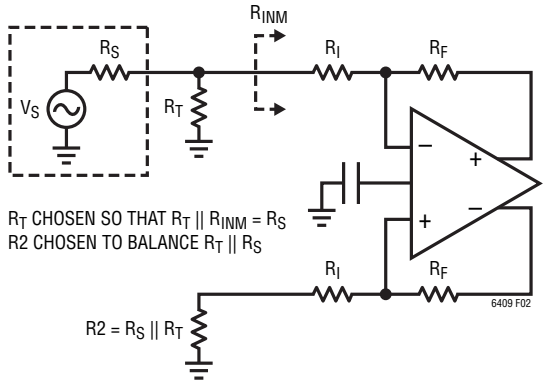

Figure 2. Optimal Compensation for Signal Source Impedance

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram which takes into consideration that real world resistors will not match perfectly. Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx V_{INDIFF} \bullet \frac{R_F}{R_I} +$$

$$V_{CM} \bullet \frac{\Delta\beta}{\beta_{AVG}} - V_{OCM} \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

where R_F is the average of R_{F1}, and R_{F2}, and R_I is the average of R_{I1}, and R_{I2}.

β_{AVG} is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

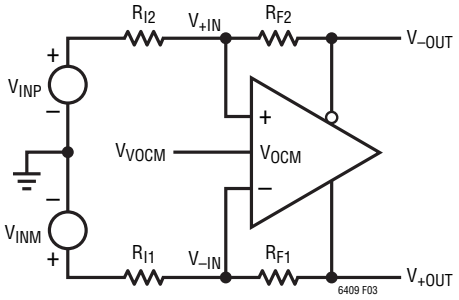

Figure 3. Real-World Application with Feedback Resistor Pair Mismatch

$\Delta\beta$ is defined as the difference in the feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

Here, V_{CM} and V_{INDIFF} are defined as the average and the difference of the two input voltages V_{INP} and V_{INM}, respectively:

$$V_{CM} = \frac{V_{INP} + V_{INM}}{2}$$

$$V_{INDIFF} = V_{INP} - V_{INM}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs. Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx (V_{CM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}} \quad (3)$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 0.1% resistors or better will mitigate most problems and will provide about 54dB worst case of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin.

There may be concern on how feedback factor mismatch affects distortion. Feedback factor mismatch from using 1% resistors or better, has a negligible effect on distortion. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage,

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resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

The apparent input referred offset induced by feedback factor mismatch is derived from Equation (3):

$V_{OSDIFF(APPARENT)} \approx (V_{CM} - V_{OCM}) \bullet \Delta\beta$

Using the LTC6409 in a single 5V supply application with 0.1% resistors, the input common mode grounded, and the V_{OCM} pin biased at 1.25V, the worst case mismatch can induce 1.25mV of apparent offset voltage.

Noise and Noise Figure

The LTC6409's differential input referred voltage and current noise densities are 1.1nV/√Hz and 8.8pA/√Hz, respectively. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A simplified noise model is shown in Figure 4. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1 + \frac{R_F}{R_I}\right)\right]^2 + 2 \bullet \left(i_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \frac{R_F}{R_I}\right)^2 + 2 \bullet e_{nRF}^2}$$

If the circuits surrounding the amplifier are well balanced, common mode noise (e_{nVOCM}) of the amplifier does not appear in the differential output noise equation given above. A plot of this equation and a plot of the noise generated by the feedback components for the LTC6409 are shown in Figure 5.

The LTC6409's input referred voltage noise contributes the equivalent noise of a 75Ω resistor. When the feedback network is comprised of resistors whose values are larger than this, the output noise is resistor noise and amplifier current noise dominant. For feedback networks consisting of resistors with values smaller than 75Ω, the output noise is voltage noise dominant (see Figure 5).

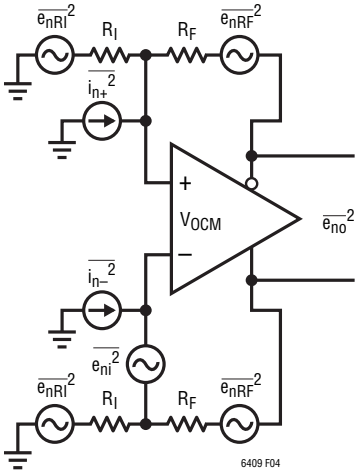

Figure 4. Simplified Noise Model

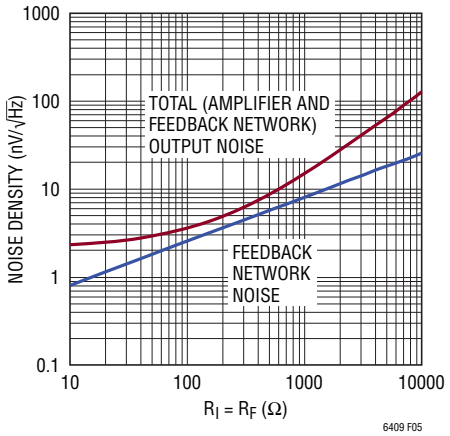

Figure 5. LTC6409 Output Noise vs Noise Contributed by Feedback Network Alone

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading by the feedback network on the output. Higher resistor values will result in higher output noise, but typically improved distortion due to less loading on the output. For this reason, when LTC6409 is configured in a differential gain of 1, using feedback resistors of at least 150Ω is recommended.

To calculate noise figure (NF), a source resistance and the noise it generates should also come into consideration. Figure 6 shows a noise model for the amplifier which includes the source resistance (R_S). To generalize the

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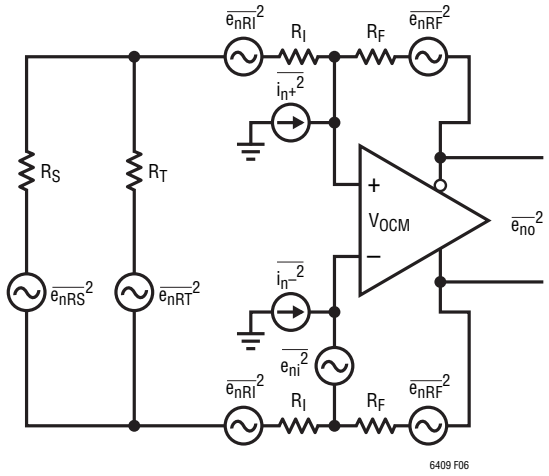

Figure 6. A More General Noise Model Including Source and Termination Resistors

calculation, a termination resistor (R_T) is included and its noise contribution is taken into account.

Now, the total output noise power (excluding the noise contribution of R_S) is calculated as:

$$e_{no}^2 = \left[e_{ni} \bullet \left(1 + \frac{R_F}{R_I + \left(\frac{R_T \| R_S}{2} \right)} \right) \right]^2 + 2 \bullet \left(i_n \bullet R_F \right)^2 +$$

$$2 \bullet \left(e_{nRI} \bullet \frac{R_F}{R_I + \left(\frac{R_T \| R_S}{2} \right)} \right)^2 + 2 \bullet e_{nRF}^2 +$$

$$\left[e_{nRT} \bullet \frac{R_F}{R_I} \bullet \left(\frac{2R_I \| R_S}{R_T + \left(2R_I \| R_S \right)} \right) \right]^2$$

Meanwhile, the output noise power due to noise of R_S is given by:

$$e_{no\,(RS)}^2 = \left[e_{nRS} \bullet \frac{R_F}{R_I} \bullet \left(\frac{2R_I \| R_T}{R_S + \left(2R_I \| R_T \right)} \right) \right]^2$$

Finally, noise figure can be obtained as:

$$NF = 10 \log \left(1 + \frac{e_{no}^2}{e_{no\,(RS)}^2} \right)$$

Figure 7 specifies the measured total output noise (e_{no}), excluding the noise contribution of source resistance, and noise figure (NF) of LTC6409 configured at closed loop gains ($A_V = R_F/R_I$) of 1V/V, 2V/V and 5V/V. The circuits in the left column use termination resistors and transformers to match to the 50Ω source resistance, while the circuits in the right column do not have such matching. For simplicity, DC-blocking and bypass capacitors have not been shown in the circuits, as they do not affect the noise results.

Relationship Between Different Linearity Metrics

Linearity is, of course, an important consideration in many amplifier applications. This section relates the intermodulation distortion of fully differential amplifiers to other linearity metrics commonly used in RF style blocks.

Intercept points are specifications that have long been used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall performance of a receiver chain, thus resulting in simpler system-level calculations. Traditionally, these systems use primarily single-ended RF amplifiers as gain blocks designed to operate in a 50Ω environment, just like the rest of the receiver chain. Since intercept points are given in dBm, this implies an associated impedance of 50Ω.

However, for LTC6409 as a differential feedback amplifier with low output impedance, a 50Ω resistive load is not required (unlike an RF amplifier). This distinction is important when evaluating the intercept point for LTC6409. In fact, the LTC6409 yields optimum distortion performance when loaded with 200Ω to 1kΩ (at each output), very similar to the input impedance of an ADC. As a result, terminating

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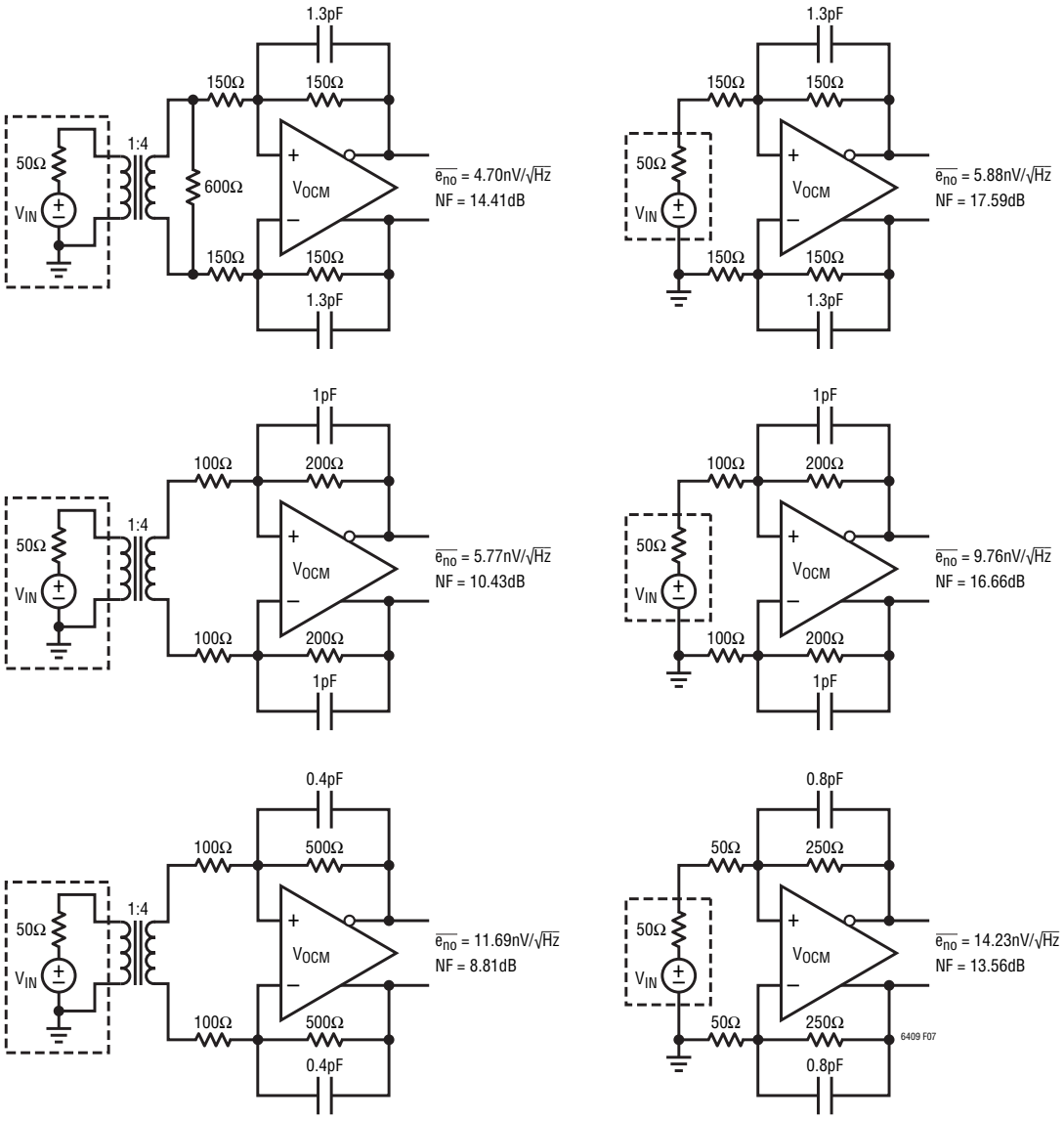

Figure 7. LTC6409 Measured Output Noise and Noise Figure at Different Closed Loop Gains with and without Source Impedance Matching

the input of the ADC to 50Ω can actually be detrimental to system performance.

The definition of 3rd order intermodulation distortion (IMD3) is shown in Figure 8. Also, a graphical representation of how to relate IMD3 to output/input 3rd order intercept points (OIP3/IIP3) has been depicted in Figure 9. Based on this figure, Equation (4) gives the definition of the intercept point, relative to the intermodulation distortion.

$$OIP3 = P_O + \frac{|IMD3|}{2} \quad (4)$$

P_O is the output power of each of the two tones at which IMD3 is measured, as shown in Figure 9. It is calculated in dBm as:

$$P_O = 10\log\left(\frac{V^2_{PDIFF}}{2 \bullet R_L \bullet 10^{-3}}\right) \quad (5)$$

where R_L is the differential load resistance, and V_{PDIFF} is the differential peak voltage for a single tone. Normally, intermodulation distortion is specified for a benchmark composite differential peak of $2V_{P-P}$ at the output of the

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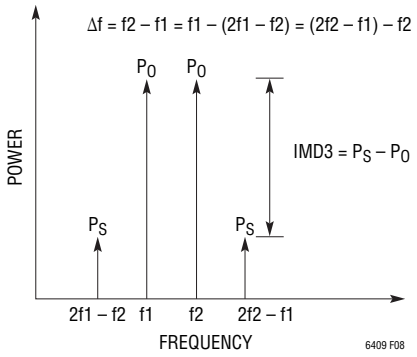


Figure 8. Definition of IMD3

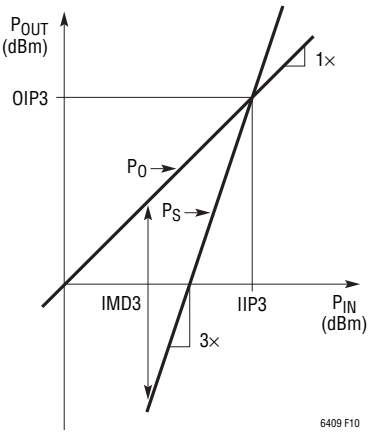


Figure 9. Graphical Representation of the Relationship between IMD3 and OIP3

amplifier, implying that each single tone is $1V_{P-P}$, resulting in V_{PDIFF} = 0.5V. Using R_L = 50Ω as the associated impedance, P_O is calculated to be close to 4dBm.

As seen in Equation (5), when a higher impedance is used, the same level of intermodulation distortion performance results in a lower intercept point. Therefore, it is important to consider the impedance seen by the output of the LTC6409 when working with intercept points.

Comparing linearity specifications between different amplifier types becomes easier when a common impedance level is assumed. For this reason, the intercept points for LTC6409 are reported normalized to a 50Ω load impedance. This is the reason why OIP3 in the Electrical Characteristics table is 4dBm more than half the absolute value of IMD3.

If the top half of the LTC6409 demo board (DC1591A, shown in Figure 12) is used to measure IMD3 and OIP3, one should make sure to properly convert the power seen at the differential output of the amplifier to the power that appears at the single-ended output of the demo board. Figure 10 shows an equivalent representation of the top half of the demo board. This view ignores the DC-blocking and bypass capacitors, which do not affect the analysis here. The transmission line transformers (used mainly for impedance matching) are modeled here as ideal 4:1 impedance transformers together with a –1dB block. This separates the insertion loss of the transformer from its ideal behavior. The 100Ω resistors at the LTC6409 output create a differential 200Ω resistance, which is an impedance match for the reflected R_L.

As previously mentioned, IMD3 is measured for $2V_{P-P}$ differential peak (i.e. 10dBm) at the output of the LTC6409, corresponding to $1V_{P-P}$ (i.e. 4dBm) at each output alone. From LTC6409 output (location A in Figure 10) to the input of the output transformer (location B), there is a voltage attenuation of 1/2 (or –6dB) formed by the resistive divider

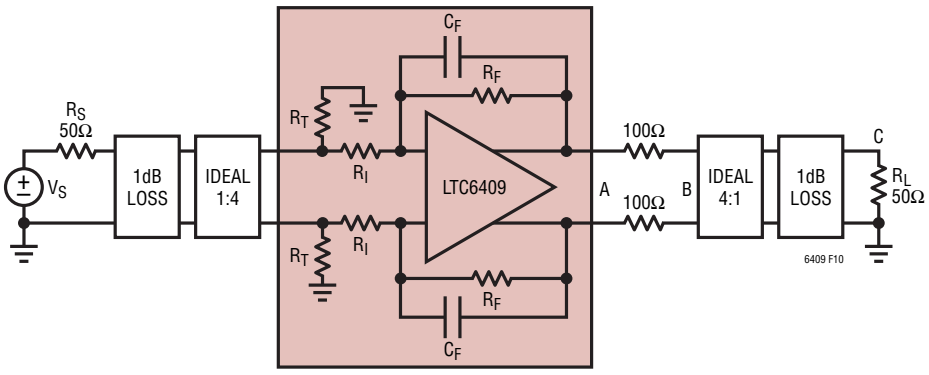


Figure 10. Equivalent Schematic of the Top Half of the LTC6409 Demo Board

APPLICATIONS INFORMATION

between the R_L • 4 = 200Ω differential resistance seen at location B and the 200Ω formed by the two 100Ω matching resistors at the LTC6409 output. Thus, the differential power at location B is 10 – 6 = 4dBm. Since the transformer ratio is 4:1 and it has an insertion loss of about 1dB, the power at location C (across R_L) is calculated to be 4 – 6 – 1 = –3dBm. This means that IMD3 should be measured while the power at the output of the demo board is –3dBm which is equivalent to having $2V_{P-P}$ differential peak (or 10dBm) at the output of the LTC6409.

GBW vs f_{-3dB}

Gain-bandwidth product (GBW) and –3dB frequency (f_{-3dB}) have been both specified in the Electrical Characteristics table as two different metrics for the speed of the LTC6409. GBW is obtained by measuring the gain of the amplifier at a specific frequency (f_{TEST}) and calculate gain • f_{TEST}. To measure gain, the feedback factor (i.e. $\beta = R_I/(R_I + R_F)$) is chosen sufficiently small so that the feedback loop does not limit the available gain of the LTC6409 at f_{TEST}, ensuring that the measured gain is the open loop gain of the amplifier. As long as this condition is met, GBW is a parameter that depends only on the internal design and compensation of the amplifier and is a suitable metric to specify the inherent speed capability of the amplifier.

f_{-3dB}, on the other hand, is a parameter of more practical interest in different applications and is by definition the frequency at which the gain is 3dB lower than its low frequency value. The value of f_{-3dB} depends on the speed of the amplifier as well as the feedback factor. Since the LTC6409 is designed to be stable in a differential signal gain of 1 (where $R_I = R_F$ or $\beta = 1/2$), the maximum f_{-3dB} is obtained and measured in this gain setting, as reported in the Electrical Characteristics table.

In most amplifiers, the open loop gain response exhibits a conventional single-pole roll-off for most of the frequencies before crossover frequency and the GBW and f_{-3dB} numbers are close to each other. However, the LTC6409 is intentionally compensated in such a way that its GBW is significantly larger than its f_{-3dB}. This means that at lower frequencies (where the input signal frequencies typically lie, e.g. 100MHz) the amplifier's gain and the thus the feedback loop gain is larger. This has the important advantage of further linearizing the amplifier and improving distortion at those frequencies.

Looking at the Frequency Response vs Closed Loop Gain graph in the Typical Performance Characteristics section of this data sheet, one sees that for a closed loop gain (A_V) of 1 (where $R_I = R_F = 150\Omega$), f_{-3dB} is about 2GHz. However, for A_V = 400 (where $R_I = 25\Omega$ and $R_F = 10k\Omega$), the gain at 100MHz is close to 40dB = 100V/V, implying a GBW value of 10GHz.

Feedback Capacitors

When the LTC6409 is configured in low differential gains, it is often advantageous to utilize a feedback capacitor (C_F) in parallel with each feedback resistor (R_F). The use of C_F implements a pole-zero pair (in which the zero frequency is usually smaller than the pole frequency) and adds positive phase to the feedback loop gain around the amplifier. Therefore, if properly chosen, the addition of C_F boosts the phase margin and improves the stability response of the feedback loop. For example, with $R_I = R_F = 150\Omega$, it is recommended for most general applications to use C_F = 1.3pF across each R_F. This value has been selected to maximize f_{-3dB} for the LTC6409 while keeping the peaking of the closed loop gain versus frequency response under a reasonable level (<1dB). It also results in the highest frequency for 0.1dB gain flatness ($f_{0.1dB}$).

However, other values of C_F can also be utilized and tailored to other specific applications. In general, a larger value for C_F reduces the peaking (overshoot) of the amplifier in both frequency and time domains, but also decreases the closed loop bandwidth (f_{-3dB}). For example, while for a closed loop gain (A_V) of 5, C_F = 0.8pF results in maximum f_{-3dB} (as previously shown in the Frequency Response vs Closed Loop Gain graph of this data sheet), if C_F = 1.2pF is used, the amplifier exhibits no overshoot in the time domain which is desirable in certain applications. Both the circuits discussed in this section have been shown in the Typical Applications section of this data sheet.

APPLICATIONS INFORMATION

Board Layout and Bypass Capacitors

For single supply applications, it is recommended that high quality 0.1µF||1000pF ceramic bypass capacitors be placed directly between each V^+ pin and its closest $V^–$ pin with short connections. The $V^–$ pins (including the Exposed Pad) should be tied directly to a low impedance ground plane with minimal routing.

For dual (split) power supplies, it is recommended that additional high quality 0.1µF||1000pF ceramic capacitors be used to bypass V^+ pins to ground and $V^–$ pins to ground, again with minimal routing.

For driving heavy differential loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than do leaded capacitors, and perform best in high speed applications.

To prevent degradation in stability response, it is highly recommended that any stray capacitance at the input pins, +IN and –IN, be kept to an absolute minimum by keeping printed circuit connections as short as possible. This becomes especially true when the feedback resistor network uses resistor values greater than 500Ω in circuits with $R_I = R_F$.

At the output, always keep in mind the differential nature of the LTC6409, because it is critical that the load impedances seen by both outputs (stray or intended), be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6409 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

The V_{OCM} pin should be bypassed to the ground plane with a high quality ceramic capacitor of at least 0.01µF. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by impedance mismatches both externally and internally to the IC.

Driving ADCs

The LTC6409's ground-referenced input, differential output and adjustable output common mode voltage make it ideal for interfacing to differential input ADCs. These ADCs are typically supplied from a single-supply voltage and have an optimal common mode input range near mid-supply. The LTC6409 interfaces to these ADCs by providing single-ended to differential conversion and common mode level shifting.

The sampling process of ADCs creates a transient that is caused by the switching in of the ADC sampling capacitor. This momentarily shorts the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended, for a valid representation of the input signal. The LTC6409 will settle quickly from these periodic load impulses. The RC network between the outputs of the driver and the inputs of the ADC decouples the sampling transient of the ADC (see Figure 11). The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LTC6409 are used to dampen and attenuate any charge injected by the ADC. The RC filter gives the additional benefit of band limiting broadband output noise. Generally, longer time constants improve SNR at the expense of settling time. The resistors in the decoupling network should be at least 10Ω. These resistors also serve to decouple the LTC6409 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. In 16-bit applications, this will typically require a minimum of eleven RC time constants. For lowest distortion, choose capacitors with low dielectric absorption (such as a C0G multilayer ceramic capacitor).

APPLICATIONS INFORMATION

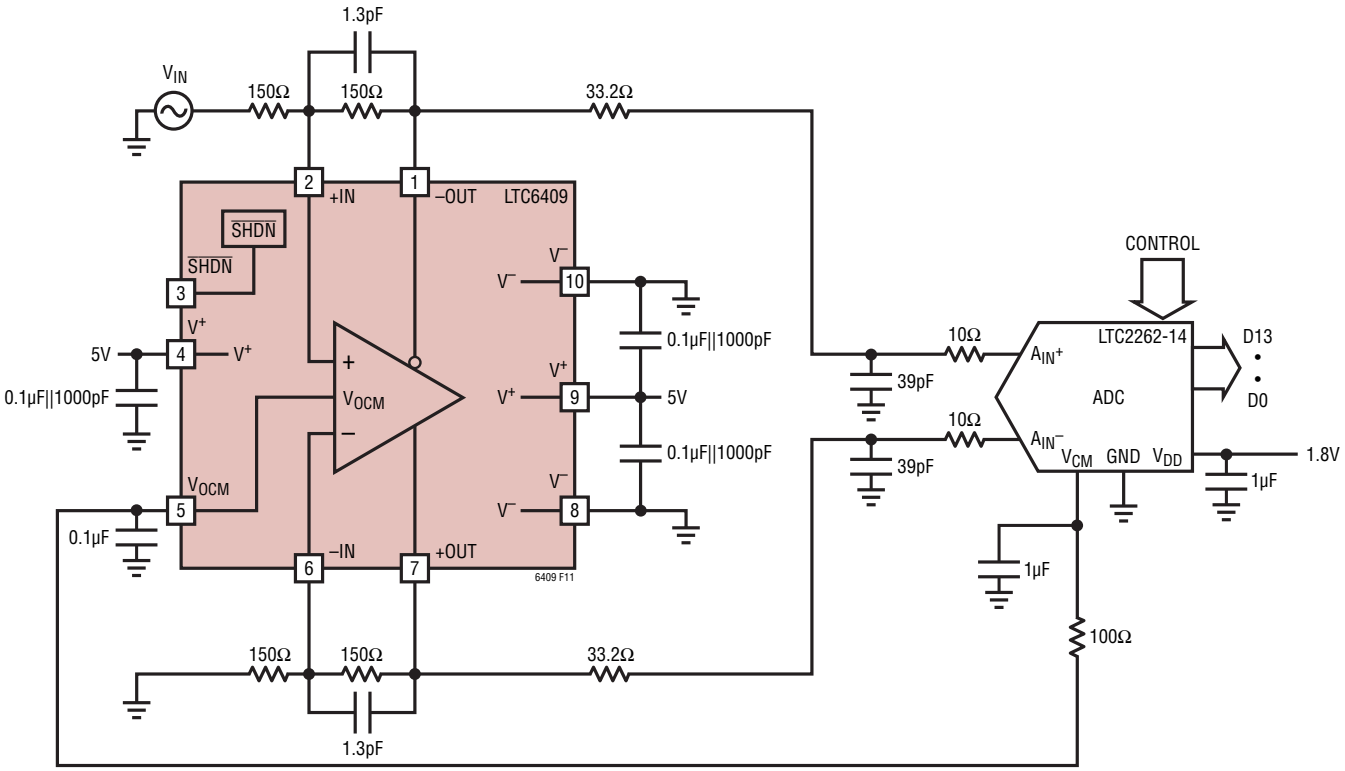


Figure 11. Driving an ADC

APPLICATIONS INFORMATION

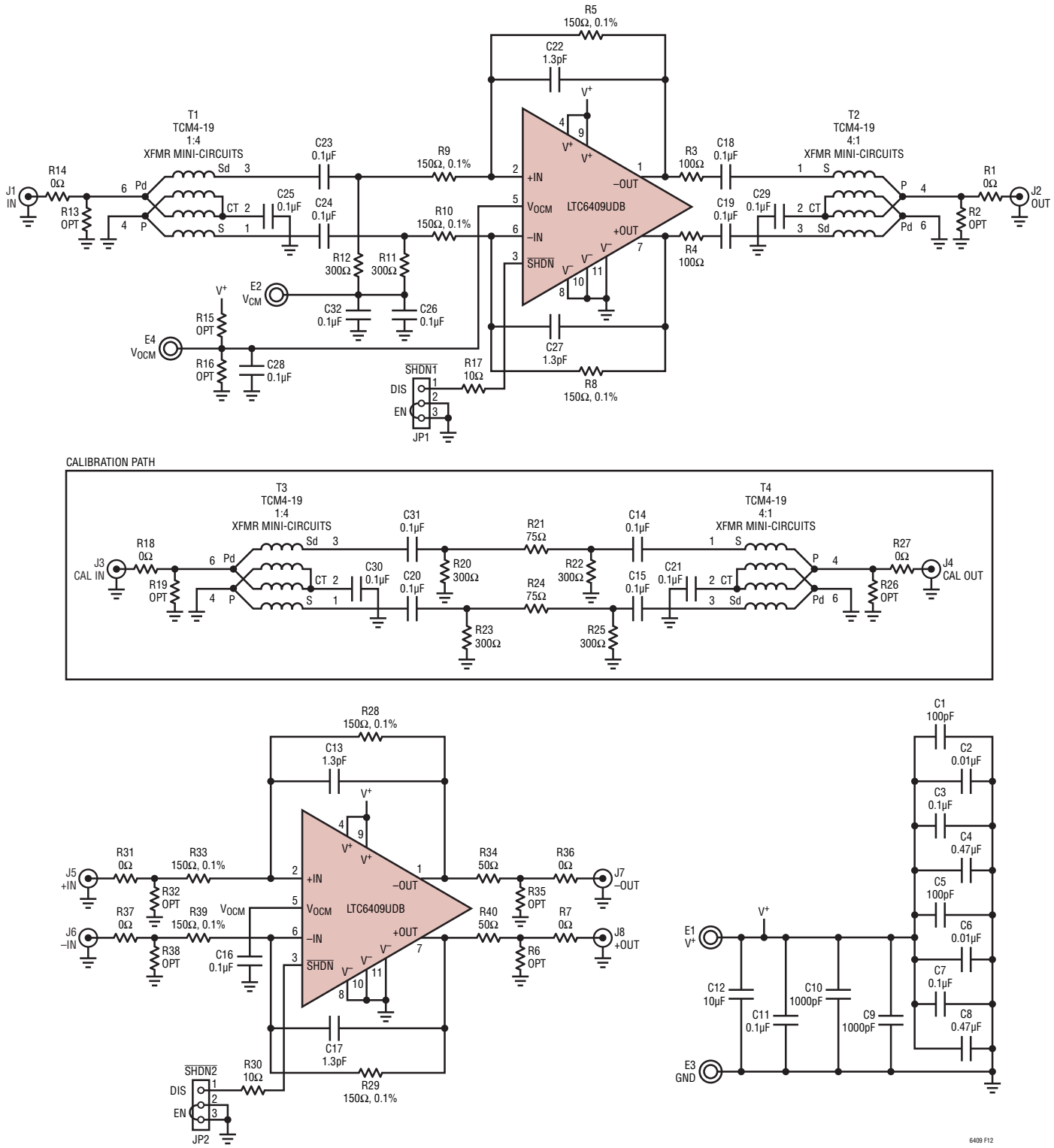


Figure 12. Demo Board DC1591A Schematic

APPLICATIONS INFORMATION

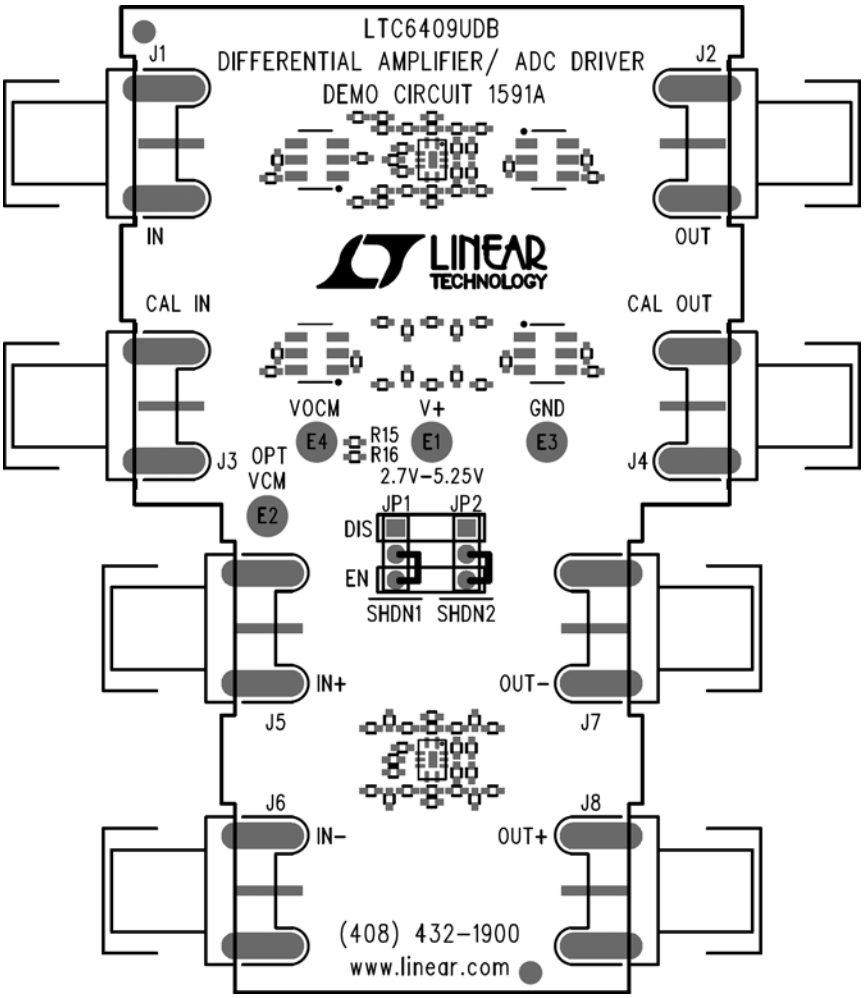
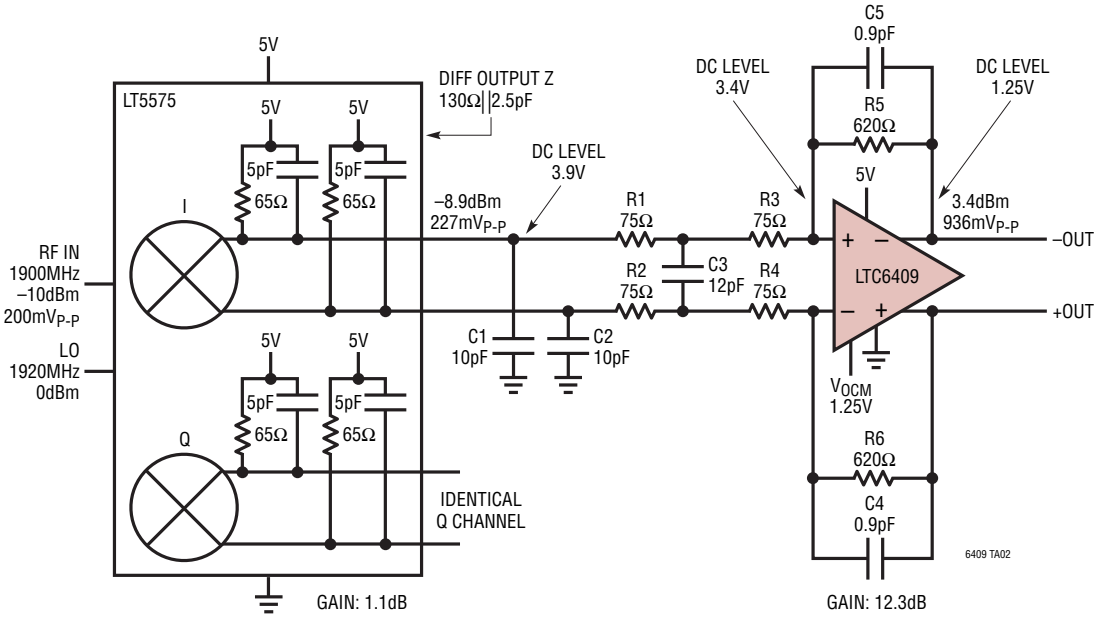


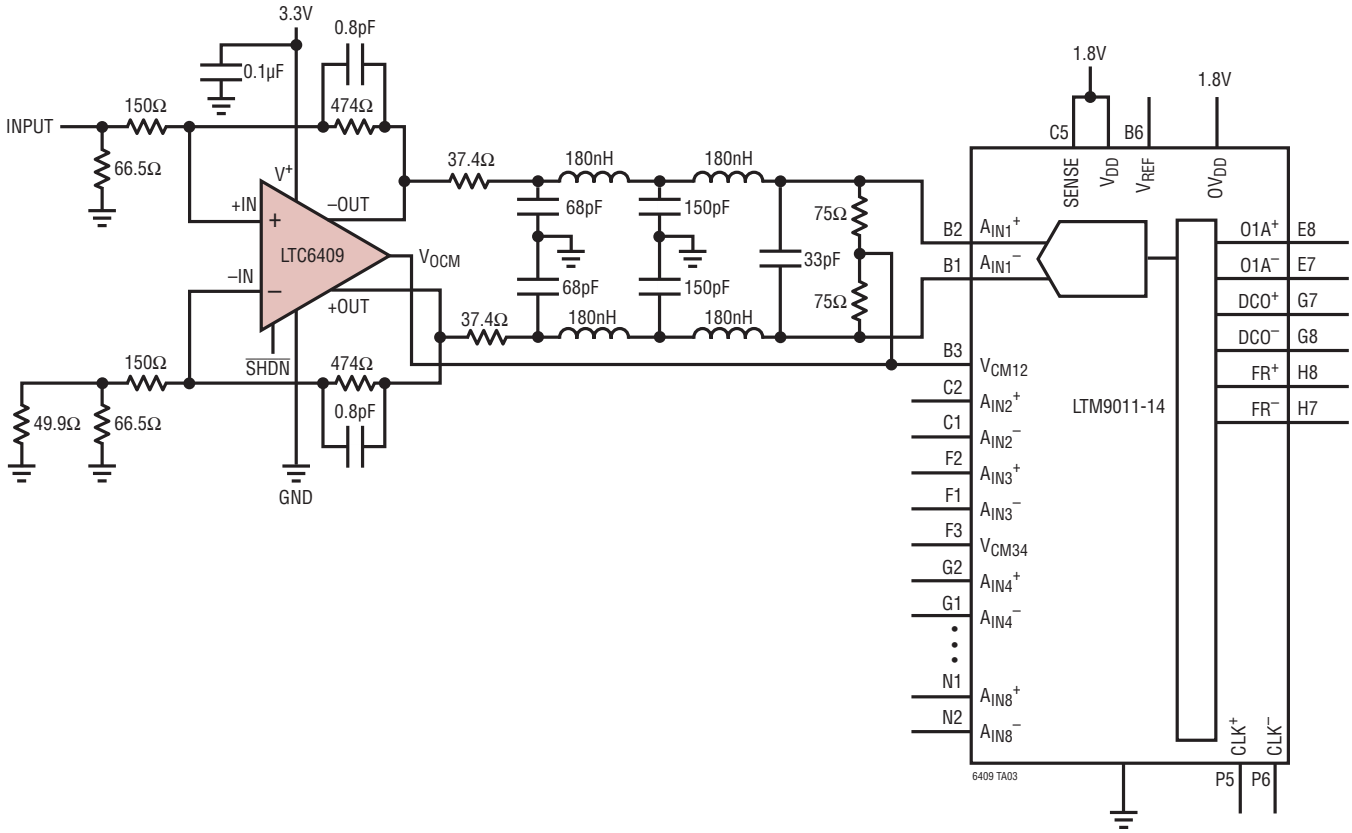
Figure 13. Demo Board DC1591A Layout

TYPICAL APPLICATIONS

DC-Coupled Level Shifting of an I/Q Demodulator Output

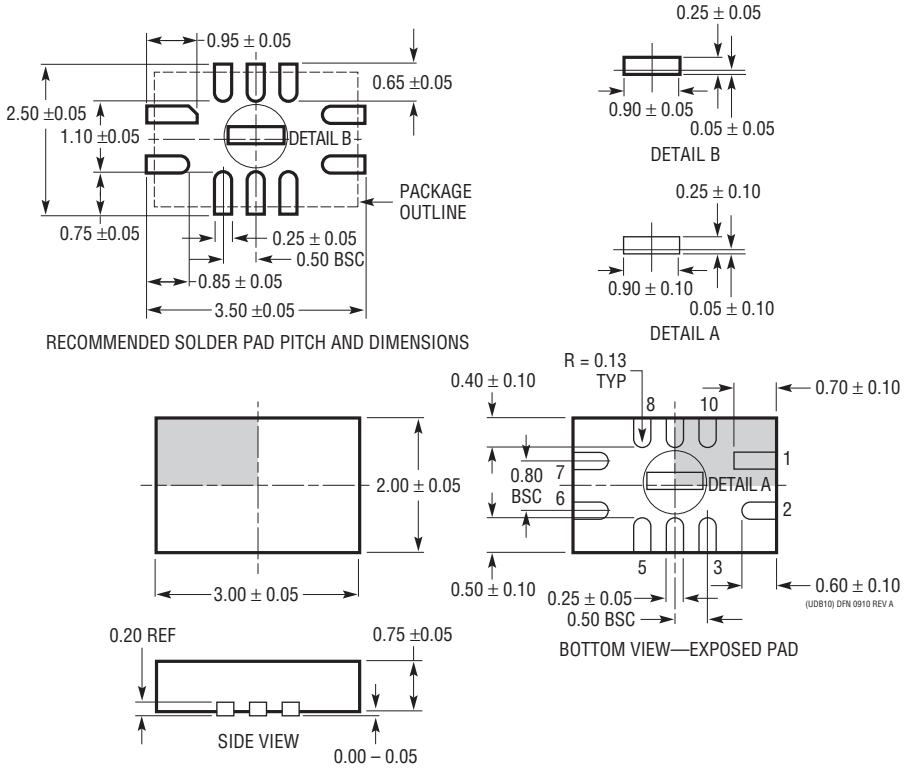


Single-Ended to Differential Conversion Using LTC6409 and 50MHz Lowpass Filter (Only One Channel Shown)



PACKAGE DESCRIPTION

UDB Package
10-Lead Plastic QFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1848 Rev A)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

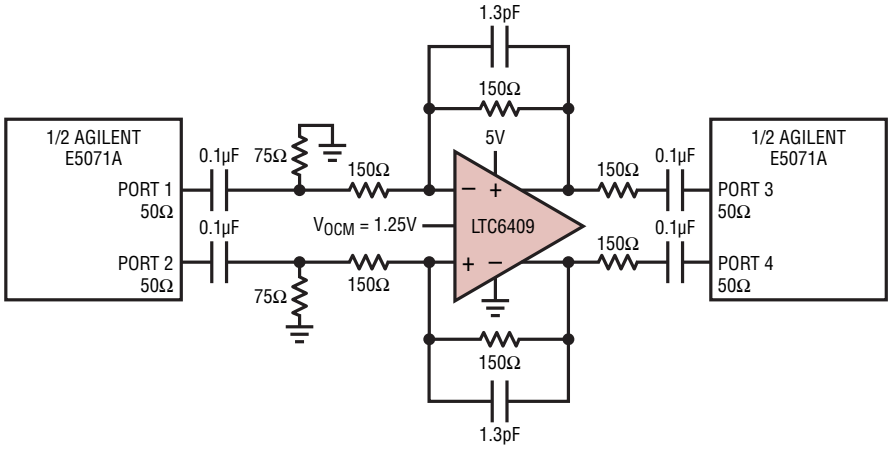
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/10	Revised Typical Application drawing	21

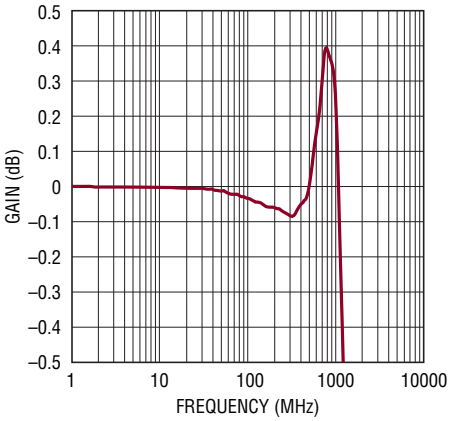
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

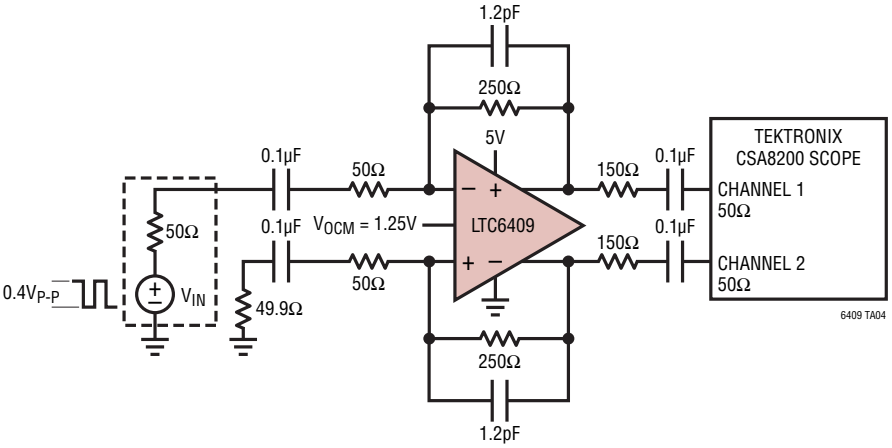
TYPICAL APPLICATIONS

LTC6409 Externally Compensated for Maximum Gain Flatness and for No-Overshoot Time-Domain Response

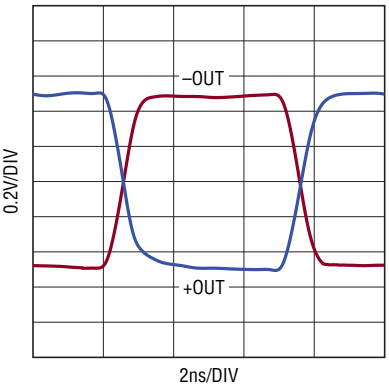


Gain 0.1dB Flatness





No-Overshoot Step Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion, Differential ADC Drivers	–71dBc IM3 at 240MHz $2V_{P-P}$ Composite, I_S = 90mA, A_V = 8dB/14dB/20dB/26dB
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion, Differential ADC Drivers	–74dBc IM3 at 140MHz $2V_{P-P}$ Composite, I_S = 50mA, A_V = 8dB/14dB/20dB/26dB
LTC6406/LTC6405	3GHz/2.7GHz Low Noise, Rail-to-Rail Input Differential Amplifier/Driver	–70dBc/–65dBc Distortion at 50MHz, I_S = 18mA, 1.6nV/$\sqrt{Hz}$ Noise, 3V/5V Supply
LTC6416	2GHz Low Noise, Differential 16-Bit ADC Buffer	–72.5dBc IM3 at 300MHz $2V_{P-P}$ Composite, 150mW on 3.6V Supply
LTC2209	16-Bit, 160Msps ADC	100dB SFDR, V_{DD} = 3.3V, V_{CM} = 1.25V
LTC2262-14	14-Bit, 150Msps Ultralow Power 1.8V ADC	88dB SFDR, 149mW, V_{DD} = 1.8V, V_{CM} = 0.9V

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