

Features

- Fast Read Access Time - 45 ns
- Low-Power CMOS Operation
 - 100 μ A max. Standby
 - 20 mA max. Active at 5 MHz
- JEDEC Standard Packages
 - 28-Lead 600-mil PDIP
 - 32-Lead PLCC
 - 28-Lead TSOP and SOIC
- 5V $\pm$ 10% Supply
- High-Reliability CMOS Technology
 - 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 μ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial, Industrial and Automotive Temperature Ranges

Description

The AT27C512R is a low-power, high-performance 524,288-bit one-time programmable read only memory (OTP EPROM) organized 64K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

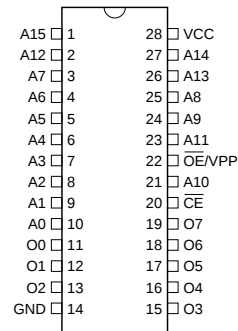
Atmel's scaled CMOS technology provides high-speed, lower active power consumption, and significantly faster programming. Power consumption is typically only 8 mA in Active Mode and less than 10 μ A in Standby.

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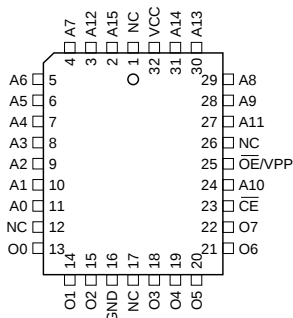
Pin Configurations

Pin Name	Function
A0 to A15	Addresses
O0 - O7	Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE/VPP}}$	Output Enable/VPP
NC	No Connect

PDIP, SOIC Top View

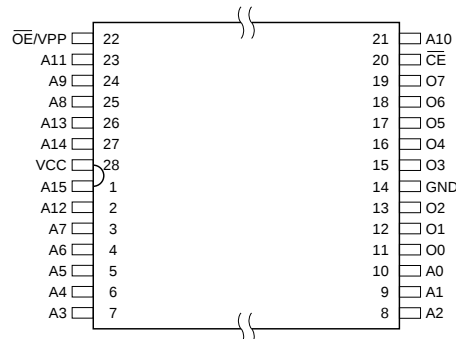


PLCC Top View



TSOP Top View

Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.



512K (64K x 8)
OTP EPROM

AT27C512R

Rev. 0015I-07/98



The AT27C512R is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

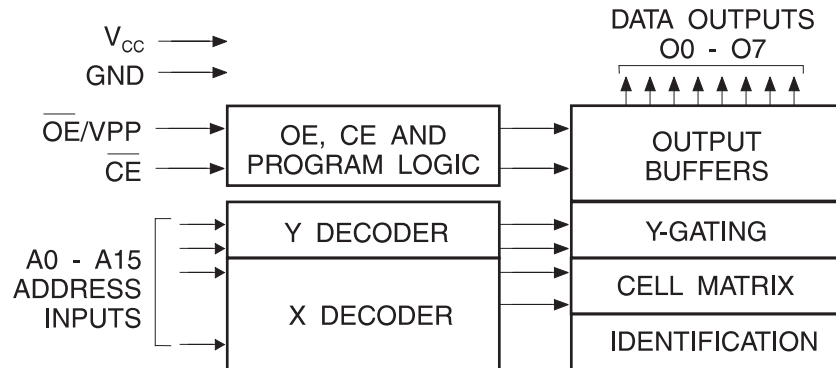
With 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μ F high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μ F bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to + 7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to + 14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground	-2.0V to + 14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

ModelPin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V _{IL}	V _{IL}	Ai	D _{OUT}
Output Disable	V _{IL}	V _{IH}	X ⁽¹⁾	High Z
Standby	V _{IH}	X ⁽¹⁾	X	High Z
Rapid Program ⁽²⁾	V _{IL}	V _{PP}	Ai	D _{IN}
PGM Inhibit	V _{IH}	V _{PP}	X ⁽¹⁾	High Z
Product Identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A15 = V _{IL}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to Programming Characteristics.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C512R					
		-45	-55	-70	-90	-12	-15
Operating Temp.(Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Auto.			-40°C - 125°C	-40°C - 125°C	-40°C - 125°C	-40°C - 125°C
V _{CC} Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}	Com., Ind,	±1	μA
			Auto.	±5	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}	Com., Ind,	±5	μA
			Auto.	±10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		1	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$		20	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

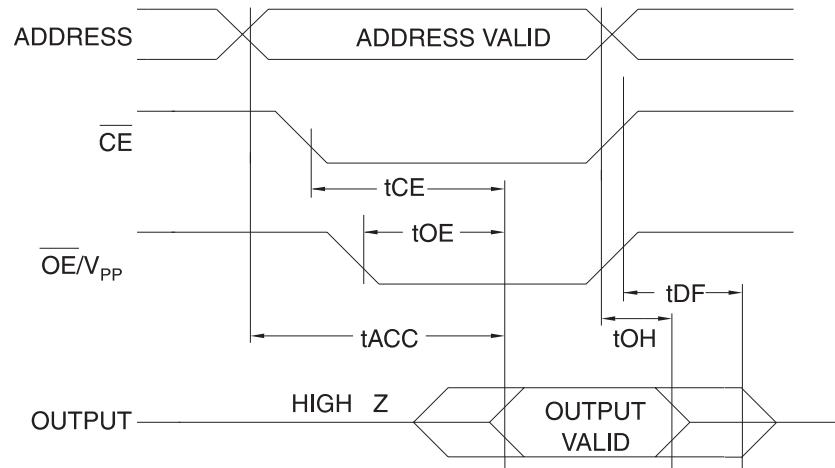
Notes: 1. V_{CC} must be applied simultaneously with or before $\overline{OE}/V_{PP}$ and removed simultaneously with or after $\overline{OE}/V_{PP}$.

AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C512R												Units
			-45		-55		-70		-90		-12		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACC} ⁽³⁾	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		45		55		70		90		120		150	ns
t _{CE} ⁽²⁾	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		45		55		70		90		120		150	ns
t _{OE} ⁽²⁾⁽³⁾	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$		20		25		30		35		35		40	ns
t _{DF} ⁽⁴⁾⁽⁵⁾	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		25		25		30		35	ns
t _{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ whichever occurred first		7		7		7		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

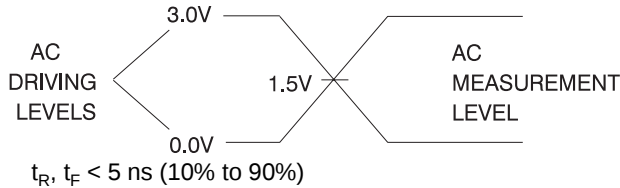
AC Waveforms for Read Operation⁽¹⁾



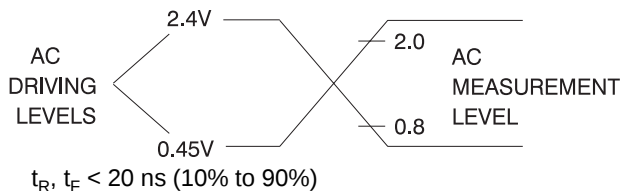
- Notes:
1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$. Timing measurement reference levels for all other speed grades are $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$. Input AC drive levels are $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$.
 2. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} .
 3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels

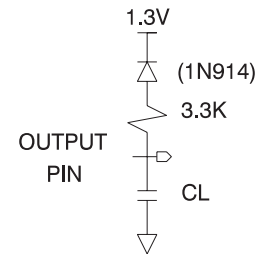
For -45 and -55 devices only:



For -70, -90, -12, -15, and -20 devices:



Output Test Load



Note: $C_L = 100$ pF including jig capacitance, except for the -45 and -55 devices, where $C_L = 30$ pF.

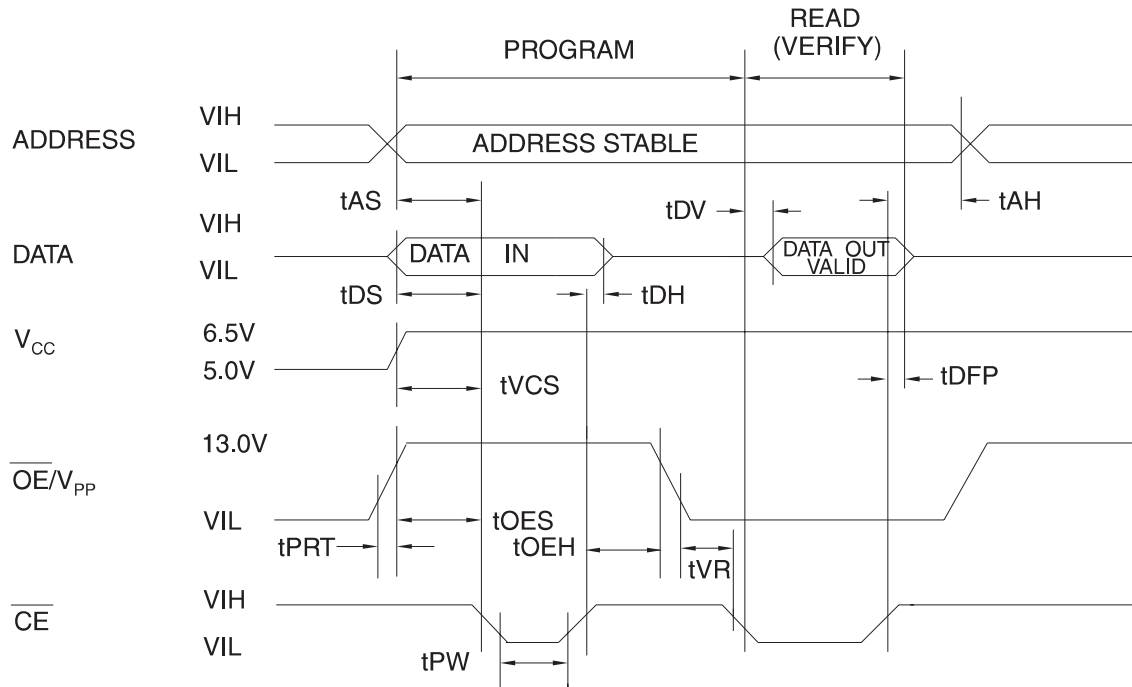
Pin Capacitance

($f = 1$ MHz $T = 25^\circ C$)⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms⁽¹⁾



- Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
 2. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, OE/V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I _{LI}	Input Load Current	V _{IN} = V _{IL} , V _{IH}		±10	μA
V _{IL}	Input Low Level		-0.6	0.8	V
V _{IH}	Input High Level		2.0	V _{CC} + 1	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V
I _{CC2}	V _{CC} Supply Current (Program and Verify)			25	mA
I _{PP2}	OE/V _{PP} Current	CE = V _{IL}		25	mA
V _{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns	2		μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		μs
t_{DS}	Data Setup Time		2		μs
t_{AH}	Address Hold Time	Input Pulse Levels 0.45V to 2.4V	0		μs
t_{DH}	Data Hold Time		2		μs
t_{DFP}	$\overline{CE}$ High to Output Float Delay ⁽²⁾	Input Timing Reference Level	0	130	ns
t_{VCS}	V_{CC} Setup Time	0.8V to 2.0V	2		μs
t_{PW}	$\overline{CE}$ Program Pulse Width ⁽³⁾	Output Timing Reference Level 0.8V to 2.0V	95	105	μs
t_{DV}	Data Valid from $\overline{CE}$ ⁽²⁾			1	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes:
- V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
 - Program Pulse width tolerance is $100 \mu\text{sec} \pm 5\%$.

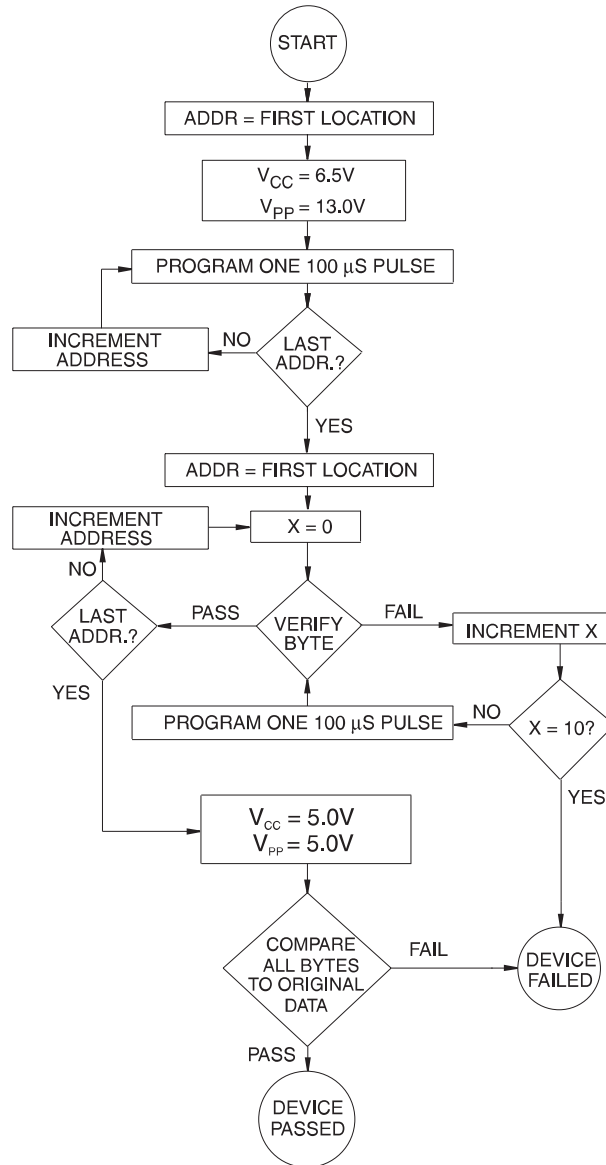
Atmel's 27C512R Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{\text{OE}}/V_{\text{PP}}$ is raised to 13.0V. Each address is first programmed with one 100 μs $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each

pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{\text{OE}}/V_{\text{PP}}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	20	0.1	AT27C512R-45JC	32J	Commercial (0°C to 70°C)
			AT27C512R-45PC	28P6	
			AT27C512R-45RC	28R	
			AT27C512R-45TC	28T	
	20	0.1	AT27C512R-45JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-45PI	28P6	
			AT27C512R-45RI	28R	
			AT27C512R-45TI	28T	
55	20	0.1	AT27C512R-55JC	32J	Commercial (0°C to 70°C)
			AT27C512R-55PC	28P6	
			AT27C512R-55RC	28R	
			AT27C512R-55TC	28T	
	20	0.1	AT27C512R-55JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-55PI	28P6	
			AT27C512R-55RI	28R	
			AT27C512R-55TI	28T	
70	20	0.1	AT27C512R-70JC	32J	Commercial (0°C to 70°C)
			AT27C512R-70PC	28P6	
			AT27C512R-70RC	28R	
			AT27C512R-70TC	28T	
	20	0.1	AT27C512R-70JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-70PI	28P6	
			AT27C512R-70RI	28R	
			AT27C512R-70TI	28T	
	20	0.1	AT27C512R-70JA	32J	Automotive (-40°C to 125°C)
			AT27C512R-70PA	28P6	
			AT27C512R-70RA	28R	

(continued)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-Lead, Thin Small Outline Package (TSOP)



Ordering Information (Continued)

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C512R-90JC	32J	Commercial (0°C to 70°C)
			AT27C512R-90PC	28P6	
			AT27C512R-90RC	28R	
			AT27C512R-90TC	28T	
	20	0.1	AT27C512R-90JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-90PI	28P6	
			AT27C512R-90RI	28R	
			AT27C512R-90TI	28T	
	20	0.1	AT27C512R-90JA	32J	Automotive (-40°C to 125°C)
			AT27C512R-90PA	28P6	
			AT27C512R-90RA	28R	
120	20	0.1	AT27C512R-12JC	32J	Commercial (0°C to 70°C)
			AT27C512R-12PC	28P6	
			AT27C512R-12RC	28R	
			AT27C512R-12TC	28T	
	20	0.1	AT27C512R-12JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-12PI	28P6	
			AT27C512R-12RI	28R	
			AT27C512R-12TI	28T	
	20	0.1	AT27C512R-12JA	32J	Automotive (-40°C to 125°C)
			AT27C512R-12PA	28P6	
			AT27C512R-12RA	28R	
150	20	0.1	AT27C512R-15JC	32J	Commercial (0°C to 70°C)
			AT27C512R-15PC	28P6	
			AT27C512R-15RC	28R	
			AT27C512R-15TC	28T	
	20	0.1	AT27C512R-15JI	32J	Industrial (-40°C to 85°C)
			AT27C512R-15PI	28P6	
			AT27C512R-15RI	28R	
			AT27C512R-15TI	28T	
	20	0.1	AT27C512R-15JA	32J	Automotive (-40°C to 125°C)
			AT27C512R-15PA	28P6	
			AT27C512R-15RA	28R	

Package Type	
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