

PRELIMINARY DATA SHEET

NEC

3 V SILICON RFIC FREQUENCY UPCONVERTER

UPC8106TB

FEATURES

- **RECOMMENDED OPERATING FREQUENCY:**
 $f_{RFout} = 0.4 \text{ GHz to } 2.0 \text{ GHz}$, $f_{IFin} = 100 \text{ MHz to } 400 \text{ MHz}$
- **SUPPLY VOLTAGE:**
 $V_{CC} = 2.7 \text{ to } 5.5 \text{ V}$
- **HIGH DENSITY SURFACE MOUNTING:**
 6 pin super mini mold package
- **LOW CURRENT CONSUMPTION:**
 $I_{CC} = 9 \text{ mA TYP @ } 3 \text{ V}$
- **LOW CARRIER LEAKAGE:**
 Due to double balanced mixer
- **BUILT-IN POWER SAVE FUNCTION**

DESCRIPTION

The UPC8106TB is a silicon monolithic integrated circuit designed as a frequency upconverter for cellular/cordless telephone transmitter stages, and features improved intermodulation. This device is housed in a 6 pin super mini mold package making it ideal for reducing system size. The UPC8106TB is manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses a silicon nitride passivation film and gold electrodes. These materials protect chip surfaces from external pollution and prevent corrosion/migration.

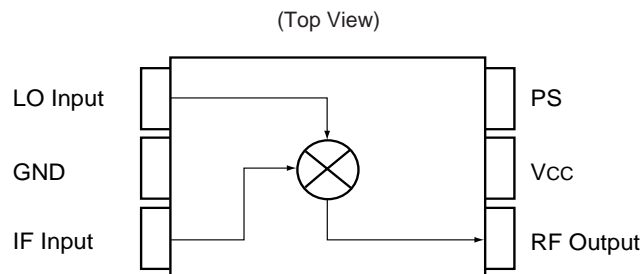
NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $V_{CC} = V_{RFout} = 3 \text{ V}$, $f_{IFin} = 240 \text{ MHz}$, $P_{LOin} = -5 \text{ dBm}$, $V_{PS} \geq 2.7 \text{ V}$ unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC8106TB S06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{CC}	Circuit Current at $V_{PS} \geq 2.7 \text{ V}$ $V_{PS} = 0 \text{ V}$	mA μA	4.5	9	13.5 10
CG	Conversion Gain at $f_{RFout} = 0.9 \text{ GHz}$, $P_{IFin} = -30 \text{ dBm}$ $f_{RFout} = 1.9 \text{ GHz}$, $P_{IFin} = -30 \text{ dBm}$	dB dB	6 4	9 7	12 10
PSAT	Maximum RF Output Power at $f_{RFout} = 0.9 \text{ GHz}$, $P_{IFin} = 0 \text{ dBm}$ $f_{RFout} = 1.9 \text{ GHz}$, $P_{IFin} = 0 \text{ dBm}$	dBm dBm	-4 -6.5	-2 -4	
OIP3	Output Third-Order Distortion Intercept Point at $f_{RFout} = 0.9 \text{ GHz}$, $f_{IFin1} = 240.0 \text{ MHz}$ $f_{RFout} = 1.9 \text{ GHz}$, $f_{IFin2} = 240.4 \text{ MHz}$	dBm dBm		+5.5 +2.0	
IM3	Third-Order Intermodulation Distortion at $f_{RFout} = 0.9 \text{ GHz}$, $f_{RFout} = 1.9 \text{ GHz}$	$f_{IFin1} = 240 \text{ MHz}$, $f_{IFin2} = 240.4 \text{ MHz}$, $P_{IFin} = -20 \text{ dBm}$		-31 -30	
SSBNF	SSB Noise Figure at $f_{RFout} = 0.9 \text{ GHz}$, $f_{IFin} = 240 \text{ MHz}$	dB		8.5	
TPS(RISE)	Power Save Rise Time at V_{PS} : GND→VCC	μS		2.0	
TPS(FALL)	Power Save Fall Time at V_{PS} : VCC→GND	μS		2.0	

INTERNAL BLOCK DIAGRAM



APPLICATION

- **CELLULAR/CORDLESS TELEPHONE**

ABSOLUTE MAXIMUM RATINGS¹ (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{CC}	Supply Voltage Pins 5 & 6	V	6.0
V _{PS}	Power Save Voltage	V	6.0
P _T	Total Power Dissipation ²	mW	200
T _{OP}	Operating Temperature	°C	-40 to +85
T _{STG}	Storage Temperature	°C	-55 to +150
P _{IN}	Input Power	dBm	+10

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB (T_A = +85°C).

RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V _{CC}	Supply Voltage ¹	V	2.7	3.0	5.5
T _{OP}	Operating Temperature	°C	-40	+25	+85
P _{LO}	LO Input Level ²	dBm	-10	-5	0
f _{RFout}	RF Output Frequency ³	GHz	0.4		2.5
f _{IFin}	IF Input Frequency	MHz	100		400

Notes:

1. The same voltage should be supplied to pin 5 and 6.
2. Z_s = 50 Ω (without matching).
3. With external matching circuit.

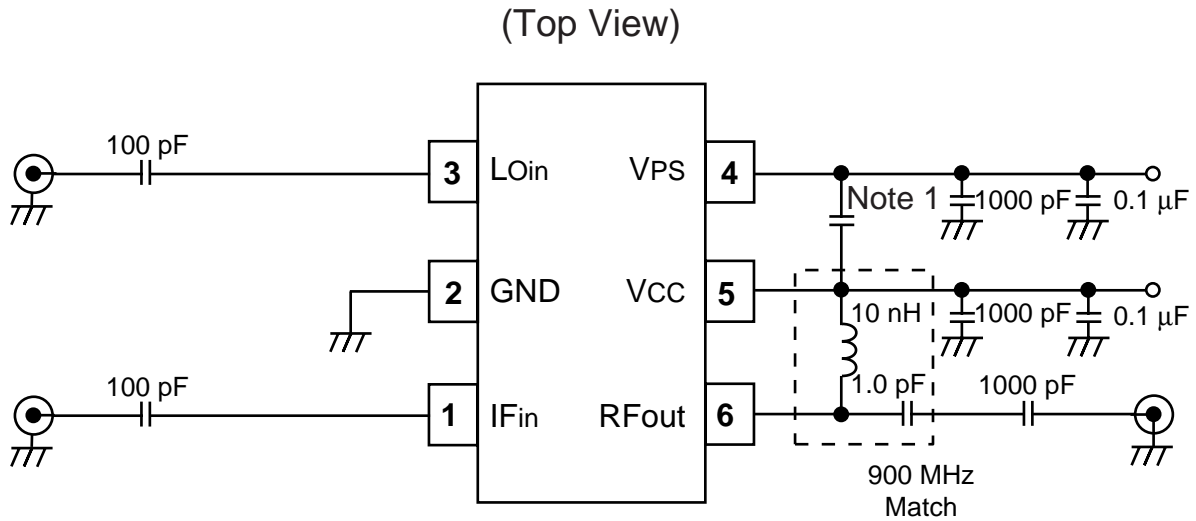
PIN FUNCTIONS

Pin No.	Symbol	Supply Voltage (V)	Pin ¹ Voltage (V)	Description	Equivalent Circuit						
1	IF Input	–	1.3	This pin is the IF input to the double balanced mixer. The input is a high impedance.							
2	GND	0	–	GND pin. Ground pattern on the board should be as wide as possible. Trace length should be kept as short as possible to minimize ground impedance.							
3	LOIN	–	2.4	LO input pin. Recommended input level is -10 to 0 dBm.							
5	V _{CC}	2.7 to 5.5	–	Supply voltage pin.							
6	RF Output	2.7 to 3.6	–	This pin is the RF output. This pin is designed as an open collector. Due to the high impedance output, this pin requires an external LC matching circuit.							
4	PS	V _{CC} /GND	–	Power save control pin. Bias controls operation as follows: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>Pin Bias</th> <th>Control</th> </tr> </thead> <tbody> <tr> <td>V_{CC}</td> <td>ON</td> </tr> <tr> <td>GND</td> <td>Power Save</td> </tr> </tbody> </table>	Pin Bias	Control	V _{CC}	ON	GND	Power Save	
Pin Bias	Control										
V _{CC}	ON										
GND	Power Save										

Note:

1. Each pin voltage is measured with V_{CC} = V_{PS} = V_{RFout} = 3.0 V

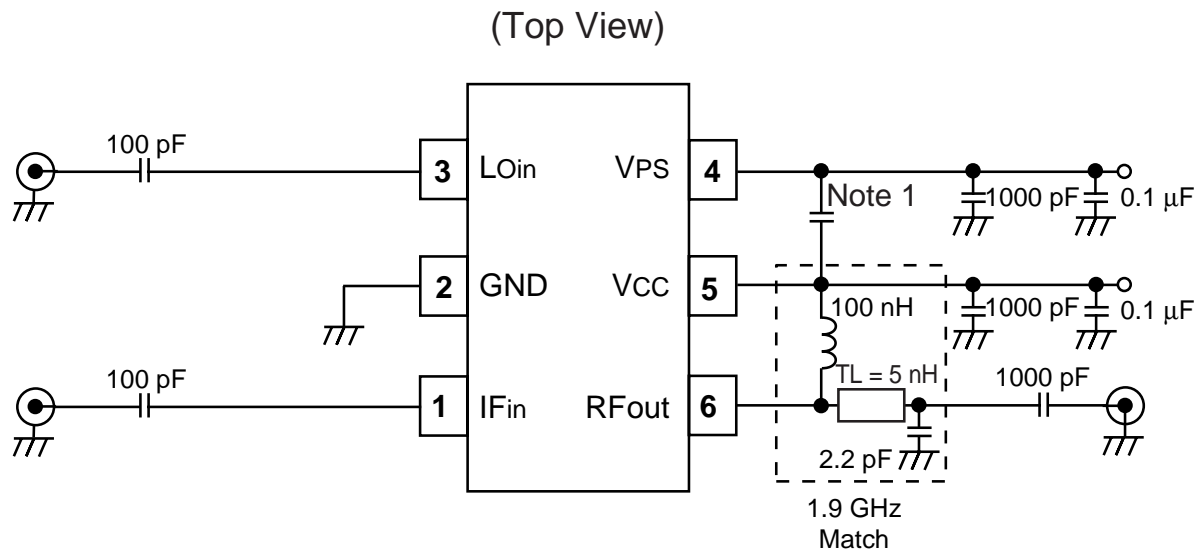
TEST CIRCUIT 1 (RF_{OUT} = 900 MHz)



Note:

1. In case of unstable operation, connect 100 pF capacitor between pins 4 and 5.

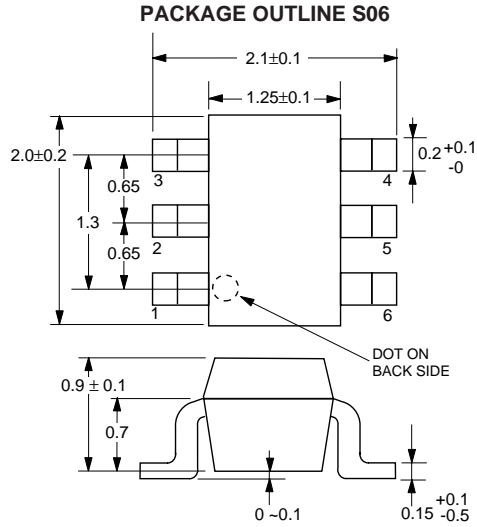
TEST CIRCUIT 2 (RF_{OUT} = 1.9 GHz)



Note:

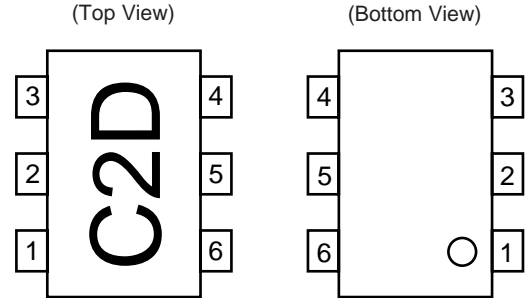
1. In case of unstable operation, connect 100 pF capacitor between pins 4 and 5.

OUTLINE DIMENSIONS (Units in mm)



Note:
All dimensions are typical unless otherwise specified.

LEAD CONNECTIONS



- 1. IF INPUT
- 2. GND
- 3. LO INPUT
- 4. POWER SAVE
- 5. Vcc
- 6. RF OUTPUT

ORDERING INFORMATION

PART NUMBER	QTY
UPC8106TB-E3	3K/Reel

Note:
Embossed Tape, 8 mm wide,
Pins 1, 2, and 3 face tape perforation side.

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