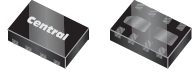


CTLDM304P-M832DS**SURFACE MOUNT
DUAL P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**

Top View Bottom View

TLM832DS CASEwww.centrasemi.com**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLDM304P-M832DS is a dual enhancement-mode P-Channel silicon MOSFET designed for high speed pulsed amplifier and driver applications. This energy efficient MOSFET offers beneficially low $r_{DS(ON)}$, low gate charge, and low threshold voltage.

MARKING CODE: C430**APPLICATIONS:**

- Switching circuits
- DC-DC converters
- Power management

FEATURES:

- Low $r_{DS(ON)}$
- High drain current
- Low gate charge

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage	
Gate-Source Voltage	
Continuous Drain Current (Steady State)	
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$	
Power Dissipation	
Operating and Storage Junction Temperature	
Thermal Resistance	

SYMBOL

V_{DS}	30
V_{GS}	12
I_D	4.2
I_{DM}	30
P_D	1.65
T_J, T_{stg}	-55 to +150
θ_{JA}	76

UNITS

V
V
A
A
W
$^\circ\text{C}$
$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=12\text{V}, V_{DS}=0$			100	nA
I_{DSS}	$V_{DS}=24\text{V}, V_{GS}=0$			1.0	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	30			V
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	0.7	1.0	1.3	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=4.2\text{A}$		60	70	$\text{m}\Omega$
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=4.0\text{A}$		64	75	$\text{m}\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=1.0\text{A}$		86	120	$\text{m}\Omega$
$Q_{g(tot)}$	$V_{DS}=15\text{V}, V_{GS}=4.5\text{V}, I_D=4.0\text{A}$		6.4		nC
Q_{gs}	$V_{DS}=15\text{V}, V_{GS}=4.5\text{V}, I_D=4.0\text{A}$		1.8		nC
Q_{gd}	$V_{DS}=15\text{V}, V_{GS}=4.5\text{V}, I_D=4.0\text{A}$		1.4		nC
C_{rss}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$		53		pF
C_{iss}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$		760		pF
C_{oss}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$		50		pF
t_{on}	$V_{DD}=15\text{V}, V_{GS}=10\text{V}, I_D=1.0\text{A}$				
	$R_L=3.6\Omega, R_G=6.0\Omega$		40		ns
t_{off}	$V_{DD}=15\text{V}, V_{GS}=10\text{V}, I_D=1.0\text{A}$				
	$R_L=3.6\Omega, R_G=6.0\Omega$		75		ns

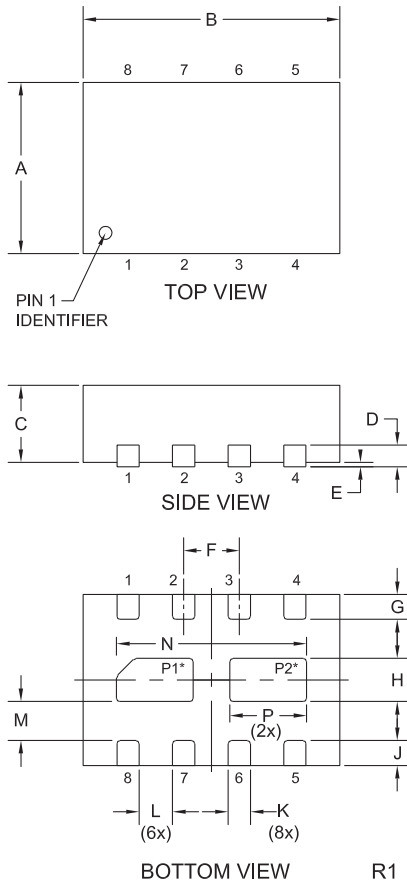
R1 (9-October 2012)

CTLDM304P-M832DS

SURFACE MOUNT
DUAL P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



TLM832DS CASE - MECHANICAL OUTLINE

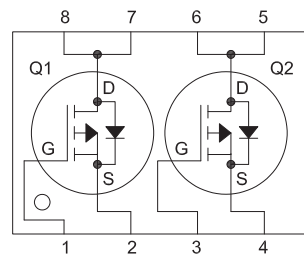


* Exposed pad P1 common to pins 7 and 8
Exposed pad P2 common to pins 5 and 6

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.077	0.081	1.95	2.05
B	0.116	0.120	2.95	3.05
C	0.031	0.039	0.80	1.00
D	0.006	0.010	0.16	0.25
E	0.000	0.002	0.00	0.05
F	0.026		0.65	
G	0.008	0.016	0.19	0.40
H	0.014	0.024	0.35	0.61
J	0.008	0.016	0.19	0.40
K	0.008	0.012	0.21	0.31
L	0.013	0.017	0.34	0.44
M	0.006	—	0.15	—
N	0.087		2.22	
P	0.029	0.039	0.74	1.00

TLM832DS (REV:R1)

PIN CONFIGURATION



LEAD CODE:

- | | |
|--------------|-------------|
| 1) Gate Q1 | 5) Drain Q2 |
| 2) Source Q1 | 6) Drain Q2 |
| 3) Gate Q2 | 7) Drain Q1 |
| 4) Source Q2 | 8) Drain Q1 |

MARKING CODE: C430

R1 (9-October 2012)

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