PI3EQX7701

5.0Gbps, 1-port, USB3.0 ReDriver™ with Digital Configuration

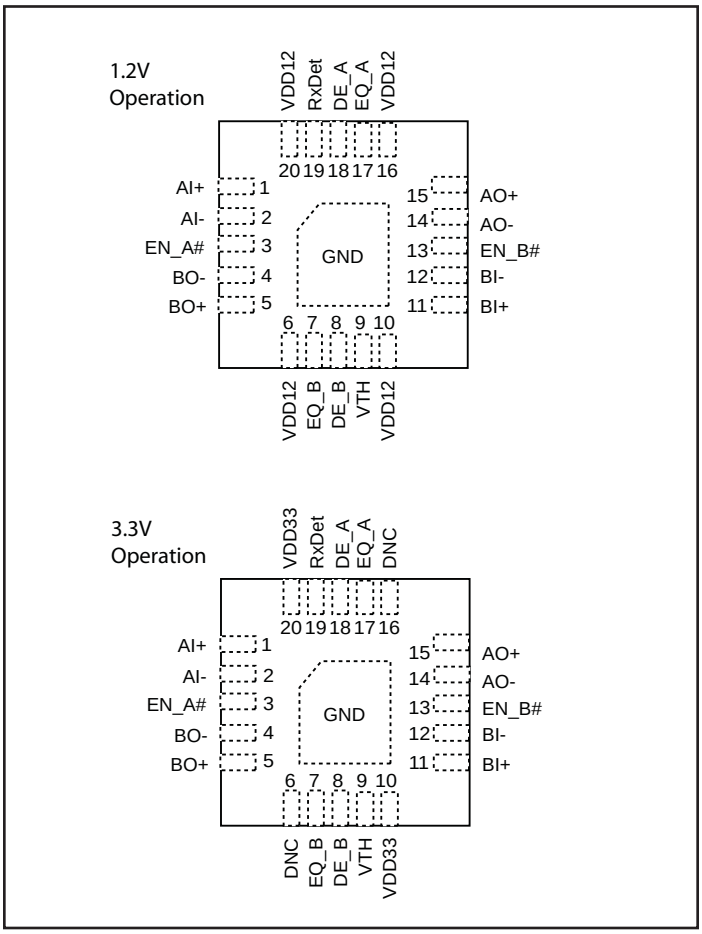
Features

- USB 3.0 compatible
- Two 5.0Gbps differential signal pairs
- Adjustable Receiver Equalization
- 100Ω Differential CML I/O's
- Pin Configured Output Emphasis Control
- Input signal level detect and squelch for each channel
- Automatic Receiver Detect with digital enable/disable
- Low Power (220mW) using 1.2V supply
- Auto "Slumber" mode for adaptive power management
- Stand-by Mode – Power Down State
- Single Supply Voltage: 1.2V or 3.3V(default)
- Packaging: 20-Contact TQFN (4x4mm)

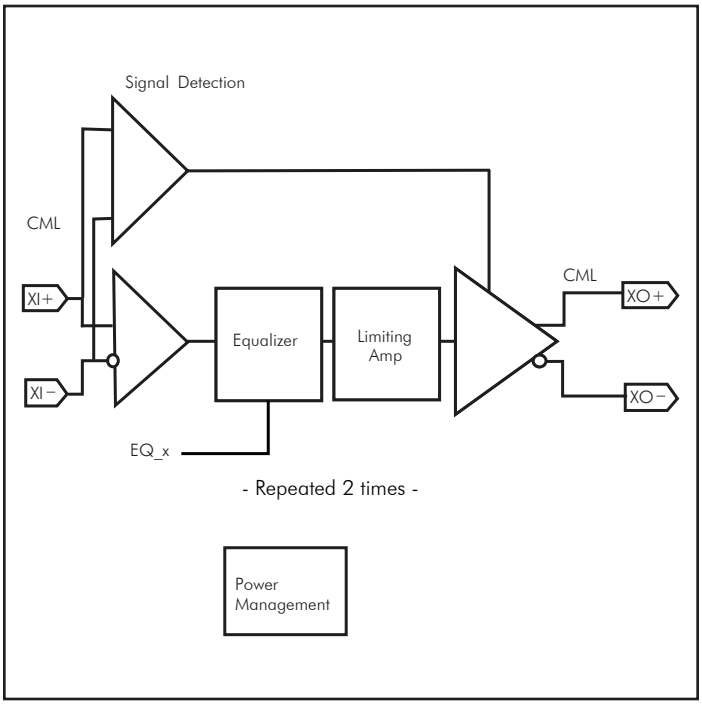
Description

Pericom Semiconductor's PI3EQX7701 is a low power, high performance 5.0 Gbps signal ReDriver™ designed specifically for the USB 3.0 protocol. The device provides programmable equalization, De-Emphasis, and input threshold controls to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX7701 supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform. The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (EN_x#) and operating, that channels' input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage. In addition to signal conditioning, when EN_x#, the device enters a low power standby mode. The PI3EQX7701 also includes a fully programmable receiver detect function. When the RxDet pin is pulled high, automatic receiver detection will be active. The receiver detection loop will be active again if either channel's signal detector is idle for longer than 1.3S. The device will then move to power down due to inactivity.

Pin Diagram (Top Side View)



Block Diagram



Pin Description

Pin #	Pin Name	Type	Description
17 7	EQ_A, EQ_B	Input	Set the equalization of two channels. “Low” means 6dB@2.5GHz and “high” means 12dB@2.5GHz. With internal 100kΩ pull-up resistor.
3	EN_A#	Input	Channel A Enable. “Low” Channel A is in normal operation. “High” Channel A is in power down mode. With internal 100kΩ pull-down resistor.
13	EN_B#	Input	Channel B Enable. “Low” Channel B is in normal operation. “High” Channel B is in power down mode. With internal 100kΩ pull-down resistor.
1 2 11 12	AI+ AI- BI+ BI-	Input	CML input channels. With Selectable input termination between 50Ω to GND and Hi-Z.
15 14 5 4	AO+ AO- BO+ BO-	Output	Selectable output termination between 50Ω to internal V_{bias} and 2kΩ to internal V_{bias}, and Hi-Z.
6 16	VDD12	Power	1.2V application. Do not connect for 3.3V supply voltage.
10 20	VDD33	Power	1.2V and 3.3V applications.
Center Pad	GND	GND	Supply Ground.
18 8	DE_A, DE_B	Input	Set the de-emphasis of the output CML buffer. “Low” means 0dB and “High” means –3.5dB. With internal 100kΩ pull-up resistor.
19	RxDet,	Input	Set the state of receiver detection of two channels. “Low” means no receiver detection and “high” means the receiver detection is active. With internal 100kΩ pull-up resistor.
9	VTH	Input	Set the threshold of two channels. “Low” means Vth=70mVppd and “high” means Vth=100mVppd. With internal 100kΩ pull-up resistor.

Adaptive Auto Power Down or "Slumber" Mode

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Pericom has added an additional adaptive auto power down feature. When a signal detector is idle for longer than 1.3s, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, it will send a wake-up signal to both channels. This results in both channels waking up and doing a receiver detection over again.

The device can also be forced into low power mode through the use of the EN_x# pins however this would require the use of GPIO pins to control.

Configuration Table

EN_x#	R_XDet	Function	Input R	Output R
1	X	Channel disable if both EN_A#, EN_B# are high, Chip Power Down	Hi-Z	Hi-Z
0	1	Chip and channel enabled, receiver detect is active	50Ω / Hi-Z*	50Ω / Hi-Z*
0	0	Chip and channel enabled, receiver detect is not active	50Ω	50Ω

* Refer to pin 19 description

Mode Adjustment

Equalization Setting:

EQ_A/B are the selection pins for the equalization selection for each direction.

Equalizer setting	
EQ_A/B	@ 2.5GHz
0	5 dB
1	11 dB (Default)

De-emphasis Setting:

DE_A/B are the selection pins for the de-emphasis selection for each direction.

Output de-emphasis setting	
DE_A/B	De-emphasis
0	0 dB
1	-3.5 dB (Default)

Threshold of Signal detector:

VTH are the selection pin to set the threshold of the signal detector.

The threshold setting of the signal detector	
VTH	Swing
0	70mVppd
1	100mVppd (Default)

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	–25mA to +25mA
Power Dissipation Continuous	1W
Operating Temperature	0 to +70°C
ESD, Human Body Model	–2kv to +2kV
ESD, Machine Model	–200V to +200V
ESD, Charged Device Model	–500V to +500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
1.2V Power Supply Characteristics (1)						
V_{DD12}	Power Supply Voltage		1.15		1.25	V
$P_{STANDBY12}$	Supply Power @1.2V Standby	EN_ [A:B]# = 1			5	mW
$P_{SLUMBER12}$	Supply Power @1.2V Slumber				36	
$P_{PARTIAL12}$	Supply Power @1.2V Partial	EN_x# = 0, $_{DIFFP-P} < V_{TH-SD}$		200		
$P_{ACTIVE12}$	Supply Power @1.2V Active	EN_x# = 0, $_{DIFFP-P} \geq V_{TH-SD}$			250	
$I_{DD-STANDBY12}$	Supply Current @1.2V Standby	EN_ [A:B]# = 1			4	mA
$I_{DD-SLUMBER12}$	Supply Current @1.2V Slumber				30	mA
$I_{DD-PARTIAL12}$	Supply Current @1.2V Partial	EN_x# = 0, $V_{RX-DIFFP-P} < V_{TH-SD}$		160		mA
$I_{DD-ACTIVE12}$	Supply Current @1.2V Active	EN_x# = 0, $V_{RX-DIFFP-P} \geq V_{TH-SD}$			210	
3.3V Power Supply Characteristics(1)						
V_{DD33}	Power Supply Voltage		3.0		3.6	V
$P_{STANDBY33}$	Supply Power @3.3V Standby	EN_ [A:B]# = 1			15	mW
$P_{SLUMBER33}$	Supply Power @3.3V Slumber				100	
$P_{PARTIAL33}$	Supply Power @3.3V Partial	EN_x# = 0, $_{DIFFP-P} < V_{TH-SD}$		525		
$P_{ACTIVE33}$	Supply Power @3.3V Active	EN_x# = 0, $_{DIFFP-P} \geq V_{TH-SD}$			700	
$I_{DD-STANDBY33}$	Supply Current @3.3V Standby	EN_ [A:B]# = 1			4	mA
$I_{DD-SLUMBER33}$	Supply Current @3.3V Slumber				30	mA
$I_{DD-PARTIAL33}$	Supply Current @3.3V Partial	EN_x# = 0, $V_{RX-DIFFP-P} < V_{TH-SD}$		160		mA
$I_{DD-ACTIVE33}$	Supply Current @3.3V Active	EN_x# = 0, $V_{RX-DIFFP-P} \geq V_{TH-SD}$			210	

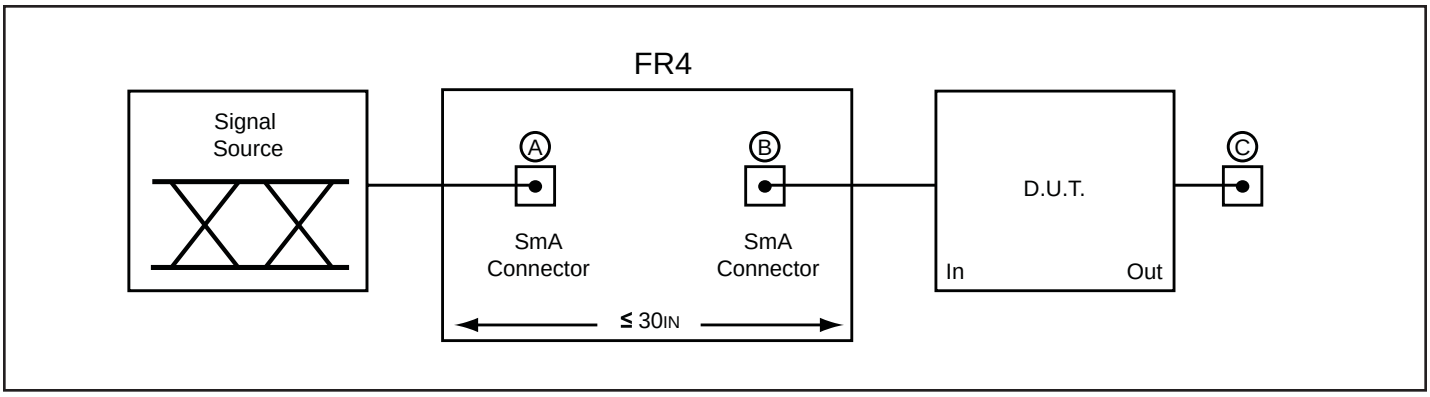
Note:
1. This device can operate from either 3.3V or 1.2V power supply. Note these different device pins are used for the different supply voltages. Performance characteristics are the same at either operating voltage.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PD}	Latency	From input to output		1	2	ns
CML Receiver Input						
Z_{RX-DC}	DC Input Impedance		40	50	60	Ω
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		120		1200	mV
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	
V_{TH-SD}	Signal detect Threshold	EN_x# = 0	65		175	mVppd
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p

Notes
1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.

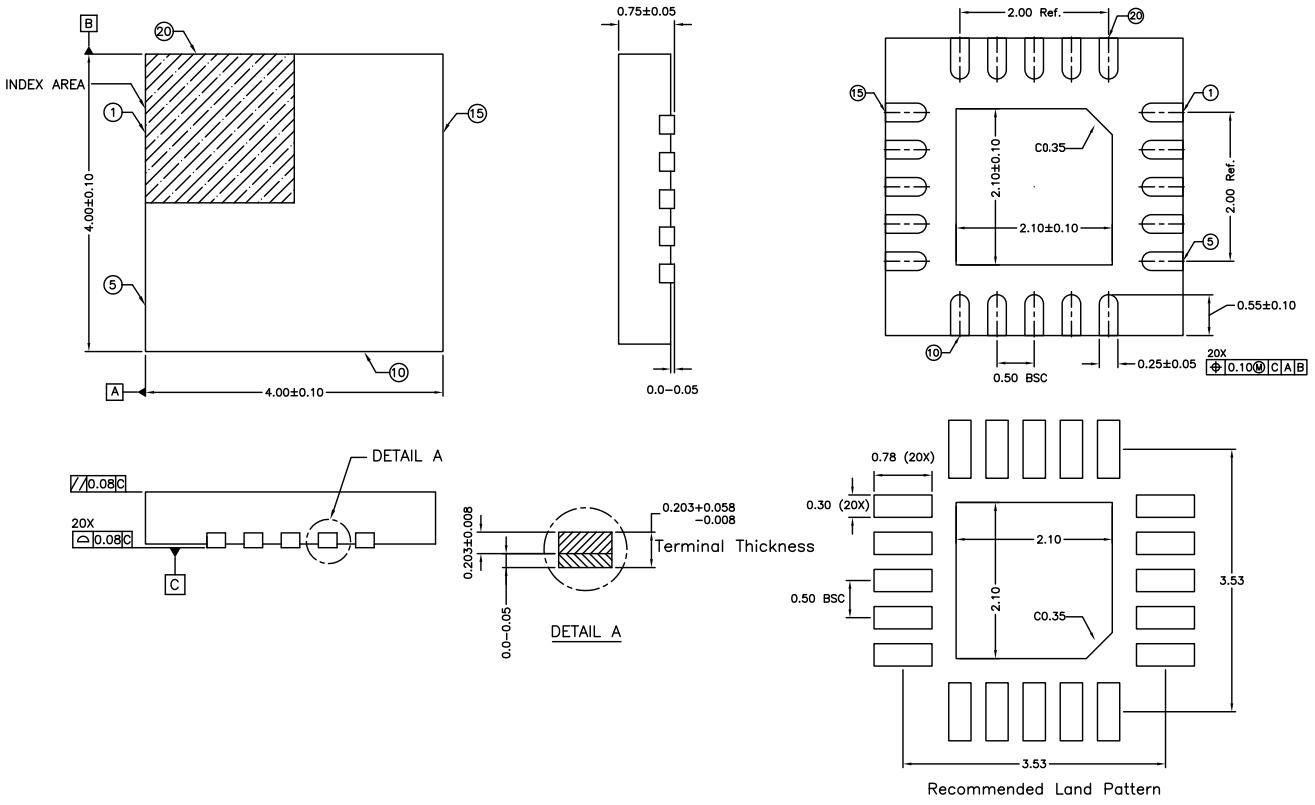
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)[1]						
Z_{OUT}	Output Resistance	Single-Ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	800		1200	mV
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	0.5		1.2	V
V_{cm_ac}	TX AC common mode voltage				100	mVpp
$V_{TX-Pre-Ratio-max}$	Max TX De-emphasis Level		-3		-4	dB
$C_{AC-coupling}$	AC coupling capacitor		75		200	nF
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				50	µA
I_{IL}	Input Low Current		-50			

Note:
1. Recommended output coupling capacitor is 75nF to 200nF (on each output)



Test Condition Referenced in the Electrical Characteristic Table

Packaging Mechanical: 20-contact TQFN (ZD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.08 mm.
4. REFER JEDEC MO–220.

PERICOM Semiconductor Corporation — DATE: 09/11/08

DESCRIPTION: 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD20

DOCUMENT CONTROL #: PD-2084 — REVISION: --

08-0456

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX7701ZDE	ZD	Pb-Free and Green 20-contact TQFN (4x4mm)

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel