

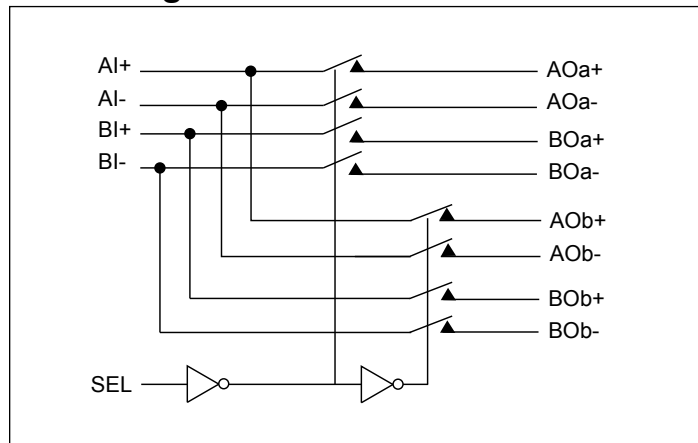
PI3PCIE2215

3.3V, PCI Express® 1-lane, 2:1 Mux/DeMux Switch

Features

- ➔ 2 Differential Channel, 2:1 Mux/DeMux
- ➔ PCI Express® 2.0 Performance, 5.0Gbps
- ➔ Pinout optimized for placement between two PCIe slots
- ➔ Bi-directional operation
- ➔ Low Bit-to-Bit Skew, 5ps max
- ➔ Low Crosstalk: -26dB@5 GHz
- ➔ Low Off Isolation: -20dB@5 GHz
- ➔ VDD Operating Range: +3.3V
- ➔ ESD Tolerance: 2kV HBM
- ➔ Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- ➔ Halogen and Antimony Free. "Green" Device (Note 3)
- ➔ For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- ➔ Packaging (Pb-free & Green):
 - 28 contact TQFN (ZH)

Block Diagram



Description

Diodes' PI3PCIE2215 is a 4 to 2 differential channel multiplexer/demultiplexer switch. The PI3PCIE family of switch solutions is fully compliant with PCIe® signals at 5.0Gbps. Due to its low bit-to-bit skew, high channel-to-channel noise isolation and high bandwidth, this product is ideal for PCI Express switching.

Application

Switch a PCI Express® lane output between two PCI Express lane inputs

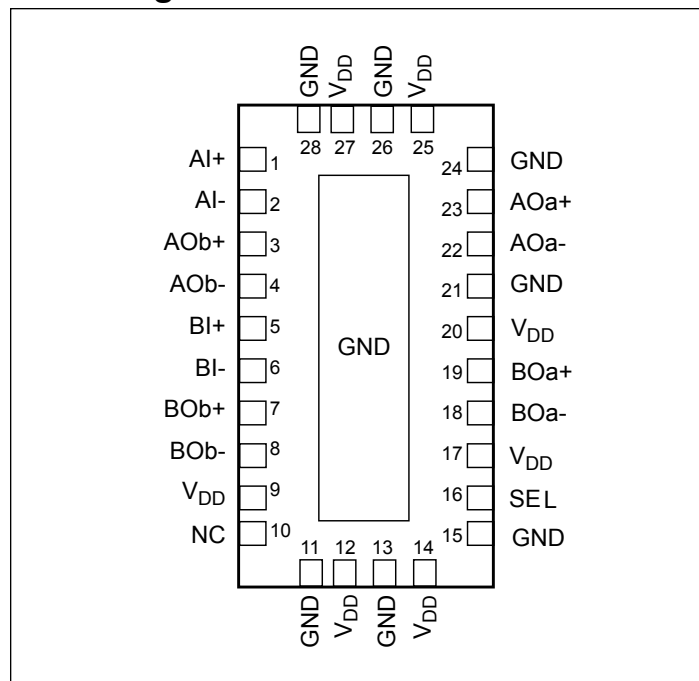
Truth Table

Function	SEL
xIy to xOay	L
xIy to xOby	H

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Descriptions

Pin Number	Pin Name	Type	Description
1 2	AI+ AI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through to the AOa+, AOa- pin respectively when SEL=0. Signal is passed through to the AOb+, AOb- pin respectively when SEL = 1.
23 22	AOa+ AOa-	Differential pass-through input	Differential analog pass-through output. Signal from AI+ and AI- is passed through AOa+ and AOa- respectively when SEL=0.
3 4	AOb+ AOb-	Differential pass-through input	Differential analog pass-through output. Signal from AI+ and AI- is passed through AOa+ and AOa- respectively when SEL=1.
5 6	BI+ BI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through to the BOa+, BOa- pin respectively when SEL=0. Signal is passed through to the BOb+, BOb- pin respectively when SEL = 1.
19 18	BOa+ BOa-	Differential pass-through input	Differential analog pass-through output. Signal from BI+ and BI- is passed through BOa+ and BOa- respectively when SEL=0.
7 8	BOb+ BOb-	Differential pass-through input	Differential analog pass-through output. Signal from BI+ and BI- is passed through BOb+ and BOb- respectively when SEL=1.
11, 13, 15, 21, 24, 26, 28, Center pad	GND	Ground input	Ground
10	NC	-	No Connect - Reserved, do not connect
16	SEL	3.6V tolerant low-voltage single-ended input	SEL controls the mux through a flow-through latch.
9, 12, 14, 17, 20, 25, 27	VDD	Power supply	Power, 3.3V $\pm$ 10%

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +4.6V
DC Input Voltage	-0.5V to 1.5V
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
V _{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I _{DD}	Total current from V _{DD} 3.3V supply		0		2.5	mA
T _{CASE}	Case temperature range for operation within spec.		-40		85	°C

DC Electrical Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min	Typ. ⁽¹⁾	Max	Units
V _{IH-SEL}	Input high level, SEL input		2.0		3.6	V
V _{IL-SEL}	Input Low Level, SEL input		0		0.8	V
I _{IN-SEL}	Input Leakage Current, SEL input	Measured with input at V _{IH-SEL} max and V _{IL-SEL} min	-10		10	μA
R _{ON}	On Resistance	V _{DD} = Min., V _{IN} = 1.3V, I _{IN} = 40mA			12	Ω
C _{ON}	On Channel Capacitance	V _{IN} = 0, V _{DD} = 3.3V		2.0		pF

Note:

1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics for xI±, xOy±

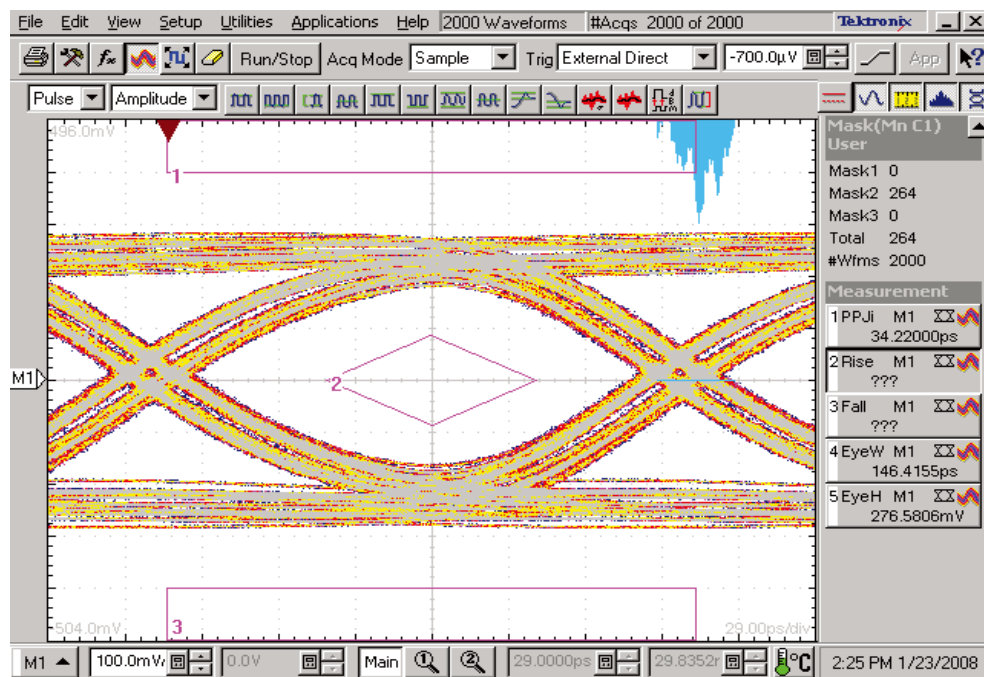
Parameter	Description	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
DDIL	Differential Insertion Loss	f=1.2GHz f=2.5GHz f=5.0GHz f=7.5GHz	-1.5 -2.0 -5.0 -9.0			dB
DDIL _{OFF}	Differential Off Isolation	f= 0 to 3.0GHz			-20.0	
DDRL	Differential Return Loss	f= 0 to 2.8GHz f= 2.8 to 5.0GHz f= 5.0 to 7.5GHz		-14.0 -8.0 -4.0		
DDNEXT	Near End Crosstalk	f= 0 to 2.5GHz f= 2.5 to 5.0GHz f= 5.0 to 7.5GHz			-32.0 -26.0 -20.0	

PI3PCIE2215

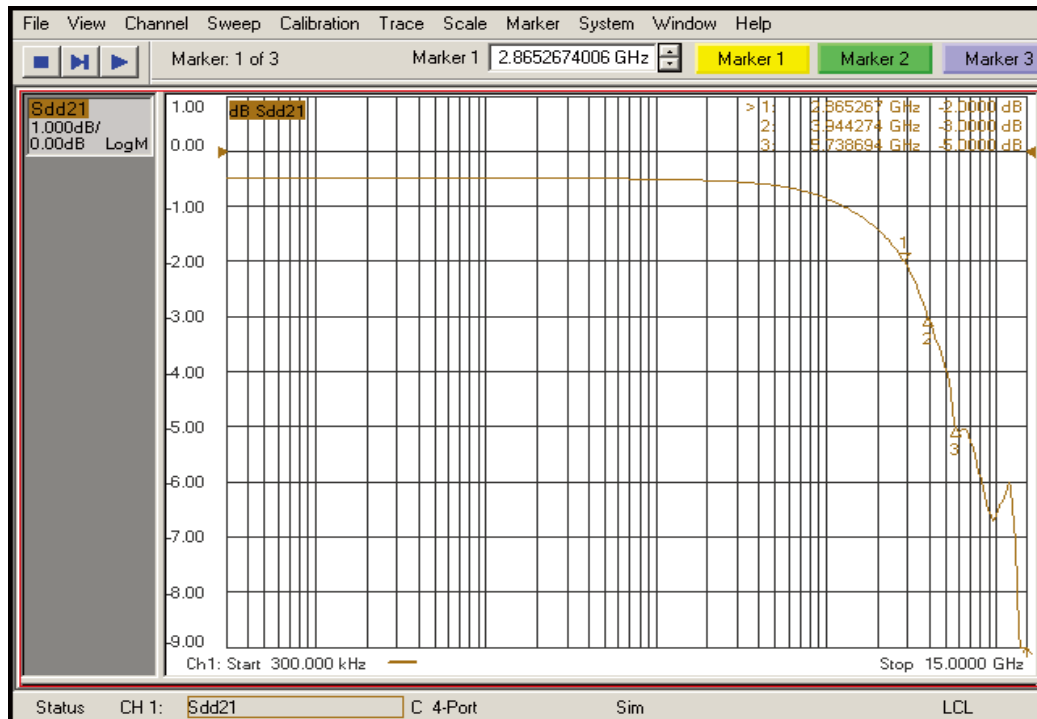
Switching Characteristics ($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH} , t_{PZL}	Line Enable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5		12.0	ns
t_{PHZ} , t_{PLZ}	Line Disable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5		12.0	ns
t_{b-b}	Bit-to-bit skew within the same differential pair	See "Test Circuit for Electrical Characteristics"			7	ps
t_{ch-ch}	Channel-to-channel skew	See "Test Circuit for Electrical Characteristics"			35	ps

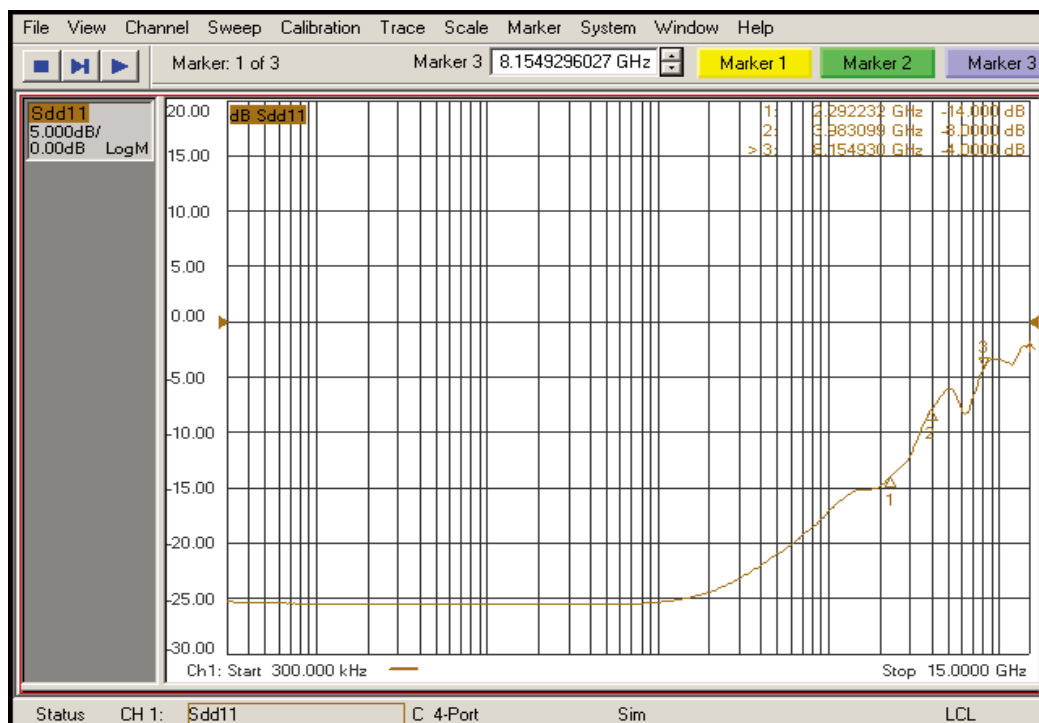
PI3PCIE2215



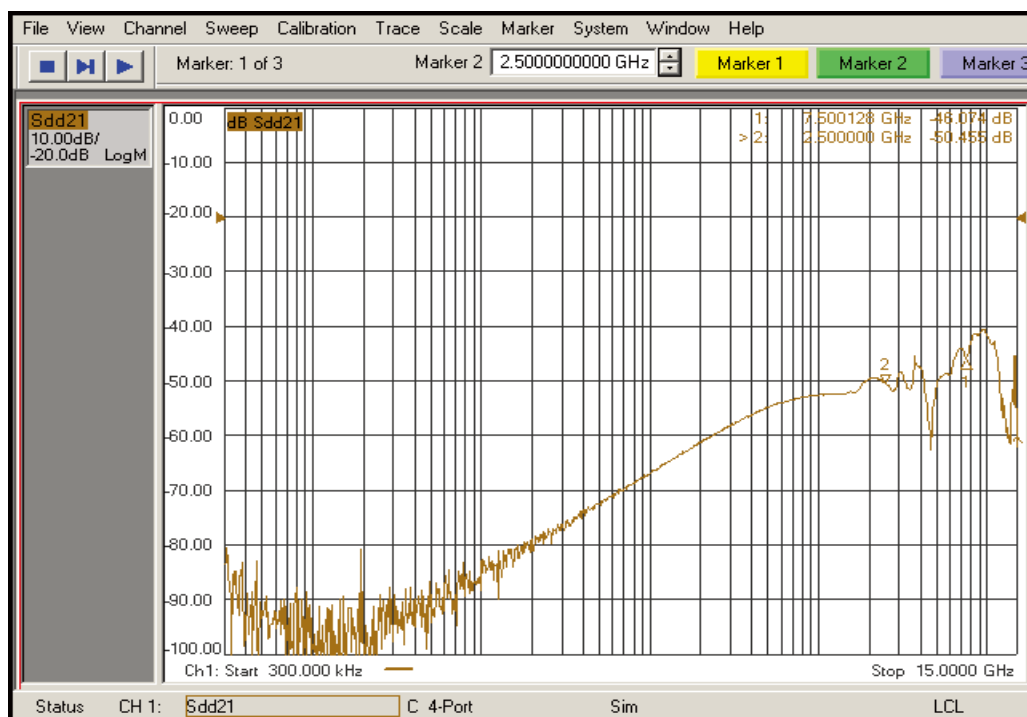
5.0 Gbps Receive Eye Mask (-3.5dB)



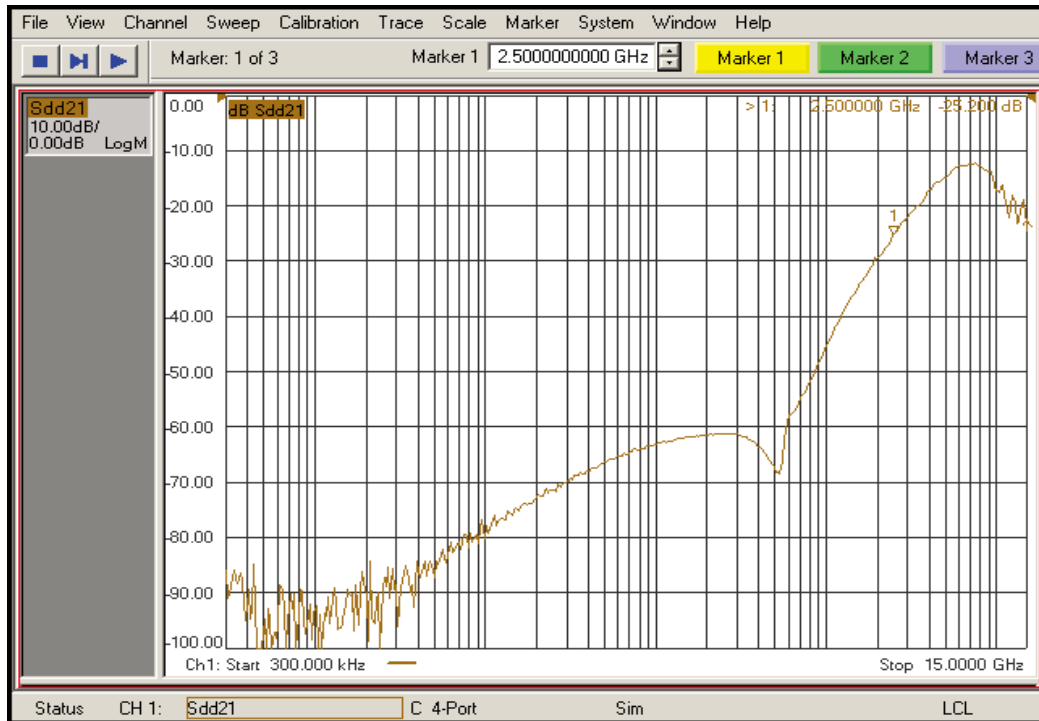
Differential Insertion Loss



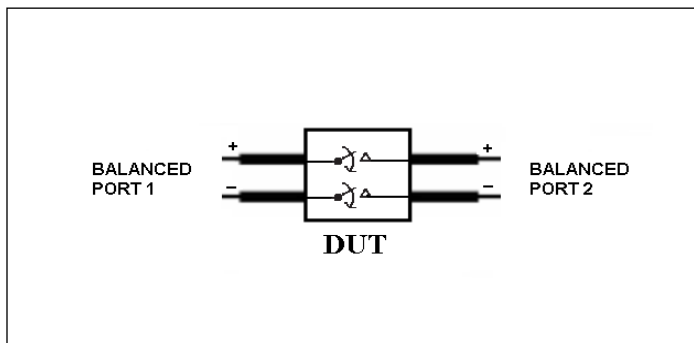
Differential Return Loss



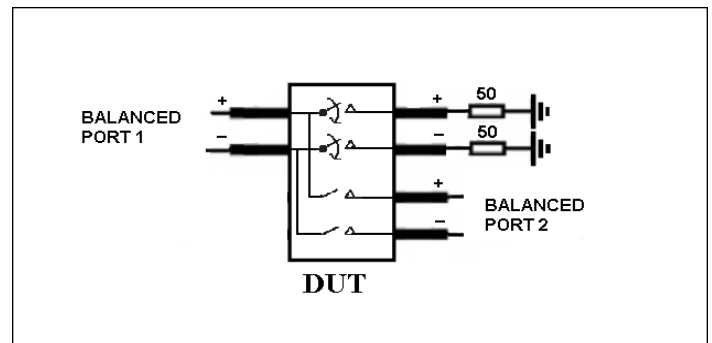
Differential Off Isolation



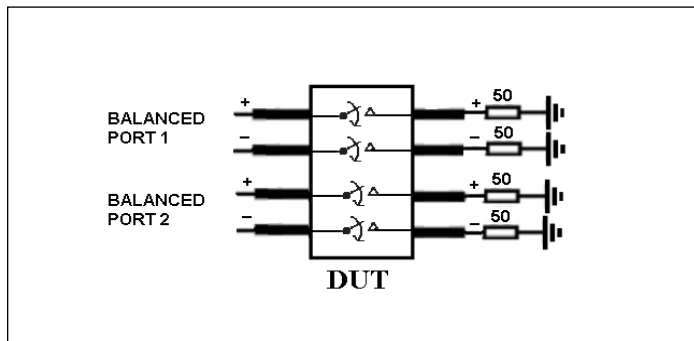
Differential Crosstalk



Differential Insertion Loss/Return Loss Test Circuit

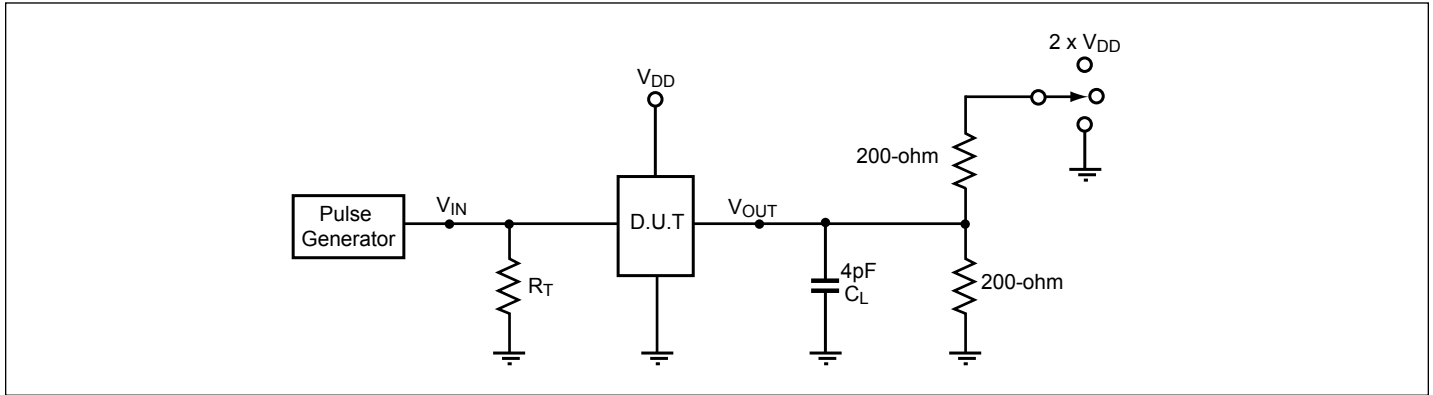


Differential Off Isolation Test Circuit



Differential Near End Crosstalk Test Circuit

Test Circuit for Electrical Characteristics⁽¹⁻⁵⁾



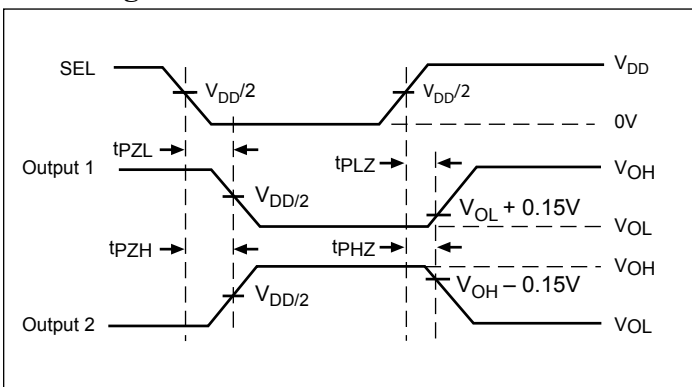
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ} , t_{PZL}	$2 \times V_{DD}$
t_{PHZ} , t_{PZH}	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Enable and Disable Times

PI3PCIE2215

Applications Information

Differential Inputs/Output Characteristics for Gen2 speeds

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	199.94	200.00	200.06	ps	Defined by Gen2 spec.
V _{RX-DIFFp-p}	Differential Input Peak to Peak Voltage	TBD		1.200	V	VRX-DIFFp-p = 2* VRX-D+ - VRX-D- . Applies to IN_S and RX_IN signals.
T _{RX-EYE}	Minimum Eye Width at IN_D input pair.	TBD			Tbit	
V _{CM-AC-pp}	AC Peak Common-Mode Input Voltage			100	mV	$V_{CM-AC-pp} = VRX-D+ + VRX-D- /2 - VRX-CM-DC$ $VRX-CM-DC = DC(aveg) \text{ of } VRX-D++VRX-D- /2$ VCM-AC-pp includes all frequencies above 30kHz.
Z _{RX-DIFF-DC}	DC Differential Input Impedance	80	100	120	W	Rx DC Differential Mode impedance
Z _{RX-DC}	DC Input Impedance	40	50	60	W	Required IN_D+ as well as IN_D-DC impedance (50 W +/- 20% tolerance). Includes mux resistance.
V _{RX-Bias}	Rx input termination voltage	0		2.0	V	Intended to limit power-up stress on PCIE output buffers.

Part Marking



YY: Year

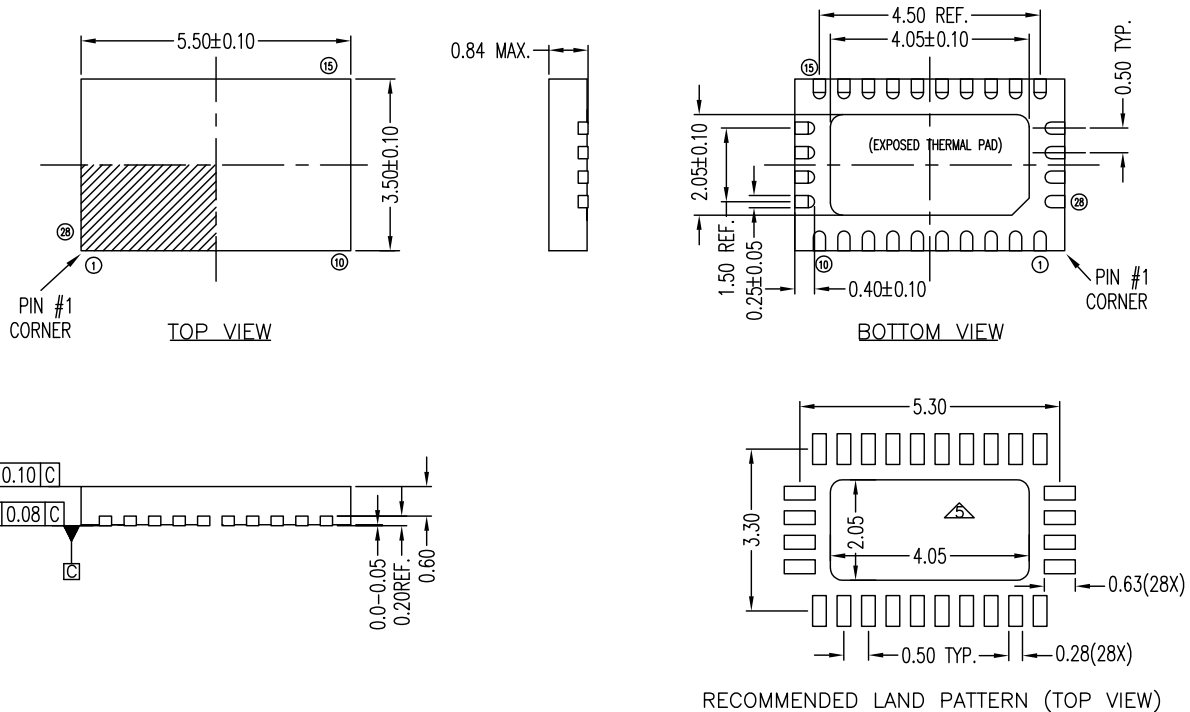
WW: Workweek

1st X: Assembly Code

2nd X: Fab Code

Bar above fab code means Cu wire

Packaging Mechanical: 28-TQFN (ZH)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).



DATE: 07/11/12

DESCRIPTION: 28-Contact, Very Thin Quad Flat No-Lead, TQFN

PACKAGE CODE: ZH28

DOCUMENT CONTROL #: PD-2034

REVISION: C

12-0419

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE2215ZHEX	ZH	28-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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