

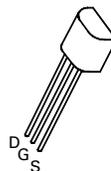
N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN0535A

ISSUE 2 – MARCH 94

FEATURES

- * 350 Volt V_{DS}
- * $R_{DS(on)}=50\Omega$



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

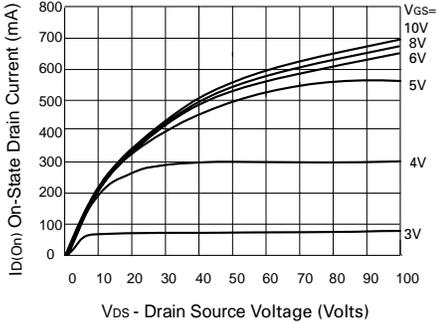
PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	350	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	90	mA
Pulsed Drain Current	I_{DM}	600	mA
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	700	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

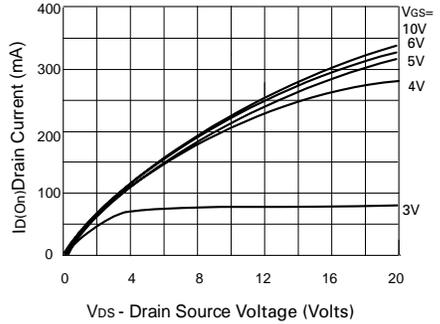
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	350		V	$I_D=1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	1	3	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		10 400	μA μA	$V_{DS}=350V, V_{GS}=0$ $V_{DS}=280V, V_{GS}=0V,$ $T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	150		mA	$V_{DS}=25V, V_{GS}=10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		50	Ω	$V_{GS}=10V, I_D=100mA$
Forward Transconductance(1)(2)	g_{fs}	100		mS	$V_{DS}=25V, I_D=100mA$
Input Capacitance (2)	C_{iss}		70	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	C_{oss}		10	pF	
Reverse Transfer Capacitance (2)	C_{rss}		4	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	$V_{DD}\approx 25V, I_D=100mA$
Rise Time (2)(3)	t_r		7	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		16	ns	
Fall Time (2)(3)	t_f		10	ns	

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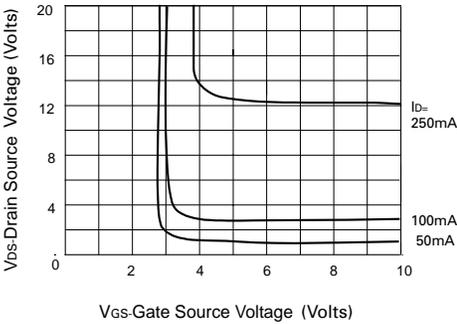
TYPICAL CHARACTERISTICS



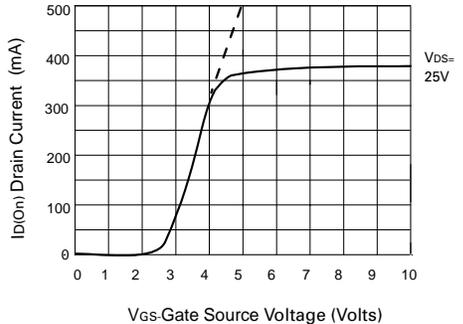
Output Characteristics



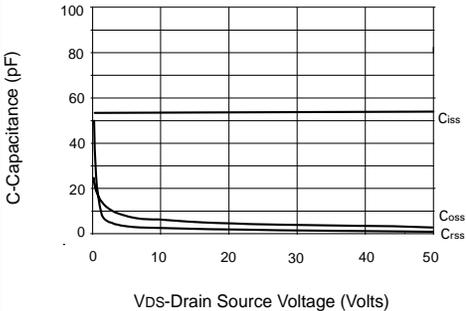
Saturation Characteristics



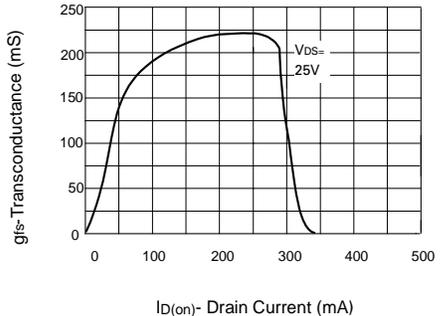
Voltage Saturation Characteristics



Transfer Characteristics

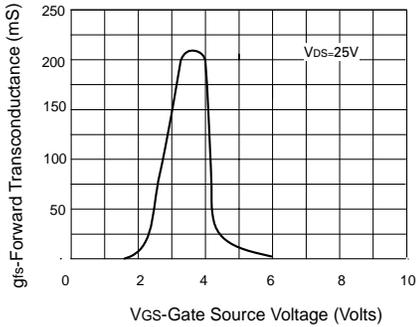


Capacitance v drain-source voltage

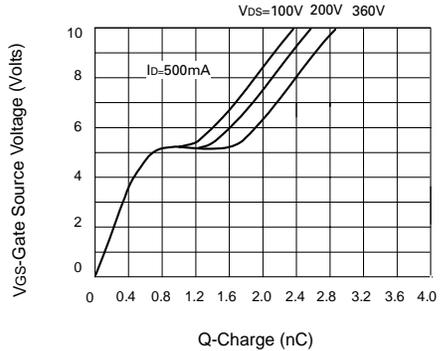


Transconductance v drain current

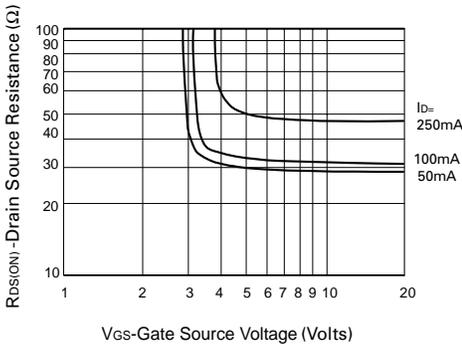
TYPICAL CHARACTERISTICS



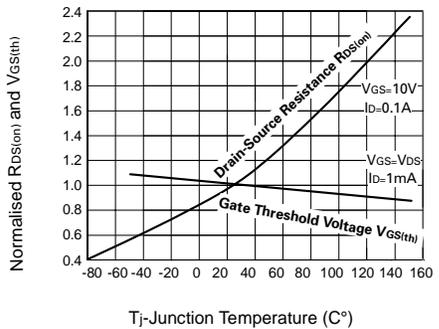
Transconductance v gate-source voltage



Gate charge v gate-source voltage



On-resistance vs gate-source voltage



Normalised $R_{DS(on)}$ and $V_{GS(th)}$ vs Temperature