

# EH3500TTS-106.250M TR



## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) HCMOS/TTL (CMOS) 5.0Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 106.250MHz  $\pm$ 100ppm 0°C to +70°C

## ELECTRICAL SPECIFICATIONS

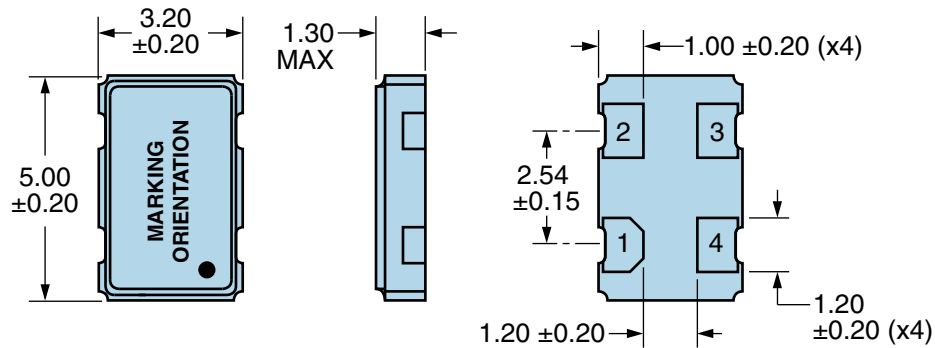
Nominal Frequency	106.250MHz
Frequency Tolerance/Stability	$\pm$ 100ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)
Aging at 25°C	$\pm$ 5ppm/year Maximum
Operating Temperature Range	0°C to +70°C
Supply Voltage	5.0Vdc $\pm$ 10%
Input Current	50mA Maximum (No Load)
Output Voltage Logic High (Voh)	2.4Vdc Minimum with TTL Load, Vdd-0.4Vdc Minimum with HCMOS Load (IOH = -16mA)
Output Voltage Logic Low (Vol)	0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA)
Rise/Fall Time	4nSec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load)
Duty Cycle	50 $\pm$ 5(%) (Measured at 50% of waveform with TTL Load or with HCMOS Load)
Load Drive Capability	5TTL Load or 15pF HCMOS Load Maximum
Output Logic Type	CMOS
Pin 1 Connection	Tri-State (Disabled Output: High Impedance)
Tri-State Input Voltage (Vih and Vil)	+2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output.
Absolute Clock Jitter	$\pm$ 250pSec Maximum, $\pm$ 100pSec Typical
One Sigma Clock Period Jitter	$\pm$ 50pSec Maximum, $\pm$ 30pSec Typical
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-202, Method 213, Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007, Condition A

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## MECHANICAL DIMENSIONS (all dimensions in millimeters)

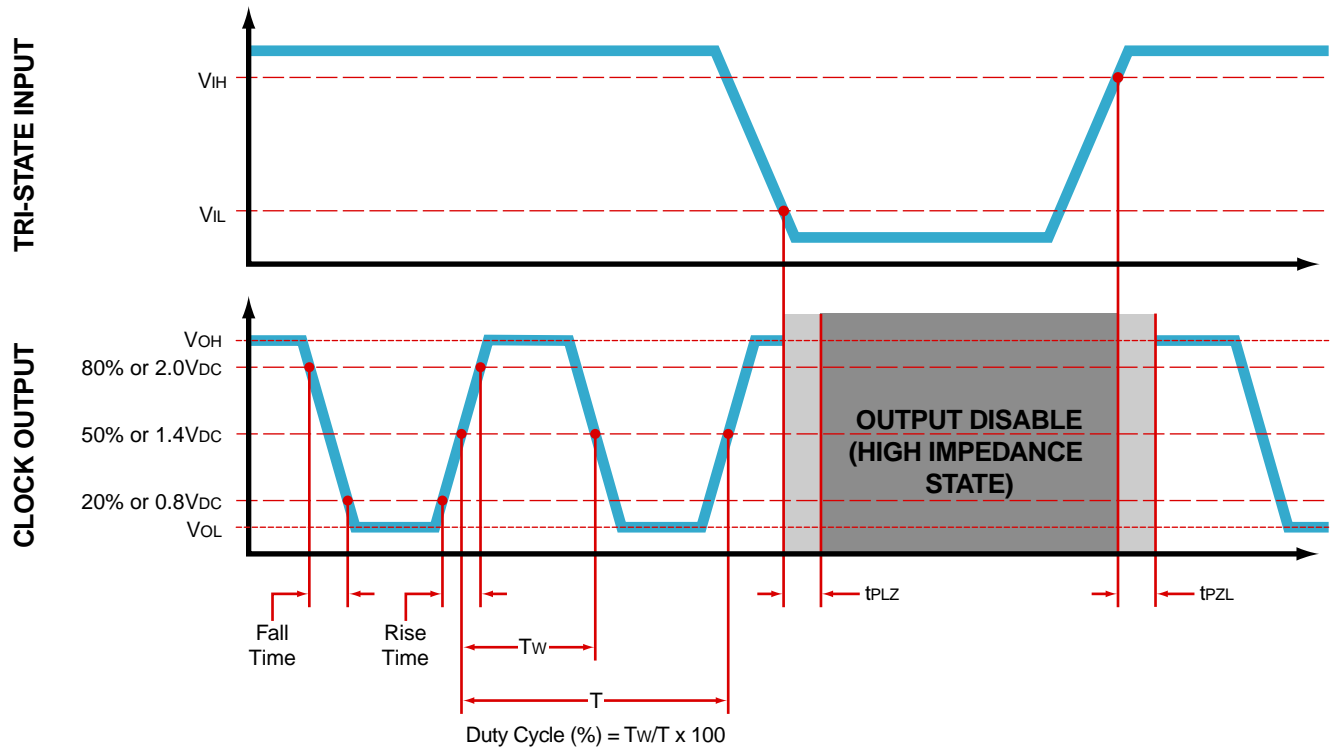


PIN	CONNECTION
1	Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	<b>E106.25</b> <i>E=Ecliptek Designator</i>
2	<b>XXXXX</b> <i>XXXXX=Ecliptek Manufacturing Identifier</i>

# EH3500TTS-106.250M TR [↗](#)

## OUTPUT WAVEFORM & TIMING DIAGRAM

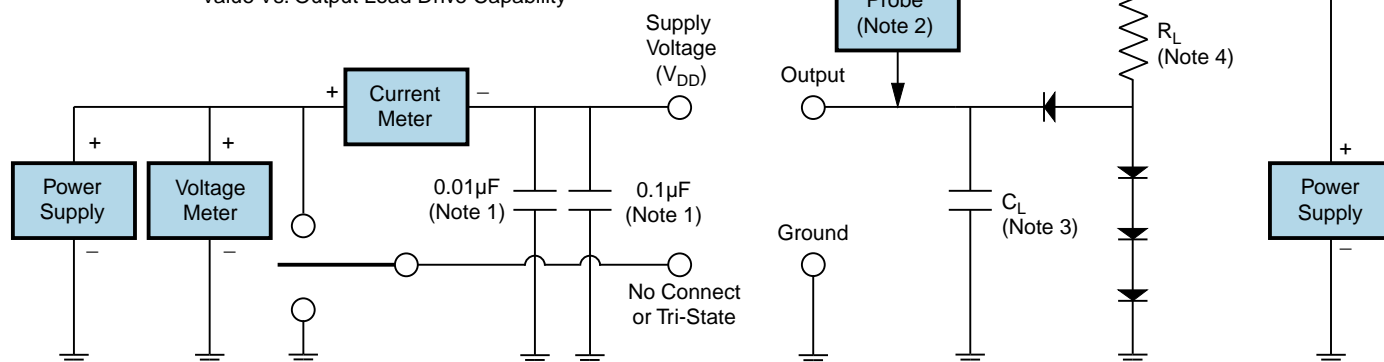


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## Test Circuit for TTL Output

Output Load Drive Capability	$R_L$ Value (Ohms)	$C_L$ Value (pF)
10TTL	390	15
5TTL	780	15
2TTL	1100	6
10LSTTL	2000	15
1TTL	2200	3

Table 1:  $R_L$  Resistance Value and  $C_L$  Capacitance Value Vs. Output Load Drive Capability



Note 1: An external 0.1 $\mu$ F low frequency tantalum bypass capacitor in parallel with a 0.01 $\mu$ F high frequency ceramic bypass capacitor close to the package ground and V<sub>DD</sub> pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

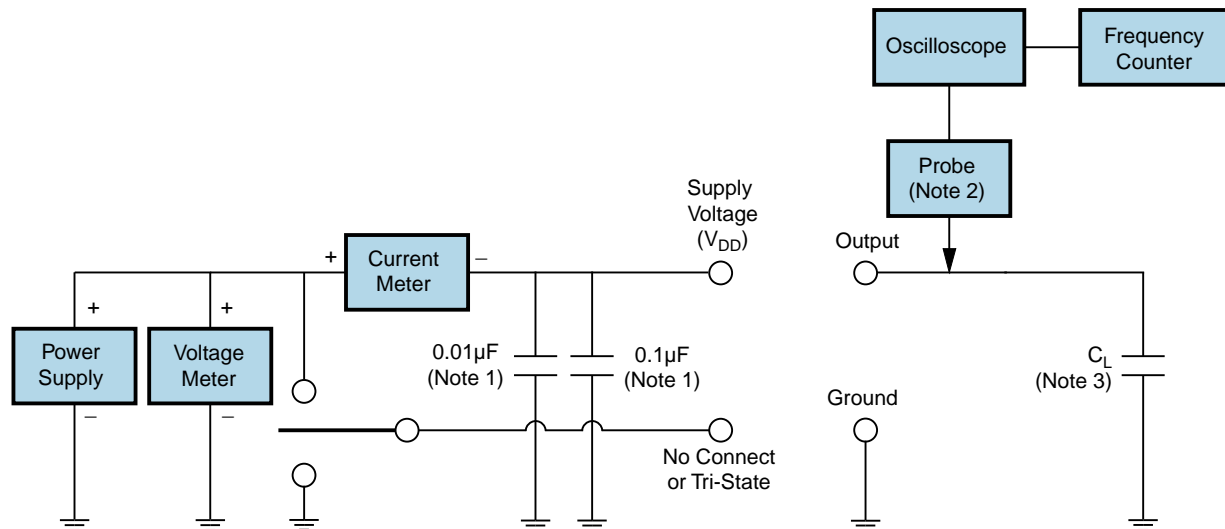
Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.

Note 4: Resistance value  $R_L$  is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.

Note 5: All diodes are MMBD7000, MMBD914, or equivalent.

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## Test Circuit for CMOS Output



Note 1: An external  $0.1\mu\text{F}$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu\text{F}$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.

Note 2: A low capacitance ( $<12\text{pF}$ ), 10X attenuation factor, high impedance ( $>10\text{Mohms}$ ), and high bandwidth ( $>300\text{MHz}$ ) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.