

# EH3600TTS-24.576M TR [↗](#)

<b>Lead Free</b>  <b>COMPLIANT</b>	<b>EU RoHS</b> 2011/65 + 2015/863 <b>COMPLIANT</b>	<b>ChinaRoHS</b>  <b>COMPLIANT</b>	<b>REACH</b> <b>SVHC 163</b> Jun 15, 2015 <b>COMPLIANT</b>
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## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 24.576MHz ±100ppm 0°C to +70°C

## ELECTRICAL SPECIFICATIONS

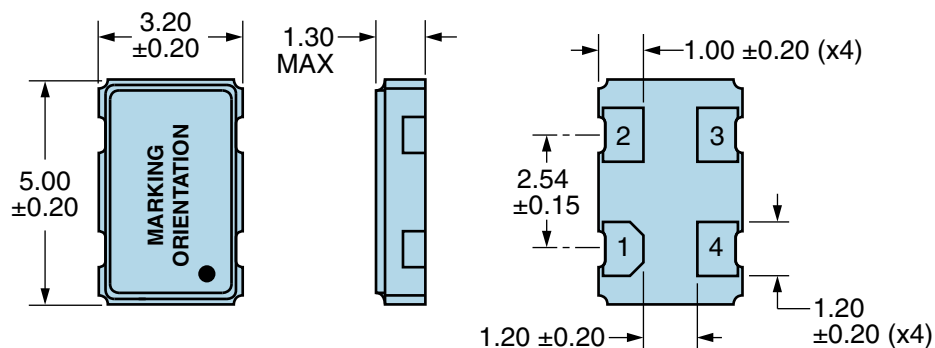
<b>Nominal Frequency</b>	24.576MHz
<b>Frequency Tolerance/Stability</b>	±100ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
<b>Aging at 25°C</b>	±5ppm/year Maximum
<b>Operating Temperature Range</b>	0°C to +70°C
<b>Supply Voltage</b>	3.3Vdc ±10%
<b>Input Current</b>	35mA Maximum (No Load)
<b>Output Voltage Logic High (Voh)</b>	2.7Vdc Minimum (IOH = -8mA)
<b>Output Voltage Logic Low (Vol)</b>	0.5Vdc Maximum (IOL = +8mA)
<b>Rise/Fall Time</b>	6nSec Maximum (Measured at 20% to 80% of waveform)
<b>Duty Cycle</b>	50 ±5(%) (Measured at 50% of waveform)
<b>Load Drive Capability</b>	30pF Maximum
<b>Output Logic Type</b>	CMOS
<b>Pin 1 Connection</b>	Tri-State (High Impedance)
<b>Tri-State Input Voltage (Vih and Vil)</b>	70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.
<b>Absolute Clock Jitter</b>	±250pSec Maximum, ±100pSec Typical
<b>One Sigma Clock Period Jitter</b>	±50pSec Maximum, ±40pSec Typical
<b>Start Up Time</b>	10mSec Maximum
<b>Storage Temperature Range</b>	-55°C to +125°C

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

<b>Fine Leak Test</b>	MIL-STD-883, Method 1014, Condition A
<b>Gross Leak Test</b>	MIL-STD-883, Method 1014, Condition C
<b>Mechanical Shock</b>	MIL-STD-202, Method 213, Condition C
<b>Resistance to Soldering Heat</b>	MIL-STD-202, Method 210
<b>Resistance to Solvents</b>	MIL-STD-202, Method 215
<b>Solderability</b>	MIL-STD-883, Method 2003
<b>Temperature Cycling</b>	MIL-STD-883, Method 1010
<b>Vibration</b>	MIL-STD-883, Method 2007, Condition A

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## MECHANICAL DIMENSIONS (all dimensions in millimeters)

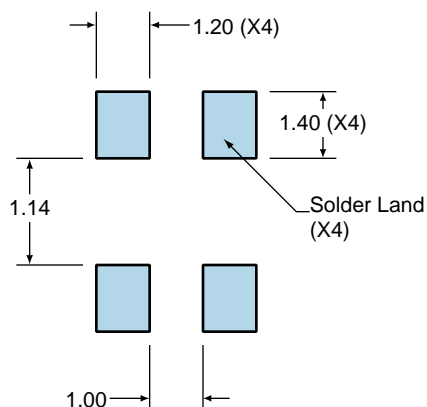


PIN	CONNECTION
1	Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	<b>E24.576</b> E=Ecliptek Designator
2	<b>XXXXX</b> XXXXX=Ecliptek Manufacturing Identifier

## Suggested Solder Pad Layout

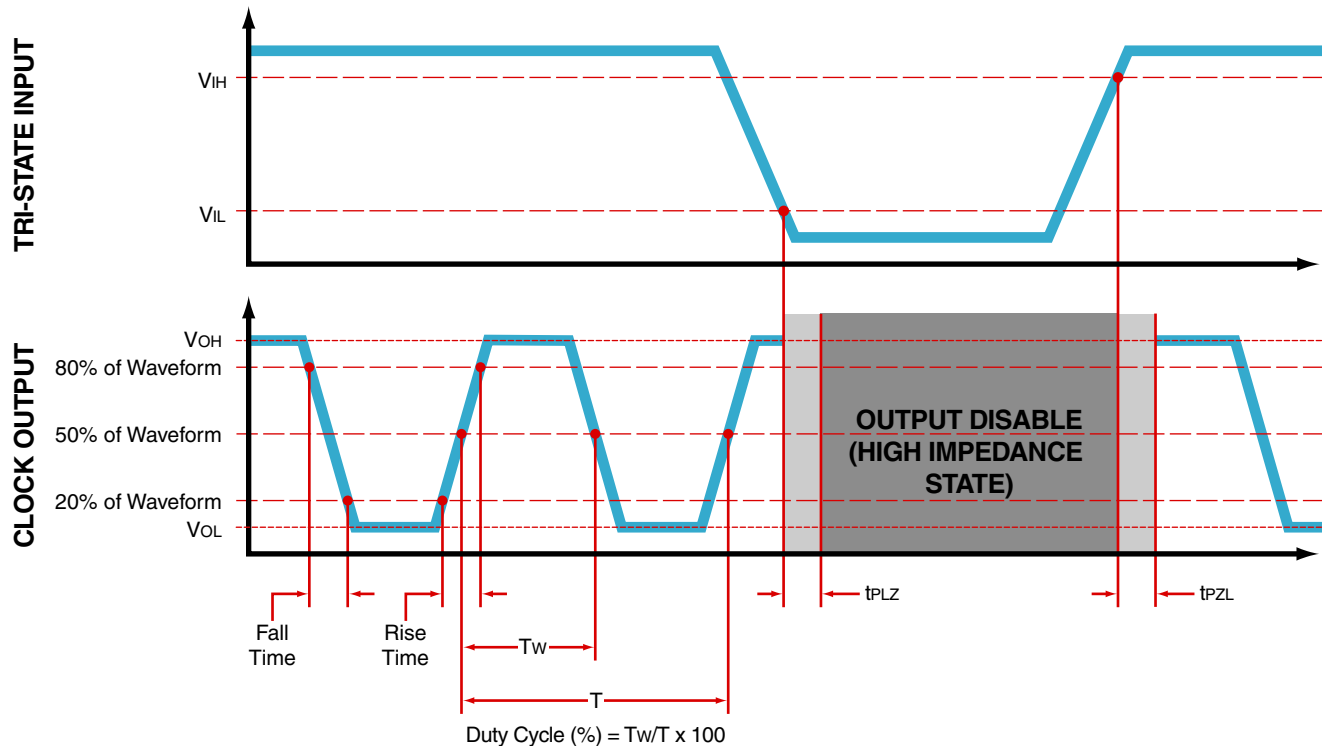
All Dimensions in Millimeters



All Tolerances are  $\pm 0.1$

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## OUTPUT WAVEFORM & TIMING DIAGRAM



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## Test Circuit for CMOS Output



Note 1: An external  $0.1\mu\text{F}$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu\text{F}$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.

Note 2: A low capacitance ( $<12\text{pF}$ ), 10X attenuation factor, high impedance ( $>10\text{Mohms}$ ), and high bandwidth ( $>300\text{MHz}$ ) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.

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## Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

All Dimensions in Millimeters

Compliant to EIA-481

