

# EH3625ETTS-2.048M TR

[Click part number to visit Part Number Details page](#)

## REGULATORY COMPLIANCE (Data Sheet downloaded on Apr 27, 2017)


[Click badges to download compliance docs](#)

Regulatory Compliance standards are subject to updates by governing bodies. Click the badges to download the latest compliance docs for this part number directly from Ecliptek.



## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 2.048MHz  $\pm 25$ ppm -40°C to +85°C

## ELECTRICAL SPECIFICATIONS

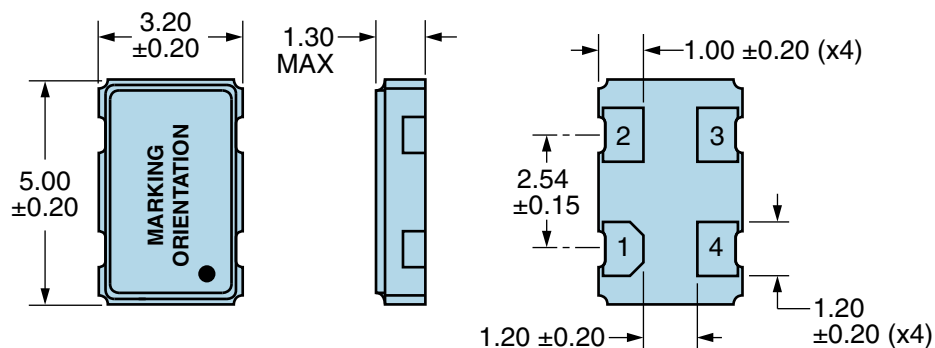
Nominal Frequency	2.048MHz
Frequency Tolerance/Stability	$\pm 25$ ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Aging at 25°C	$\pm 5$ ppm/year Maximum
Operating Temperature Range	-40°C to +85°C
Supply Voltage	3.3Vdc $\pm 10\%$
Input Current	35mA Maximum (No Load)
Output Voltage Logic High (Voh)	2.7Vdc Minimum (IOH = -8mA)
Output Voltage Logic Low (Vol)	0.5Vdc Maximum (IOL = +8mA)
Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 $\pm 10$ (%) (Measured at 50% of waveform)
Load Drive Capability	30pF Maximum
Output Logic Type	CMOS
Pin 1 Connection	Tri-State (High Impedance)
Tri-State Input Voltage (Vih and Vil)	70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.
Absolute Clock Jitter	$\pm 250$ pSec Maximum, $\pm 100$ pSec Typical
One Sigma Clock Period Jitter	$\pm 50$ pSec Maximum, $\pm 40$ pSec Typical
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-202, Method 213, Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007, Condition A

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## MECHANICAL DIMENSIONS (all dimensions in millimeters)

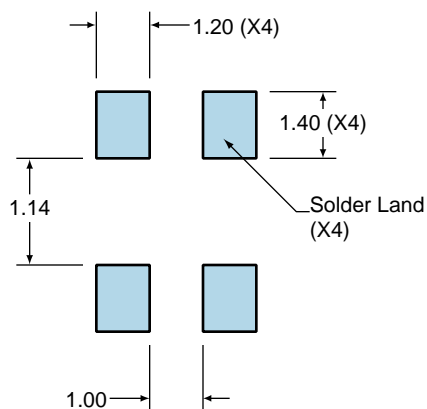


PIN	CONNECTION
1	Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	<b>E2.0480</b> E=Ecliptek Designator
2	<b>XXXXX</b> XXXXX=Ecliptek Manufacturing Identifier

## Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are  $\pm 0.1$

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## OUTPUT WAVEFORM & TIMING DIAGRAM



## Test Circuit for CMOS Output



Note 1: An external  $0.1\mu\text{F}$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu\text{F}$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.

Note 2: A low capacitance ( $<12\text{pF}$ ), 10X attenuation factor, high impedance ( $>10\text{Mohms}$ ), and high bandwidth ( $>300\text{MHz}$ ) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.

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## Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

All Dimensions in Millimeters

Compliant to EIA-481

