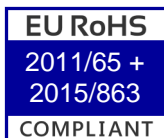


# EV34C6B4A1-34.368M TR



## ITEM DESCRIPTION


Voltage Controlled Quartz Crystal Clock Oscillators VCXO LVCMOS (CMOS) 2.5Vdc 6 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 34.368MHz  $\pm 50$ ppm Maximum  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   $\pm 80$ ppm Minimum 10% Typical, 20% Maximum

## ELECTRICAL SPECIFICATIONS

Nominal Frequency	34.368MHz
Frequency Tolerance/Stability	$\pm 50$ ppm Maximum (Inclusive of all conditions: Calibration Tolerance at $25^{\circ}\text{C}$ , Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, and Vibration.)
Aging at $25^{\circ}\text{C}$	$\pm 2$ ppm/First Year Typical, $\pm 10$ ppm/10 Years Maximum
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Supply Voltage	2.5Vdc $\pm 5\%$
Input Current	15mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	5nSec Maximum (Measured at 20% to 80% of Waveform)
Duty Cycle	50 $\pm 10$ (%) (Measured at 50% of Waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Absolute Pull Range	$\pm 80$ ppm Minimum (Inclusive of all conditions: Calibration Tolerance at $25^{\circ}\text{C}$ , Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, Vibration, and Aging over the Control Voltage (Vc.)
Control Voltage	0.2Vdc to 2.3Vdc (Test Condition for APR)
Control Voltage Range	0.0Vdc to Vdd
Linearity	10% Typical, 20% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB, Vc = 1.25Vdc)
Input Impedance	50kOhms Minimum
Input Leakage Current	10 $\mu$ A Maximum
Phase Noise	All Values are Typical -65dBc/Hz at offset of 10Hz -95dBc/Hz at offset of 100Hz -120dBc/Hz at offset of 1kHz -142dBc/Hz at offset of 10kHz -152dBc/Hz at offset of 100kHz -154dBc/Hz at offset of 1MHz
Tri-State Input Voltage (Vih and Vil)	90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)
RMS Phase Jitter	1pSec Maximum (Fj = 12kHz to 20MHz; Random)
Start Up Time	10mSec Maximum
Storage Temperature Range	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

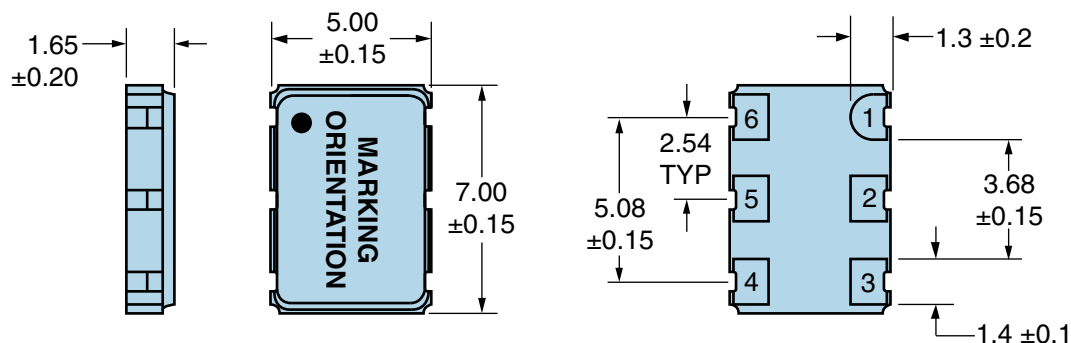
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004

**EV34C6B4A1-34.368M TR** **ENVIRONMENTAL & MECHANICAL SPECIFICATIONS CONTINUED**

<b>Moisture Sensitivity</b>	J-STD-020, MSL 1
<b>Resistance to Soldering Heat</b>	MIL-STD-202, Method 210, Condition K
<b>Resistance to Solvents</b>	MIL-STD-202, Method 215
<b>Solderability</b>	MIL-STD-883, Method 2003
<b>Temperature Cycling</b>	MIL-STD-883, Method 1010, Condition B
<b>Vibration</b>	MIL-STD-883, Method 2007, Condition A

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## MECHANICAL DIMENSIONS (all dimensions in millimeters)

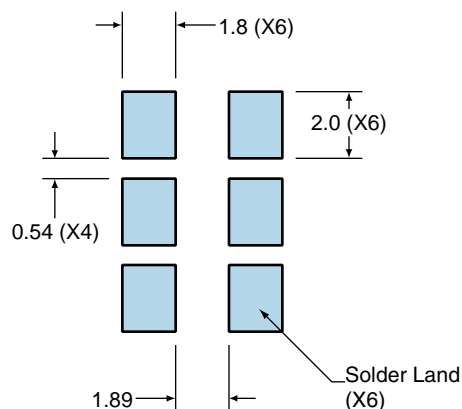


PIN	CONNECTION
1	Control Voltage
2	Tri-State
3	Case/Ground
4	Output
5	No Connect
6	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	34.368M
3	XXXXX XXXXX=Ecliptek Manufacturing Identifier

## Suggested Solder Pad Layout

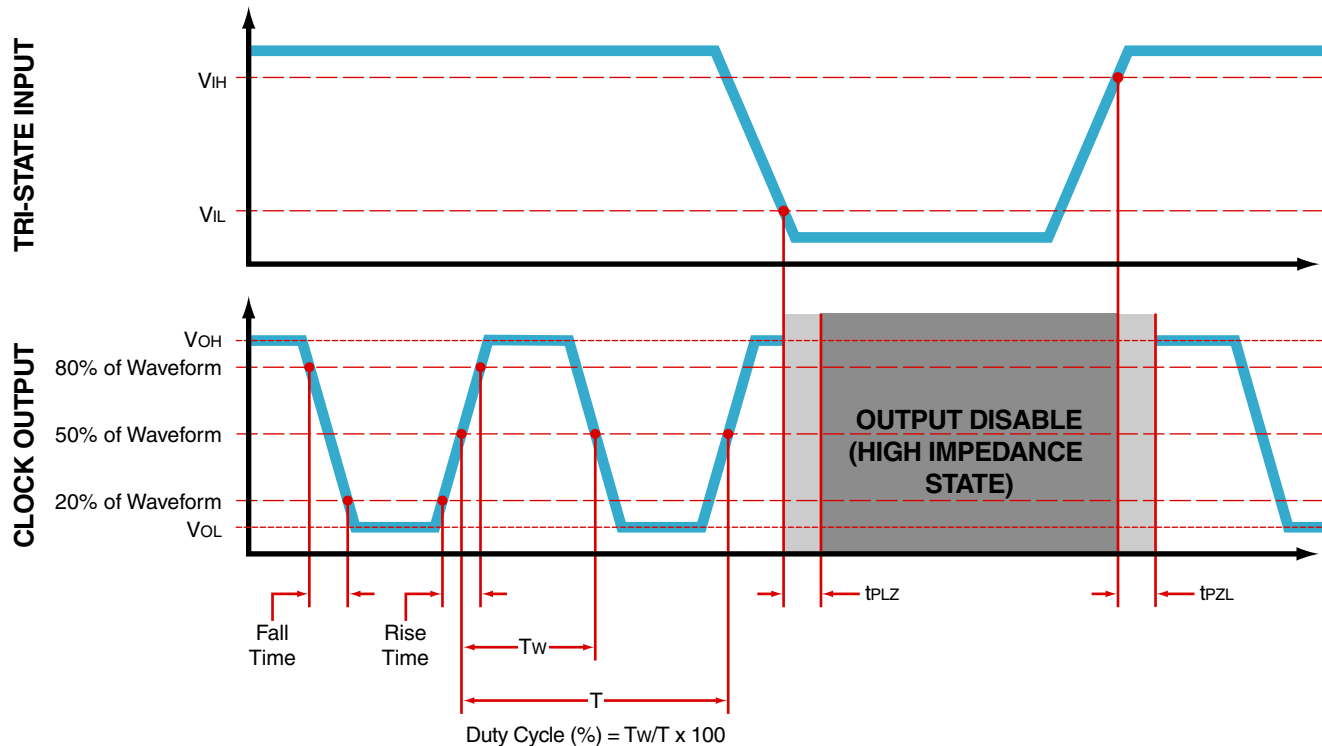
All Dimensions in Millimeters



All Tolerances are ±0.1

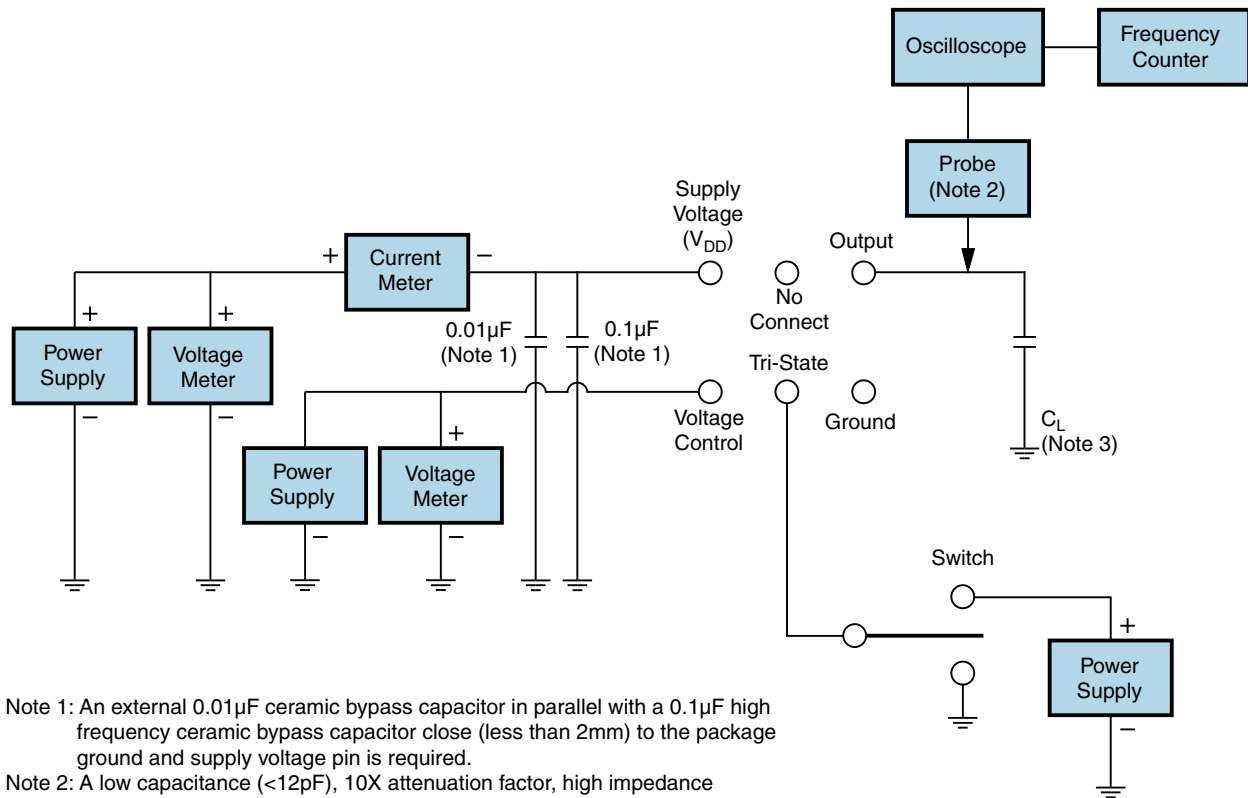
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## OUTPUT WAVEFORM & TIMING DIAGRAM



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## Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.

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## Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

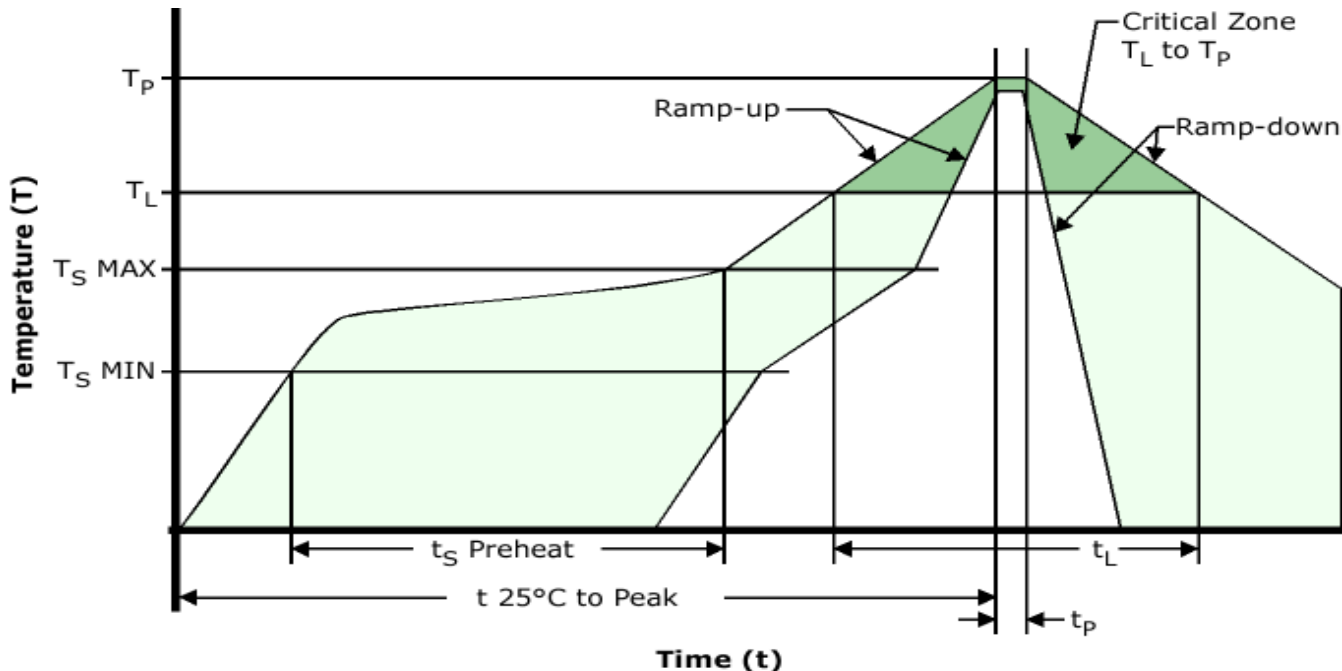
All Dimensions in Millimeters

Compliant to EIA-481



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## Recommended Solder Reflow Methods



## High Temperature Infrared/Convection

$T_S$  MAX to  $T_L$  (Ramp-up Rate) 3°C/Second Maximum

### Preheat

- Temperature Minimum ( $T_S$  MIN) 150°C
- Temperature Typical ( $T_S$  TYP) 175°C
- Temperature Maximum ( $T_S$  MAX) 200°C
- Time ( $t_s$  MIN) 60 - 180 Seconds

Ramp-up Rate ( $T_L$  to  $T_P$ ) 3°C/Second Maximum

### Time Maintained Above:

- Temperature ( $T_L$ ) 217°C
- Time ( $t_L$ ) 60 - 150 Seconds

Peak Temperature ( $T_P$ ) 260°C Maximum for 10 Seconds Maximum

Target Peak Temperature ( $T_P$  Target) 250°C +0/-5°C

Time within 5°C of actual peak ( $t_p$ ) 20 - 40 Seconds

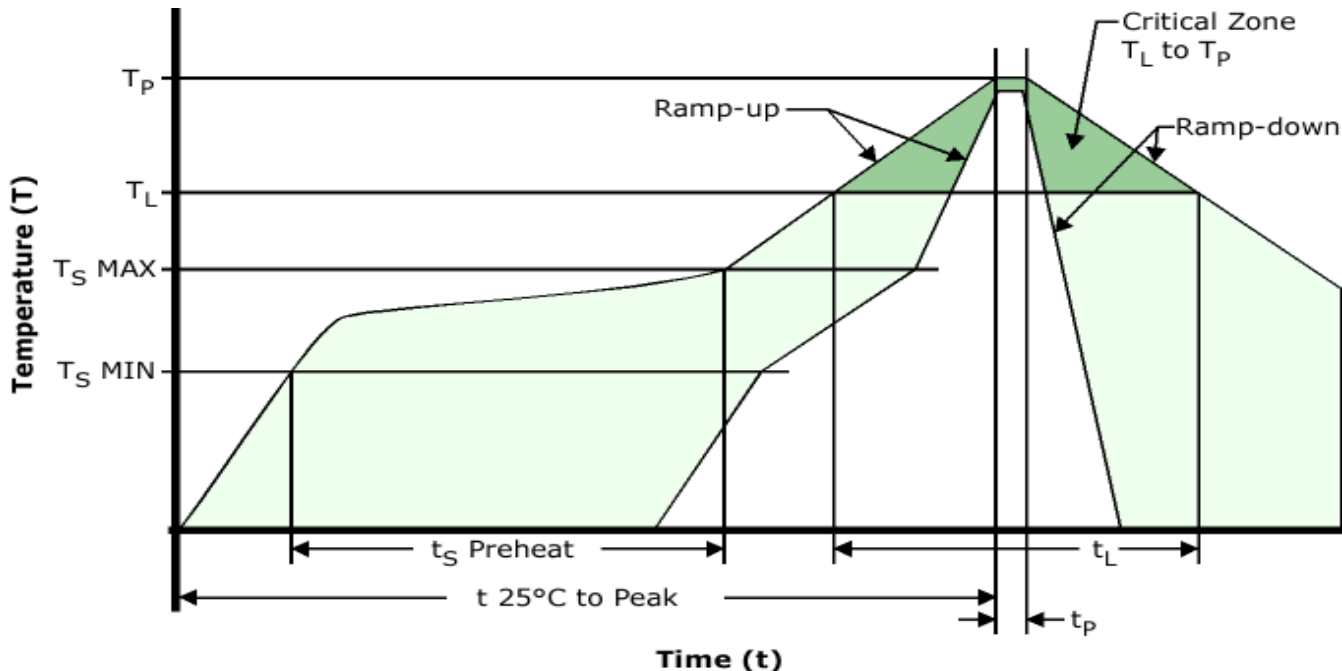
Ramp-down Rate 6°C/Second Maximum

Time 25°C to Peak Temperature (t) 8 Minutes Maximum

Moisture Sensitivity Level Level 1

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## Recommended Solder Reflow Methods



### Low Temperature Infrared/Convection 240°C

**T<sub>s</sub> MAX to T<sub>L</sub> (Ramp-up Rate)** 5°C/Second Maximum

#### Preheat

- Temperature Minimum (T<sub>s</sub> MIN) N/A  
 - Temperature Typical (T<sub>s</sub> TYP) 150°C  
 - Temperature Maximum (T<sub>s</sub> MAX) N/A  
 - Time (t<sub>s</sub> MIN) 60 - 120 Seconds

**Ramp-up Rate (T<sub>L</sub> to T<sub>P</sub>)** 5°C/Second Maximum

#### Time Maintained Above:

- Temperature (T<sub>L</sub>) 150°C  
 - Time (t<sub>L</sub>) 200 Seconds Maximum

**Peak Temperature (T<sub>P</sub>)** 240°C Maximum

**Target Peak Temperature (T<sub>P</sub> Target)** 240°C Maximum 2 Times / 230°C Maximum 1 Time

**Time within 5°C of actual peak (t<sub>p</sub>)** 10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time

**Ramp-down Rate** 5°C/Second Maximum

**Time 25°C to Peak Temperature (t)** N/A

**Moisture Sensitivity Level** Level 1

### Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

### High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.