

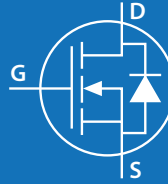
EPC2202 - Automotive 80 V (D-S) Enhancement Mode Power Transistor

V_{DS} , 80 V

$R_{DS(on)}$, 17 mΩ

I_D , 18 A

AEC-Q101



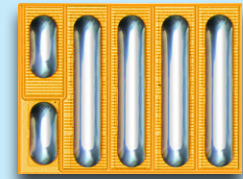
Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:
Ask a GaN
Expert



Die size: 2.1 x 1.6 mm

EPC2202 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- Lidar/pulsed power applications
- High power density DC-DC converters
- Class-D audio
- High intensity headlamps

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint



Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 12^\circ\text{C/W}$)	18	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	75	
V_{GS}	Gate-to-Source Voltage	5.75	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	4	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	69	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 300 \mu\text{A}$	80			V
I_{DSS}	Drain-Source Leakage	$V_{DS} = 64 \text{ V}$, $V_{GS} = 0 \text{ V}$		20	250	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.01	3	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.01	0.25	mA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 3 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 11 \text{ A}$		12	17	mΩ
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.8		V

All measurements were done with substrate connected to source.

Dynamic Characteristics[#] (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		345	415	pF
C _{RSS}	Reverse Transfer Capacitance			3		
C _{OSS}	Output Capacitance			230	345	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 50 V, V _{GS} = 0 V		279		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			352		
R _G	Gate Resistance			0.4		Ω
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 11 A		3.2	4	nC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 11 A		1		
Q _{GD}	Gate-to-Drain Charge			0.55		
Q _{G(TH)}	Gate Charge at Threshold			0.7		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		18	27	
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 62.5% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 62.5% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

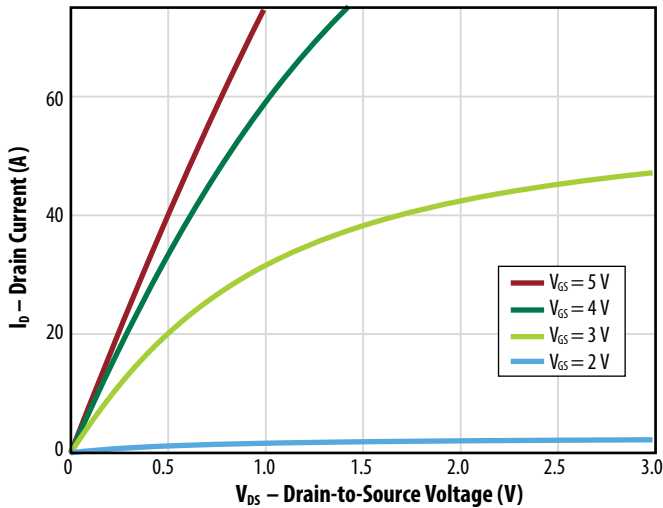


Figure 2: Typical Transfer Characteristics

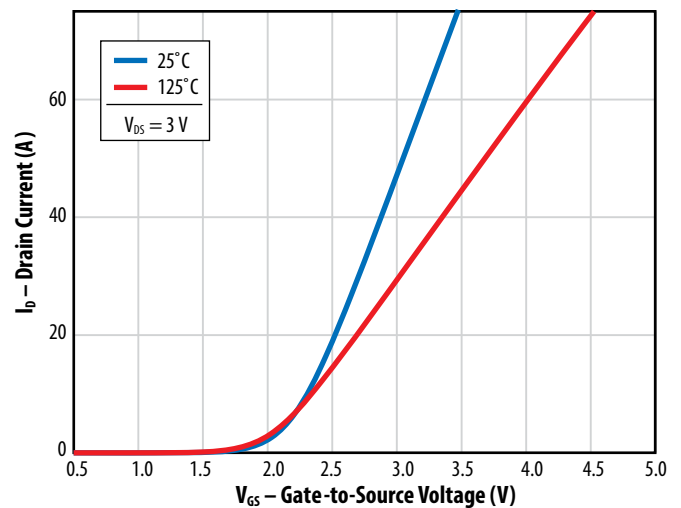


Figure 3: R_{DS(on)} vs. V_{GS} for Various Currents

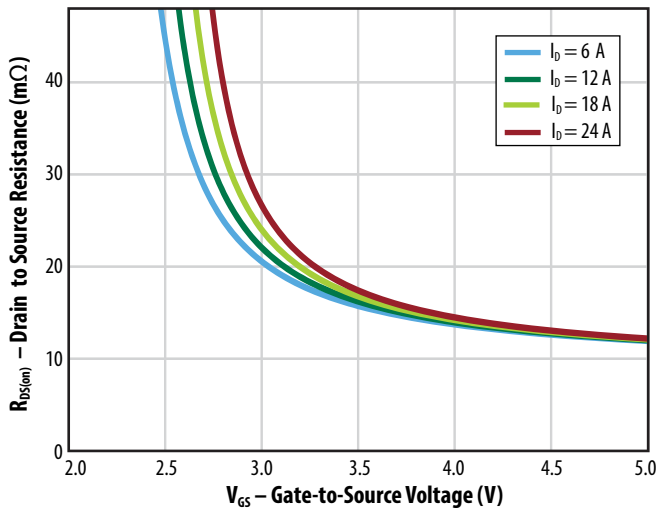


Figure 4: R_{DS(on)} vs. V_{GS} for Various Temperatures

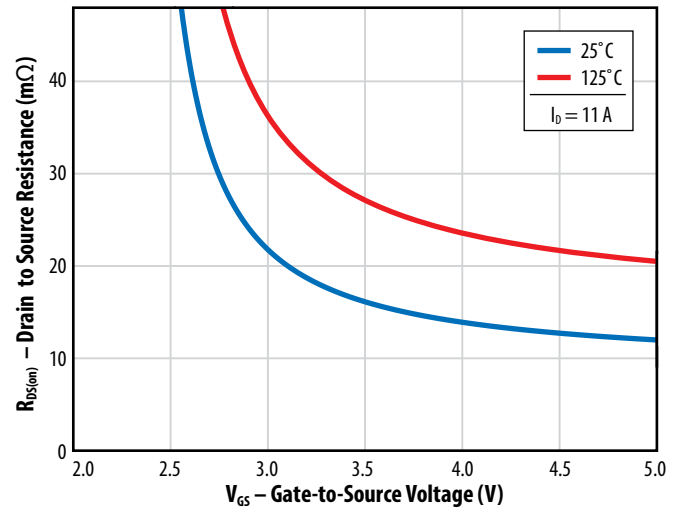


Figure 5a: Typical Capacitance (Linear Scale)

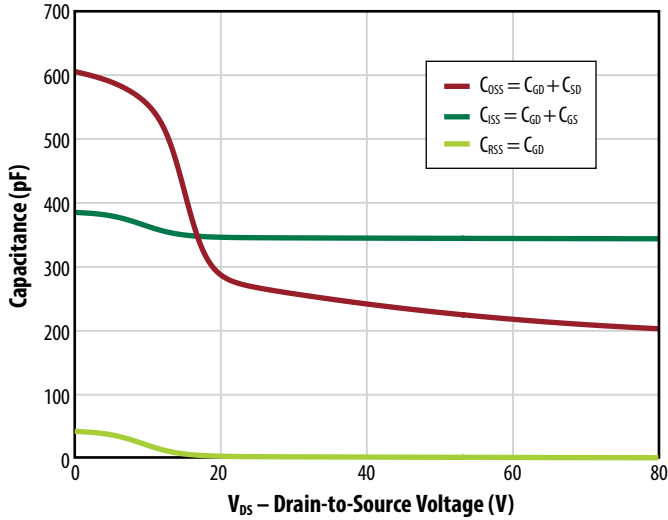


Figure 5b: Typical Capacitance (Log Scale)

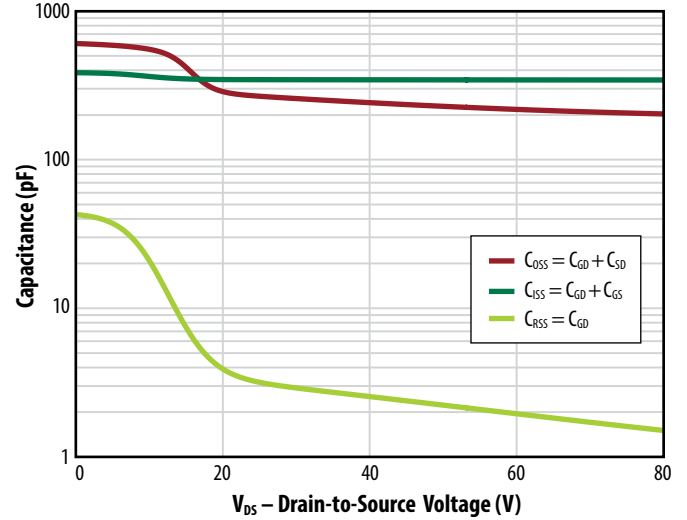


Figure 5c: Typical Output Charge and C_{oss} Stored Energy

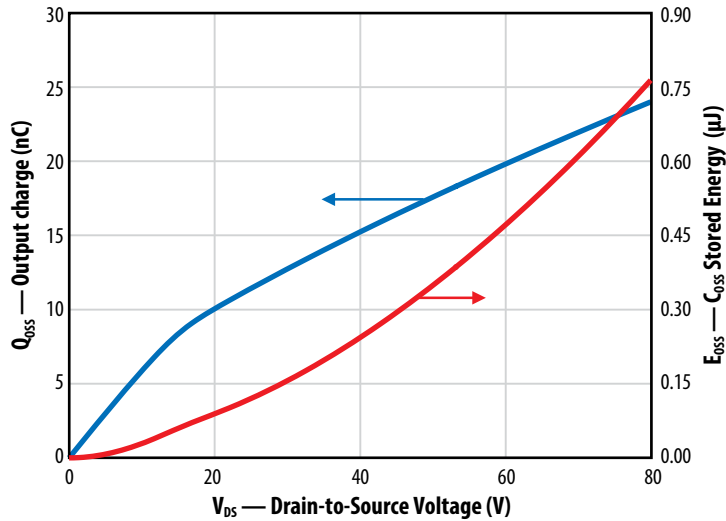


Figure 6: Typical Gate Charge

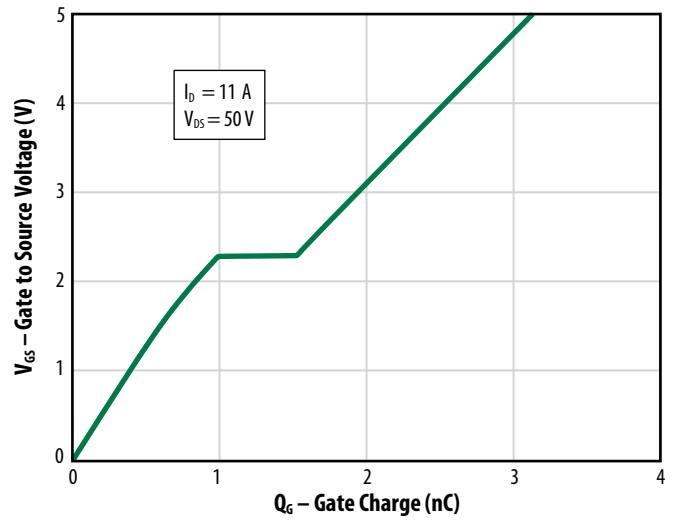


Figure 7: Typical Reverse Drain-Source Characteristics

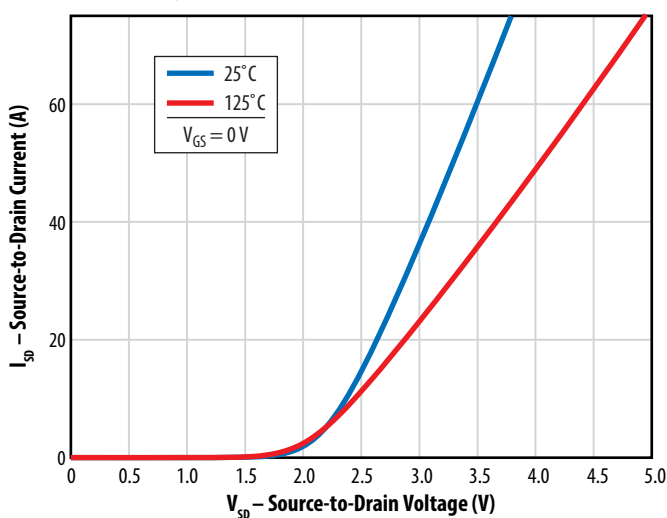
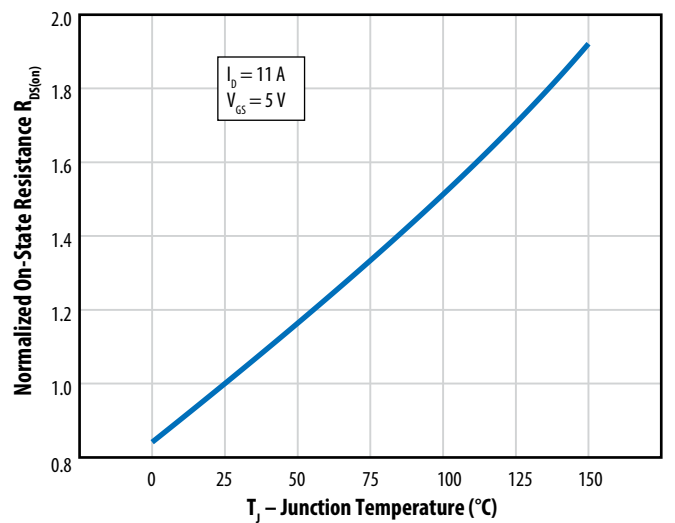


Figure 8: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0V for OFF.

Figure 9: Normalized Threshold Voltage vs. Temperature

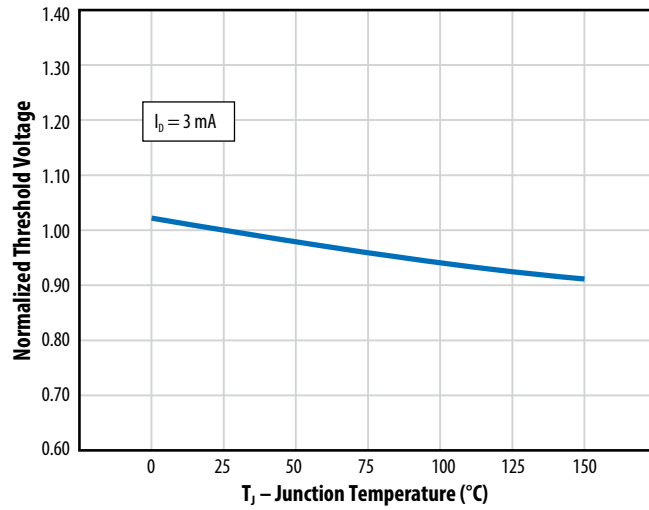


Figure 10: Transient Thermal Response Curves

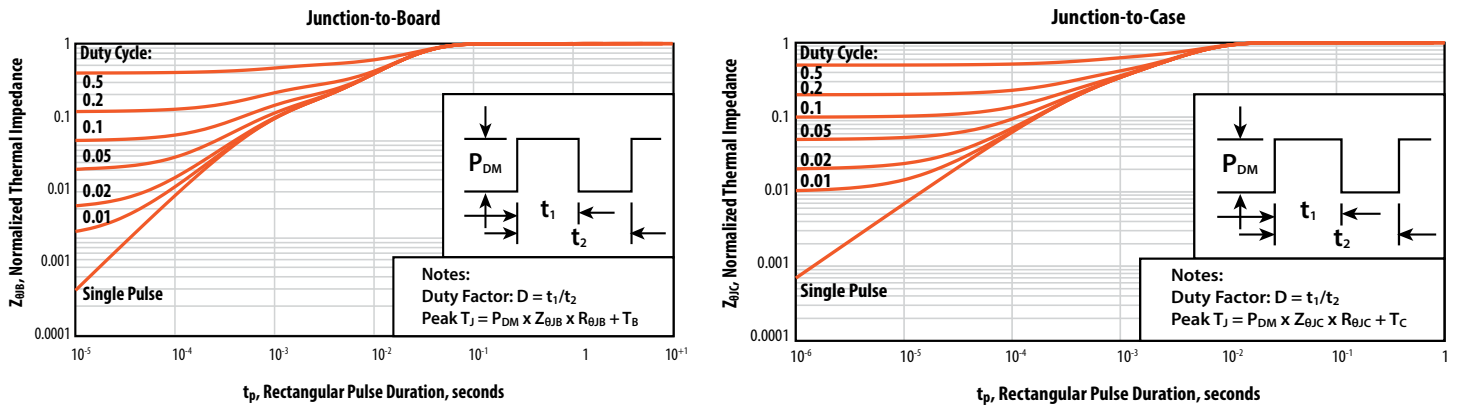
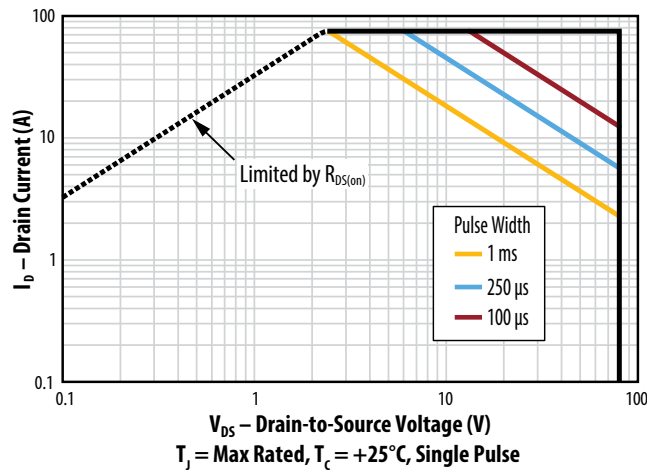
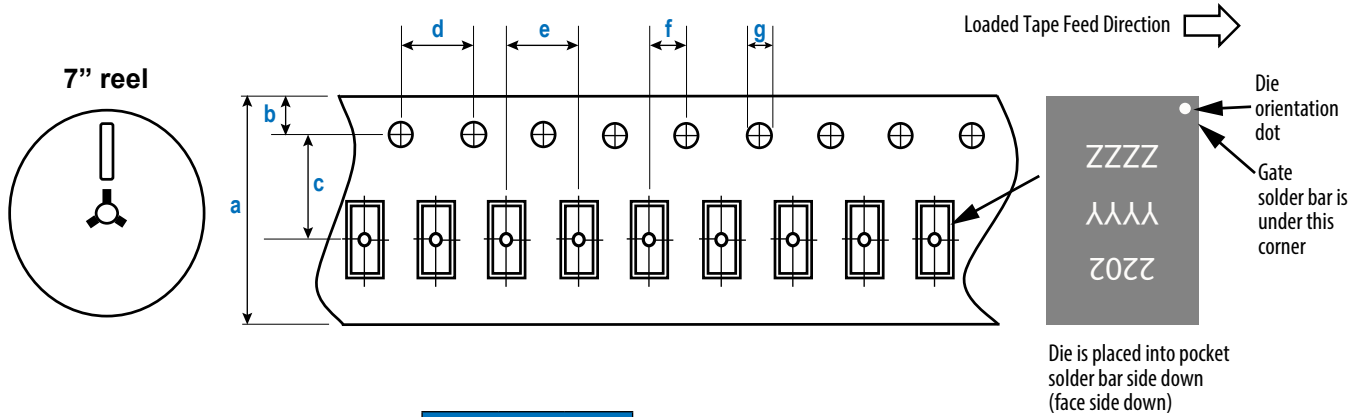


Figure 11: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

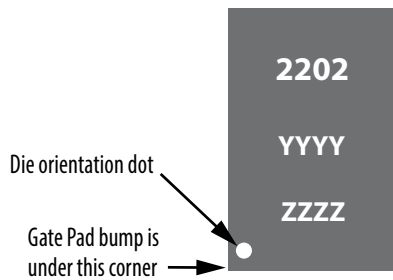


EPC2202 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	7.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

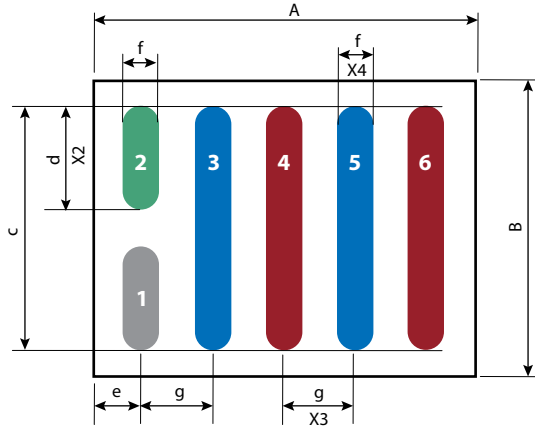
DIE MARKINGS



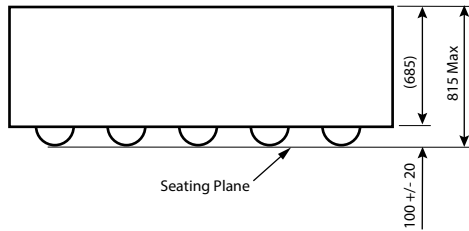
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2202	2202	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View



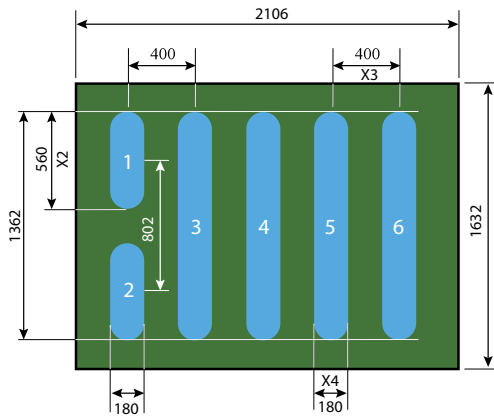
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2076	2106	2136
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;
 Pads no. 3, 5 are Drain;
 Pads no. 4, 6 are Source;
 Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(units in μm)



The land pattern is solder mask defined.

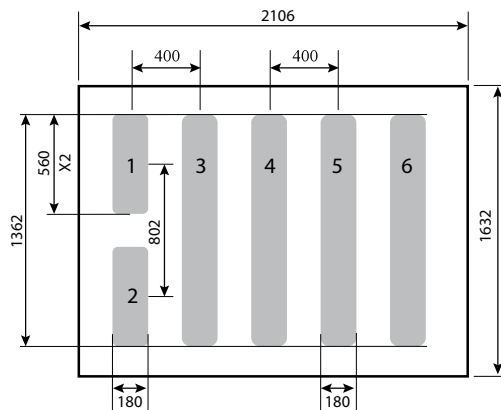
Pad no. 1 is Gate;
 Pads no. 3, 5 are Drain;
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 Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

Solder mask
 (for solder mask defined pads)

RECOMMENDED STENCIL DRAWING

(measurements in μm)



Recommended stencil should be 4mil (100 μm) thick, must be laser cut, opening per drawing. The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at

TYPICAL THERMAL CONCEPT

The EPC2202 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs.

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

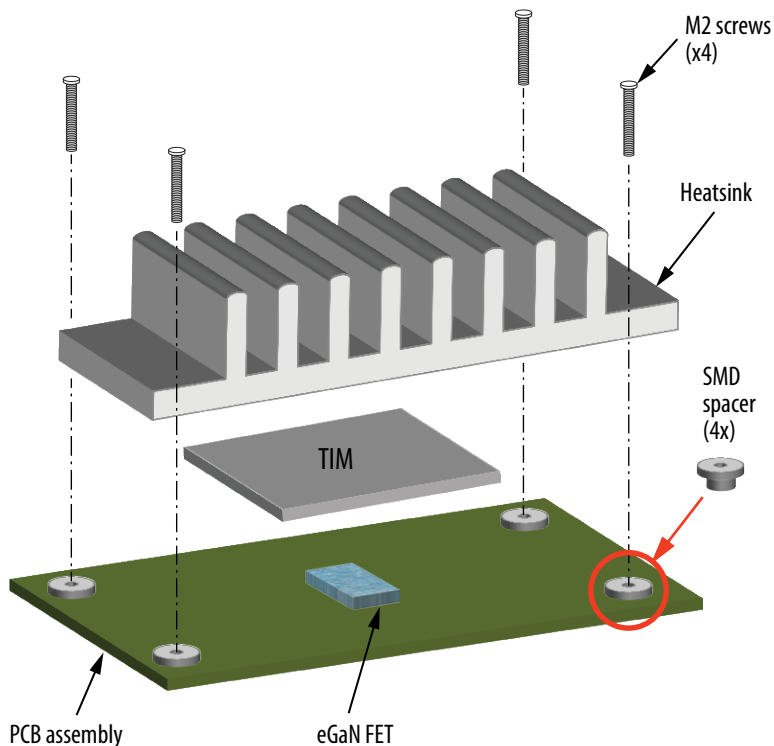


Figure 13: Exploded view of heatsink assembly using screws

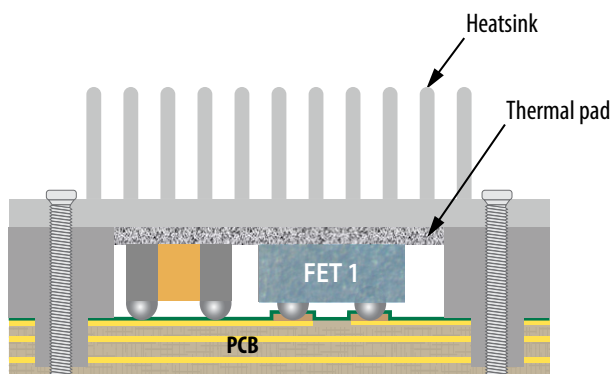


Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

Solder mask defined pads are recommended for best reliability.

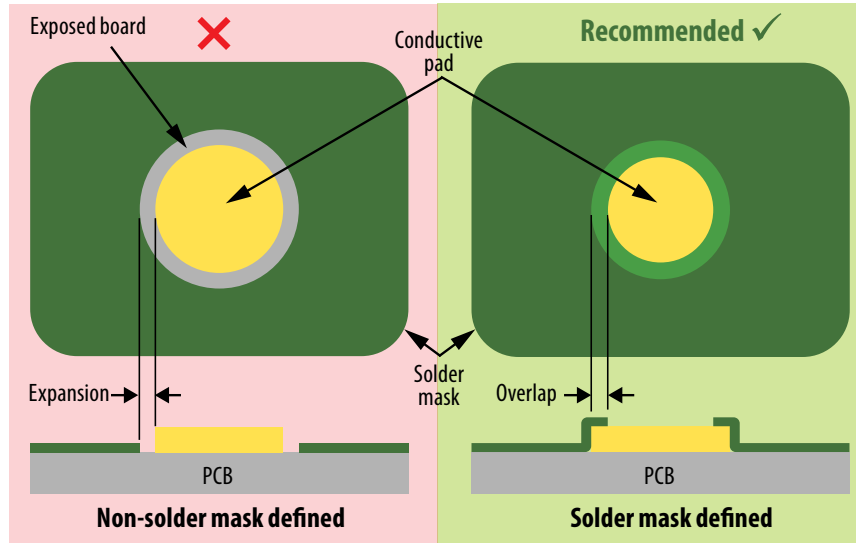


Figure 15: Solder mask defined versus non-solder mask defined pad

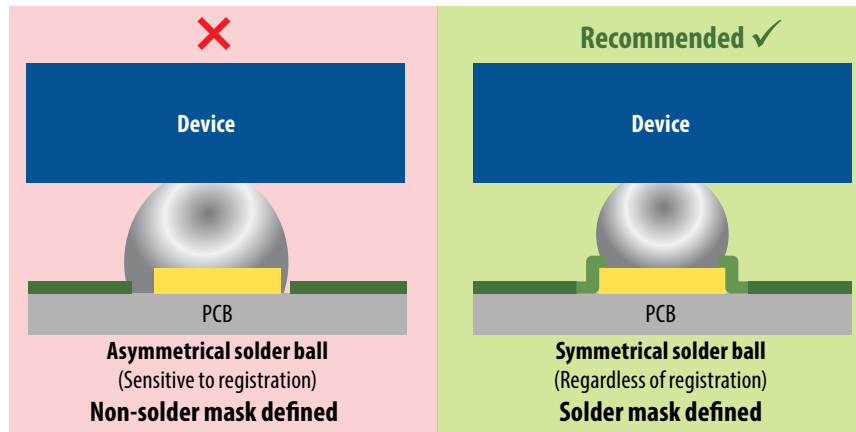


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip> (for preliminary device Altium footprints, contact EPC)

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