FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS377
Octal D Flip-Flop with Common Enable and Clock

General Description

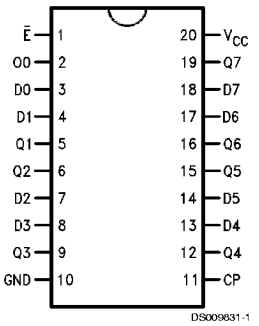
The 'LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

Features

- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

Connection Diagram

Dual-In-Line Package



DS009831-1

Order Number DM54LS377E, DM54LS377J, DM54LS377W, DM74LS377WM or DM74LS377N
See Package Number
E20A, J20A, M20B, N20A or W20A

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q7	Flip-Flop Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54LS	−55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS377			DM74LS377			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH or LOW	20			10			ns
t_s (L)	D_n to CP	20			10			
t_h (H)	Hold Time HIGH or LOW	5.0			5.0			ns
t_h (L)	D_n to CP	5.0			5.0			
t_s (H)	Setup Time HIGH or LOW	10			10			ns
t_s (L)	$\overline{E}$ to CP	20			20			
t_h (H)	Hold Time HIGH or LOW	5.0			5.0			ns
t_h (L)	$\overline{E}$ to CP	5.0			5.0			
t_w (H)	CP Pulse Width HIGH or LOW	20			20			ns
t_w (L)		20			20			

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5			V
	Voltage	V_{IL} = Max	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54			0.4	
	Voltage	V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
	Input Voltage	V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				28	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH}	Propagation Delay		25	ns
t_{PHL}	CP to Q_n		25	

Functional Description

The 'LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

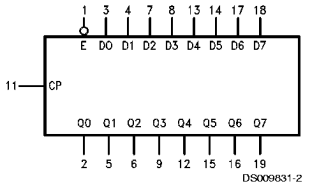
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	X	X	No Change
L	⌐	H	H
L	⌐	L	L

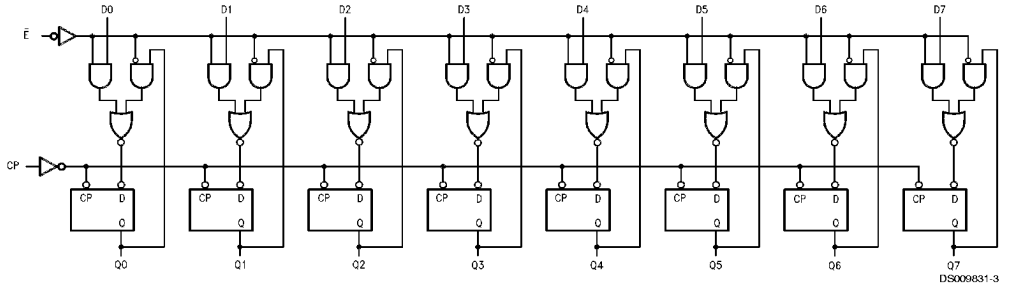
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

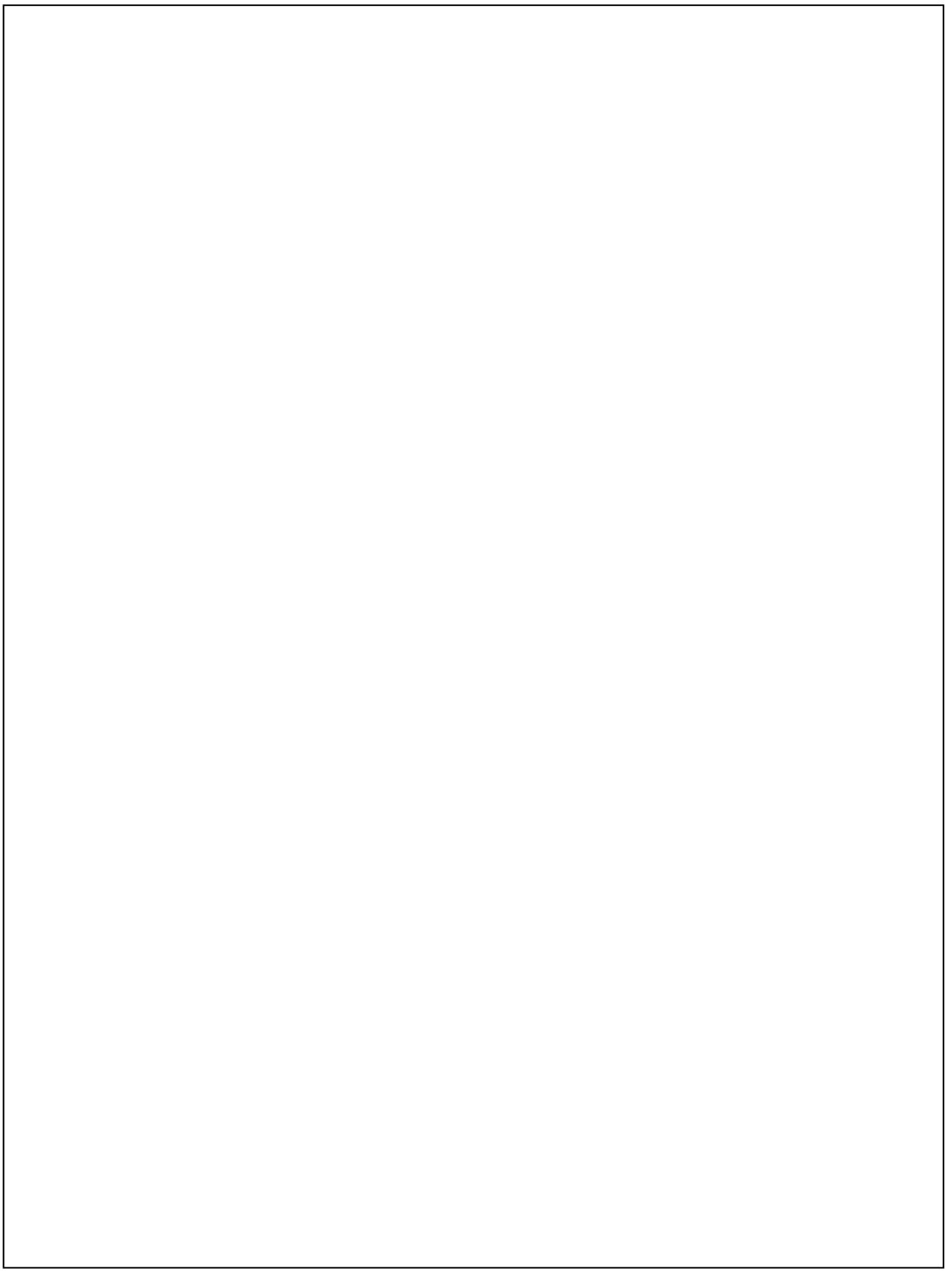
Logic Symbol



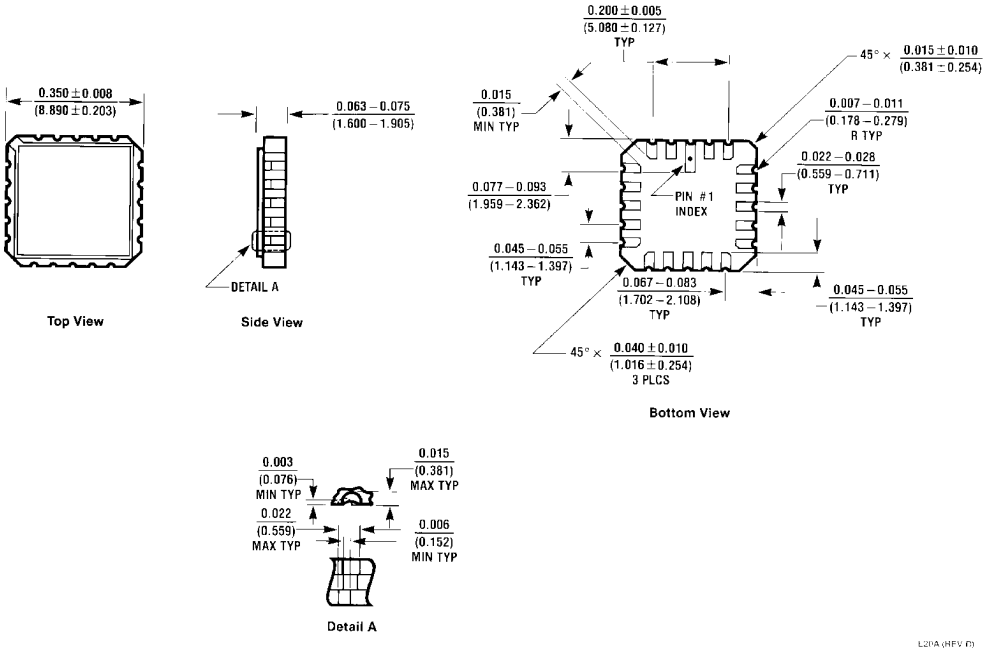
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram





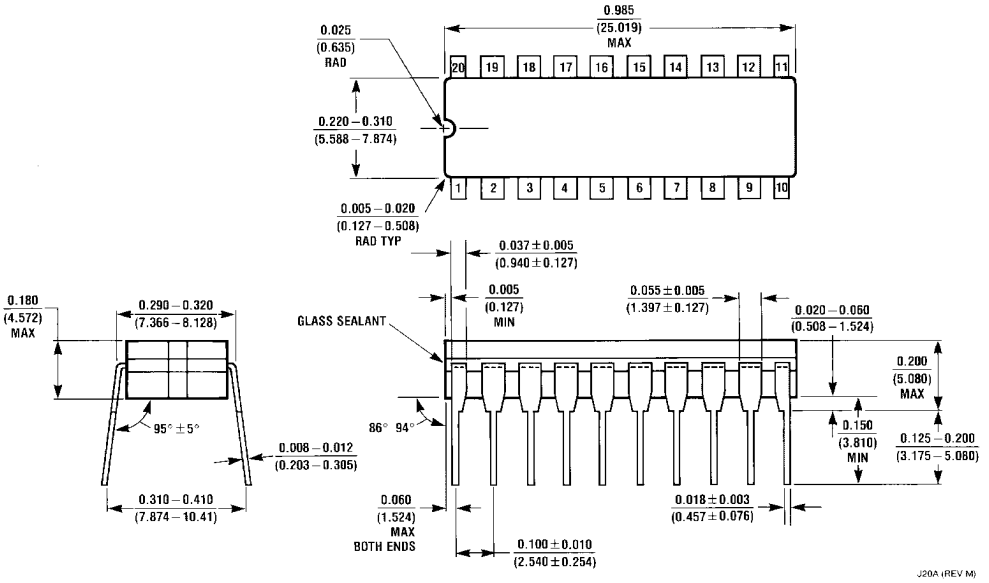
Physical Dimensions inches (millimeters) unless otherwise noted



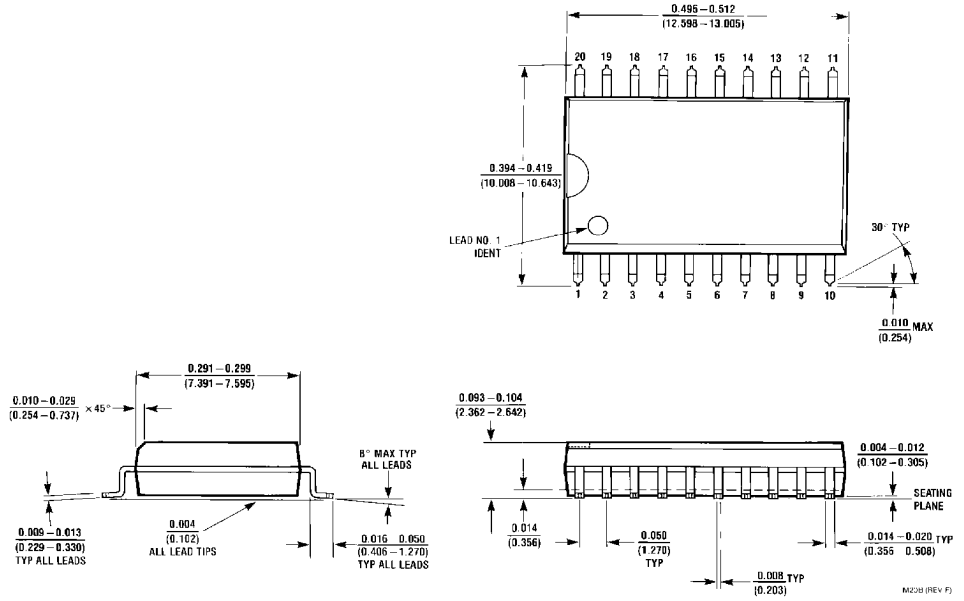
E20A (REV D)

Ceramic Leadless Chip Carrier (E)
Order Number DM54LS377E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

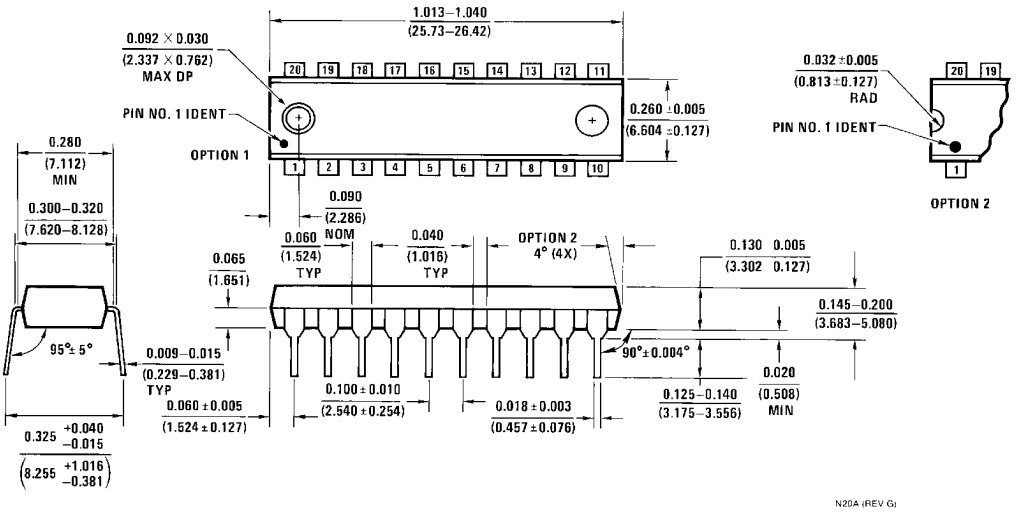


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS377J
Package Number J20A

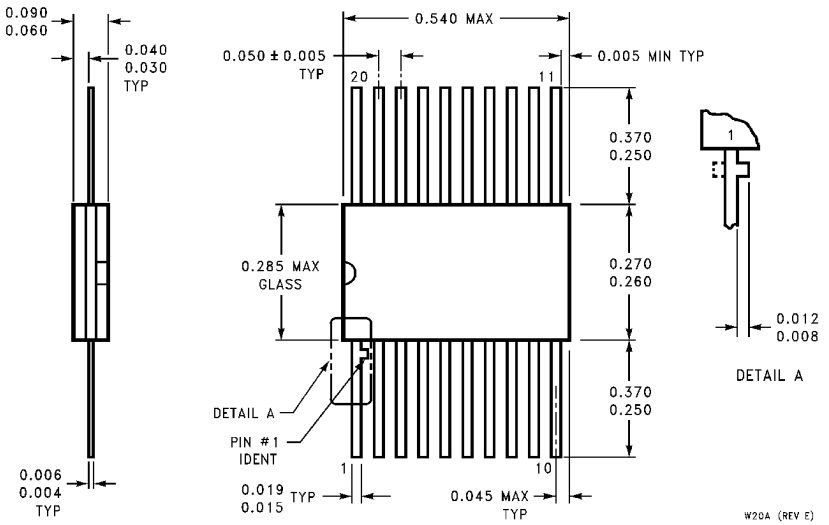


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS377WM
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS377N
Package Number N20A



20-Lead Ceramic Flat Package (W)
Order Number DM54LS377W
Package Number W20A