

FQB6N60C / FQI6N60C

600V N-Channel MOSFET

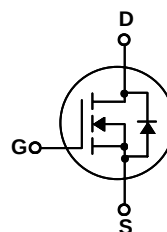
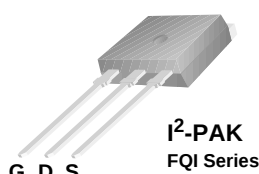
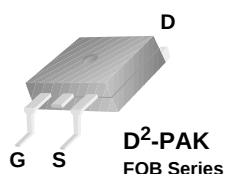
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 5.5A, 600V, $R_{DS(on)} = 2.0\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 16 nC)
- Low C_{rss} (typical 7 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB6N60C / FQI6N60C		Units
V_{DSS}	Drain-Source Voltage	600		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	5.5	5.5 *	A
		3.3	3.3 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	22	22 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	300		mJ
I_{AR}	Avalanche Current (Note 1)	5.5		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	12.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	125		W
		1.0		W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	1.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	-	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.6	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.75\text{ A}$	--	1.7	2.0	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.75\text{ A}$ (Note 4)	--	4.8	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	620	810	pF
C_{oss}	Output Capacitance		--	65	85	pF
C_{rss}	Reverse Transfer Capacitance		--	7	10	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 5.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	15	40	ns
t_r	Turn-On Rise Time		--	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	45	100	ns
t_f	Turn-Off Fall Time		--	45	100	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 5.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	16	20	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	6.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	5.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	22	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 5.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 5.5 A,	--	310	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	2.1	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 18.2\text{ mH}$, $I_{AS} = 5.5\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 5.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

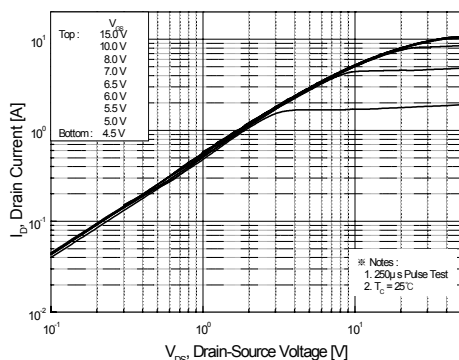


Figure 1. On-Region Characteristics

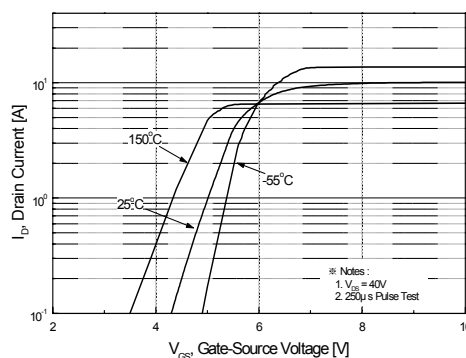


Figure 2. Transfer Characteristics

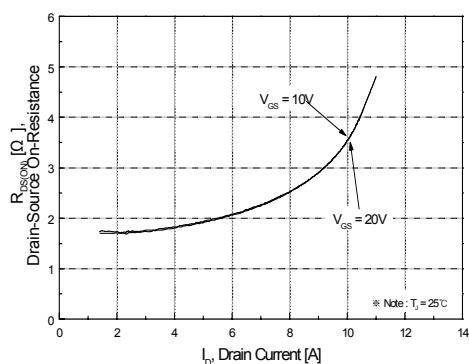


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

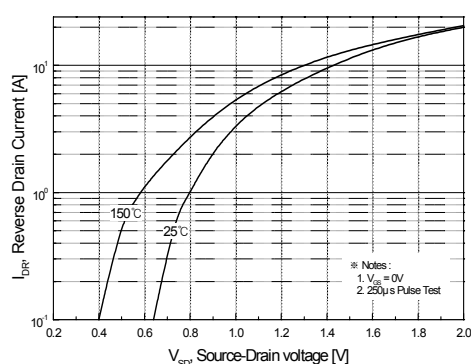


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

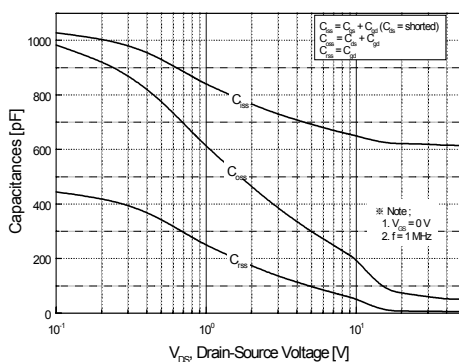


Figure 5. Capacitance Characteristics

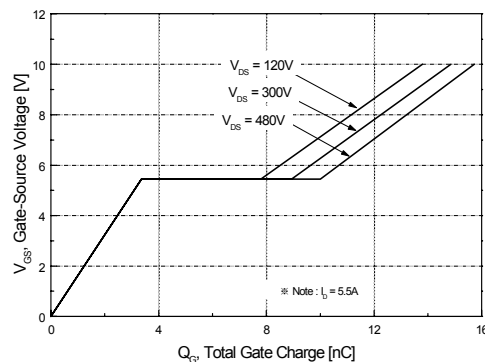


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

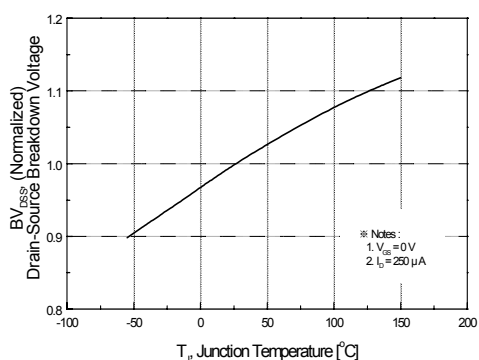


Figure 7. Breakdown Voltage Variation vs Temperature

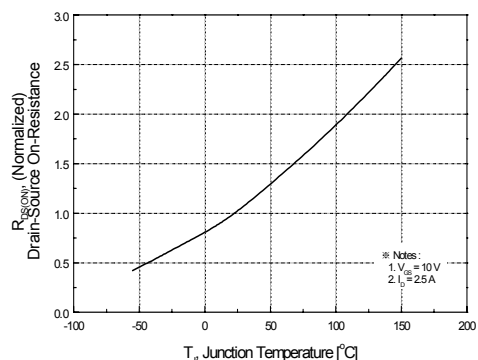


Figure 8. On-Resistance Variation vs Temperature

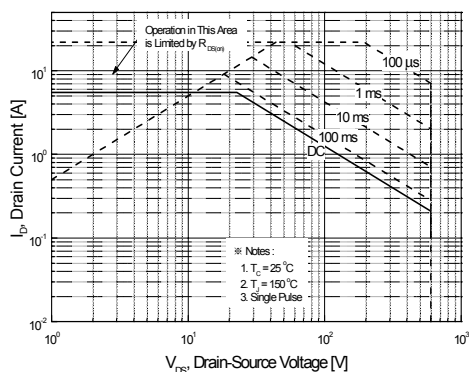


Figure 9. Maximum Safe Operating Area

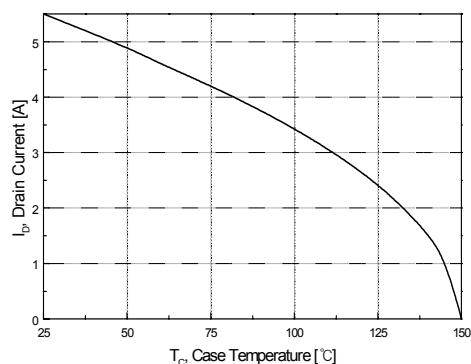


Figure 10. Maximum Drain Current vs Case Temperature

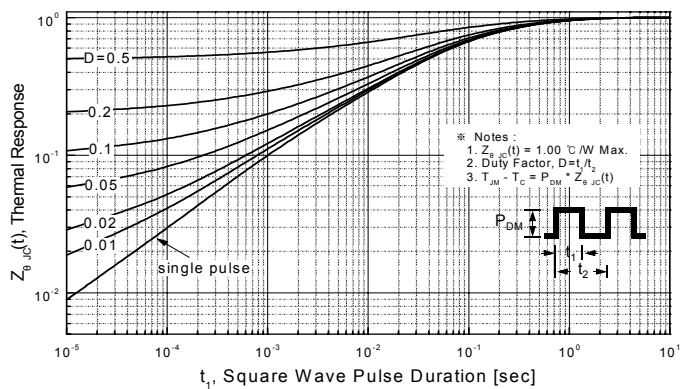
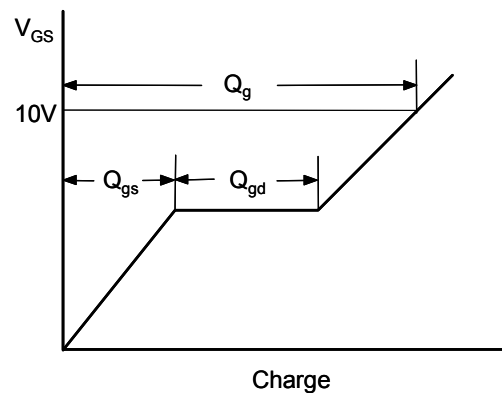
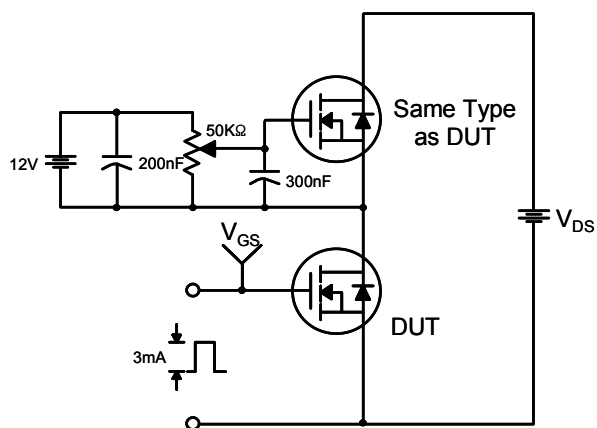
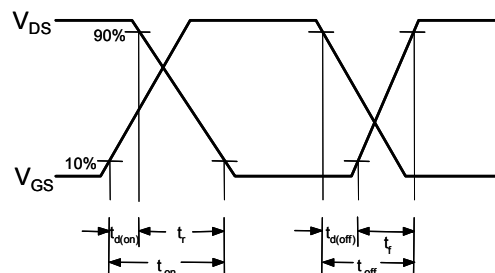
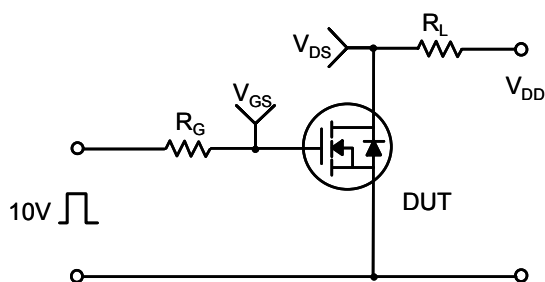


Figure 11. Transient Thermal Response Curve

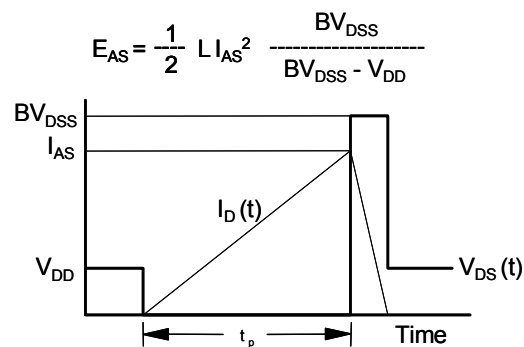
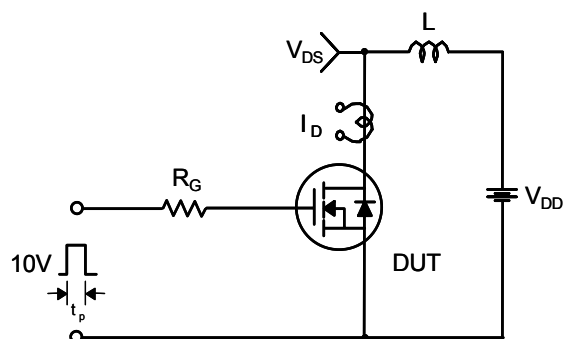
Gate Charge Test Circuit & Waveform



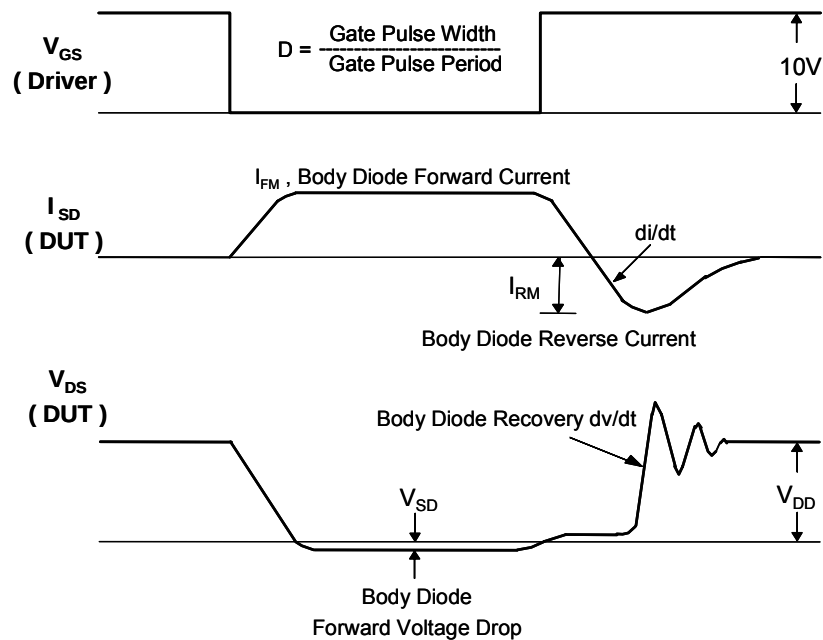
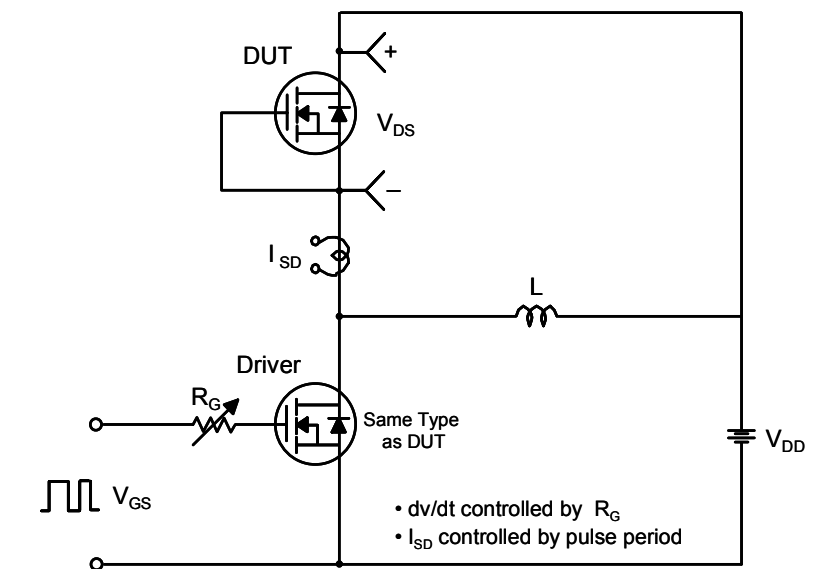
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



FQ6N60C / FQ16N60C

Technical drawing of a rectangular electronic component with three pins, showing top, side, and front views with dimensions in millimeters.

Top View Dimensions:

- Overall width: 9.90 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin pitch (center-to-center): 2.54 TYP
- Pin width: 0.80 ± 0.10
- Distance from top edge to pin start: 1.40 ± 0.20
- Distance from pin start to pin end: 4.90 ± 0.20
- Distance from pin end to bottom edge: 9.20 ± 0.20
- Top edge chamfer: 1.20 ± 0.20
- Top edge chamfer radius: (0.40)

Side View Dimensions:

- Overall width: 4.50 ± 0.20
- Pin width: 0.80 ± 0.10
- Distance from top edge to pin start: 1.40 ± 0.20
- Distance from pin start to pin end: 4.90 ± 0.20
- Distance from pin end to bottom edge: 9.20 ± 0.20
- Top edge chamfer: 1.20 ± 0.20
- Top edge chamfer radius: (0.40)

Front View Dimensions:

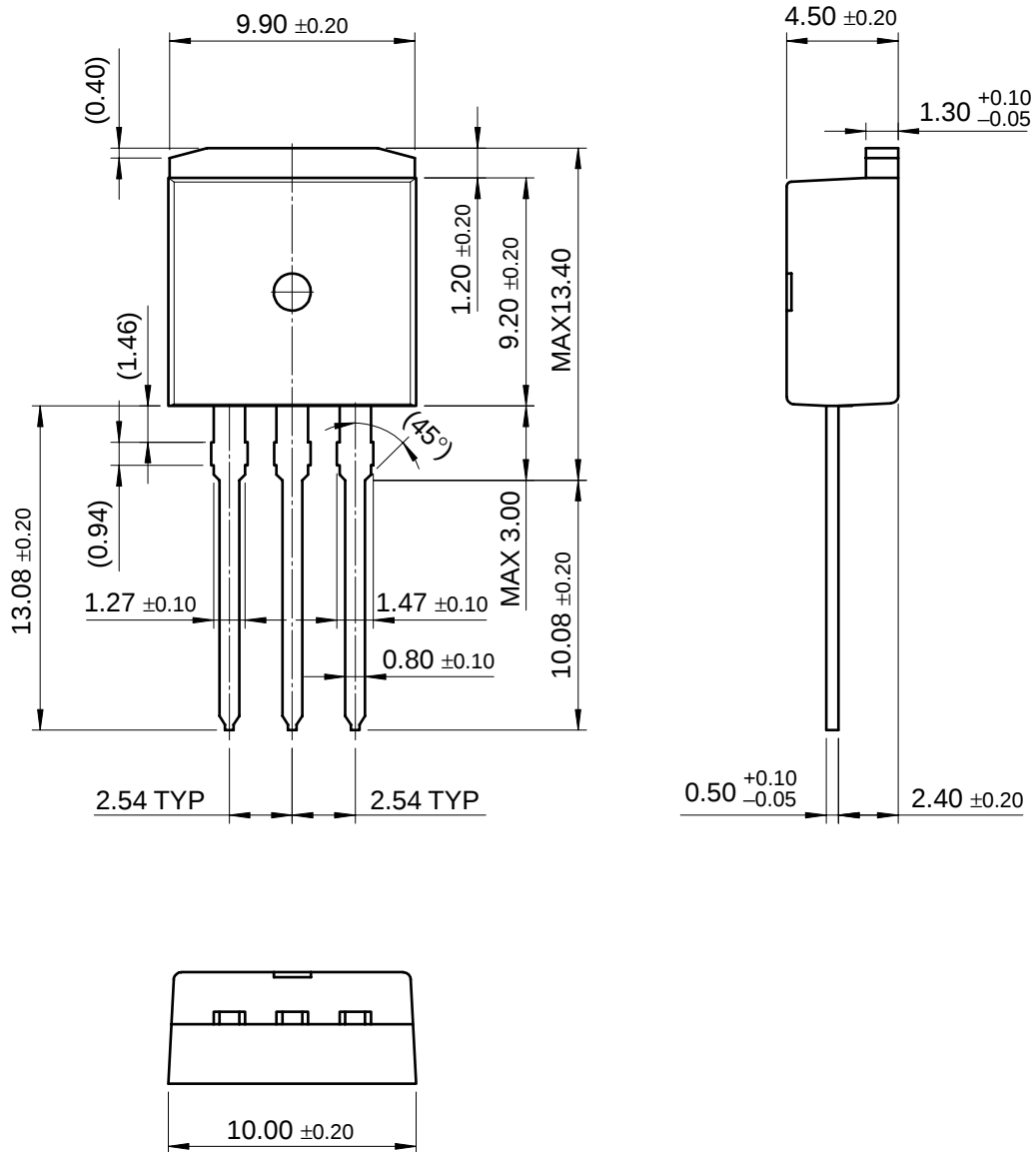
- Overall width: 10.00 ± 0.20
- Pin pitch (center-to-center): 2.54 TYP
- Pin width: 0.80 ± 0.10
- Distance from top edge to pin start: 1.40 ± 0.20
- Distance from pin start to pin end: 4.90 ± 0.20
- Distance from pin end to bottom edge: 9.20 ± 0.20
- Top edge chamfer: 1.20 ± 0.20
- Top edge chamfer radius: (0.40)

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Package Dimensions (Continued)

I²-PAK



Dimensions in Millimeters

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