Freescale Semiconductor
Data Sheet: Technical Data

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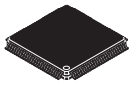
MCF52235



LQFP-80
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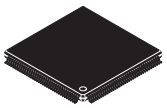

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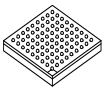

MAPBGA-121
12mm_x_12mm

MCF52235 ColdFire Microcontroller Data Sheet

Supports MCF52230, MCF52231, MCF52232, MCF52233, MCF52234, MCF52235, and MCF52236

The MCF52235 is a member of the ColdFire® family of reduced instruction set computing (RISC) microcontrollers. This document provides an overview of the MCF52235 microcontroller family, focusing on its highly integrated and diverse feature set.

This 32-bit device is based on the Version 2 ColdFire core operating at a frequency up to 60 MHz, offering high performance and low power consumption. On-chip memories connected tightly to the processor core include up to 256 Kbytes of Flash and 32 Kbytes of static random access memory (SRAM). On-chip modules include:

- V2 ColdFire core providing 56 Dhrystone 2.1 MIPS @ 60 MHz executing out of on-chip Flash memory using enhanced multiply accumulate (EMAC) and hardware divider
- Enhanced Multiply Accumulate Unit (EMAC) and hardware divide module
- Cryptographic Acceleration Unit (CAU) coprocessor
- Fast Ethernet Controller (FEC)
- On-chip Ethernet Transceiver (EPHY)
- FlexCAN controller area network (CAN) module
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)
- Inter-integrated circuit (I^2C™) bus controller
- Queued serial peripheral interface (QSPI) module
- Eight-channel 10- or 12-bit fast analog-to-digital converter (ADC)
- Four channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support (DTIM)
- Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM) and pulse accumulation
- Eight/Four-channel 8/16-bit pulse width modulation timers (two adjacent 8-bit PWMs can be concatenated to form a single 16-bit timer)
- Two 16-bit periodic interrupt timers (PITs)
- Real-time clock (RTC) module
- Programmable software watchdog timer
- Two interrupt controllers providing every peripheral with a unique selectable-priority interrupt vector plus seven external interrupts with fixed levels/priorities
- Clock module with support for crystal or external oscillator and integrated phase-locked loop (PLL)
- Test access/debug port (JTAG, BDM)

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1 MCF52235 Family Configurations

Table 1. MCF52235 Family Configurations

Module	52230	52231	52232	52233	52234	52235	52236
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•	•
System Clock (MHz)	60	60	50	60	60	60	50
Performance (Dhrystone 2.1 MIPS)	56	56	46	56	56	56	46
Flash / Static RAM (SRAM)	128/32 Kbytes	128/32 Kbytes	128/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes
Interrupt Controllers (INTC0/INTC1)	•	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•	•
Random Number Generator and Crypto Acceleration Unit (CAU)	—	—	—	—	—	•	—
FlexCAN 2.0B Module	—	•	—	—	•	•	—
Fast Ethernet Controller (FEC) with on-chip interface (EPHY)	•	•	•	•	•	•	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•	•
Programmable Interrupt Timer	2	2	2	2	2	2	2
Four-Channel General Purpose Timer	•	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4	4
QSPI	•	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port[1]	•	•	•	•	•	•	•
Package	80 LQFP 112 LQFP	80 LQFP 112 LQFP	80 LQFP	80 LQFP 112 LQFP	112 LQFP 121 MAPBGA	112 LQFP 121 MAPBGA	80 LQFP

[1] The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

1.1 Block Diagram

The MCF52235 (or its variants) comes in 80- and 112-pin low-profile quad flat pack packages (LQFP) and a 121 MAPBGA, and operates in single-chip mode only. Figure 1 shows a top-level block diagram of the MCF52235.

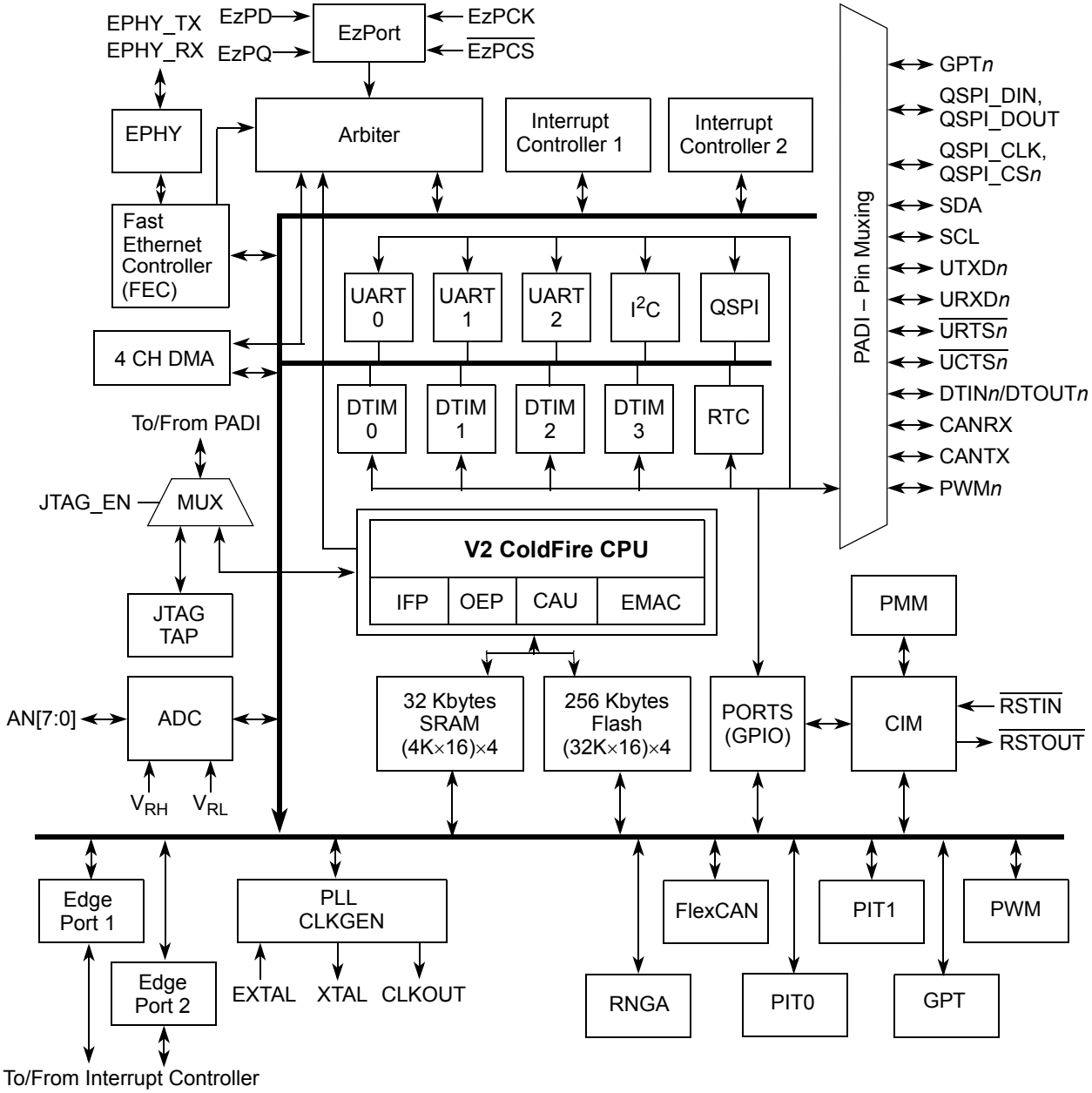


Figure 1. MCF52235 Block Diagram

1.2 Features

This document contains information on a new product under development. Freescale reserves the right to change or discontinue this product without notice. Specifications and information herein are subject to change without notice.

1.2.1 Feature Overview

The MCF52235 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 60 MHz processor core frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
  - Cryptography Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - FIPS-140 compliant random number generator
  - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - Up to 32 Kbytes of dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 256 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- Fast Ethernet Controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- On-chip Ethernet Transceiver (EPHY)
  - Digital adaptive equalization
  - Supports auto-negotiation
  - Baseline wander correction
  - Full-/Half-duplex support in all modes
  - Loopback modes
  - Supports MDIO preamble suppression
  - Jumbo packet
- FlexCAN 2.0B module

  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0–8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused Message Buffer space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores required
  - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O

- Four 32-bit DMA timers
  - 17-ns resolution at 60 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timers
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - Crystal input
  - On-chip PLL
  - Provides clock for integrated EPHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals

  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of three clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic

pipeline, optimized for 16×16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, access debug information and real-time tracing capability is provided on 112-and 121-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF52235 implements revision B+ of the ColdFire Debug Architecture.

The MCF52235's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF52235 includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 112 and 121-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The MCF52235 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF52235 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF52235 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF52235 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 16- or 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16- or 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM

module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32 K×16-bit flash arrays to generate 256 Kbytes of 32-bit flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle flash arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash programming interface that allows the flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips. This allows easy device programming via Automated Test Equipment or bulk programming tools.

1.2.6 Cryptography Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The MCF52235 incorporates several low-power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.9 UARTs

The MCF52235 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.10 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices on a circuit board.

1.2.11 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.12 Fast ADC

The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 10- or 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.13 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the each device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.14 General Purpose Timer (GPT)

The general purpose timer (GPT) is a 4-channel timer module consisting of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.15 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or can be a free-running down-counter.

1.2.16 Pulse Width Modulation (PWM) Timers

The MCF52235 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0 to 100%. The PWM outputs have programmable polarity and can be programmed as left-aligned outputs or center-aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.19 Interrupt Controller (INTC0/INTC1)

There are two interrupt controllers on the MCF52235. These interrupt controllers are organized as seven levels with up to nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and provide each peripheral with all necessary interrupts. Each internal interrupt has a programmable level [1-7] and priority within the level. The seven external interrupts have fixed levels/priorities.

1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software

- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.2.22 GPIO

Nearly all pins on the MCF52235 have general purpose I/O capability in addition to their primary functions and are grouped into 8-bit ports. Some ports do not utilize all 8 bits. Each port has registers that configure, monitor, and control the port pins.

1.2.23 Part Numbers and Packaging

Table 2. Orderable Part Number Summary

Freescale Part Number	Description	Speed (MHz)	Flash/SRAM (Kbytes)	Package	Temp range (°C)
MCF52230CAF60	MCF52230 Microcontroller	60	128 / 32	80 LQFP	-40 to +85
MCF52230CAL60	MCF52230 Microcontroller	60	128 / 32	112 LQFP	-40 to +85
MCF52231CAF60	MCF52231 Microcontroller, FlexCAN	60	128 / 32	80 LQFP	-40 to +85
MCF52231CAL60	MCF52231 Microcontroller, FlexCAN	60	128 / 32	112 LQFP	-40 to +85
MCF52232CAF50	MCF52232 Microcontroller	50	128 / 32	80 LQFP	-40 to +85
MCF52232AF50	MCF52232 Microcontroller	50	128 / 32	80 LQFP	0 to +70
MCF52233CAF60	MCF52233 Microcontroller	60	256 / 32	80 LQFP	-40 to +85
MCF52233CAL60	MCF52233 Microcontroller	60	256 / 32	112 LQFP	-40 to +85
MCF52233CAL60A	MCF52233 Microcontroller	60	256 / 32	112 LQFP	-40 to +85
MCF52233CVM60	MCF52233 Microcontroller	60	256 / 32	121 MAPBGA	-40 to +85
MCF52234CAL60	MCF52234 Microcontroller, FlexCAN	60	256 / 32	112 LQFP	-40 to +85
MCF52234CVM60	MCF52234 Microcontroller, FlexCAN	60	256 / 32	121 MAPBGA	-40 to +85
MCF52235CAL60	MCF52235 Microcontroller, FlexCAN, CAU, RNGA	60	256 / 32	112 LQFP	-40 to +85
MCF52235CAL60A	MCF52235 Microcontroller, FlexCAN, CAU, RNGA	60	256 / 32	112 LQFP	-40 to +85
MCF52235CVM60	MCF52235 Microcontroller, FlexCAN, CAU, RNGA	60	256 / 32	121 MAPBGA	-40 to +85
MCF52236CAF50	MCF52236 Microcontroller	50	256 / 32	80 LQFP	-40 to +85
MCF52236AF50	MCF52236 Microcontroller	50	256 / 32	80 LQFP	0 to +70
MCF52236AF50A	MCF52236 Microcontroller	50	256 / 32	80 LQFP	0 to +70

1.2.24 Package Pinouts

Figure 2 shows the pinout configuration for the 80-pin LQFP.

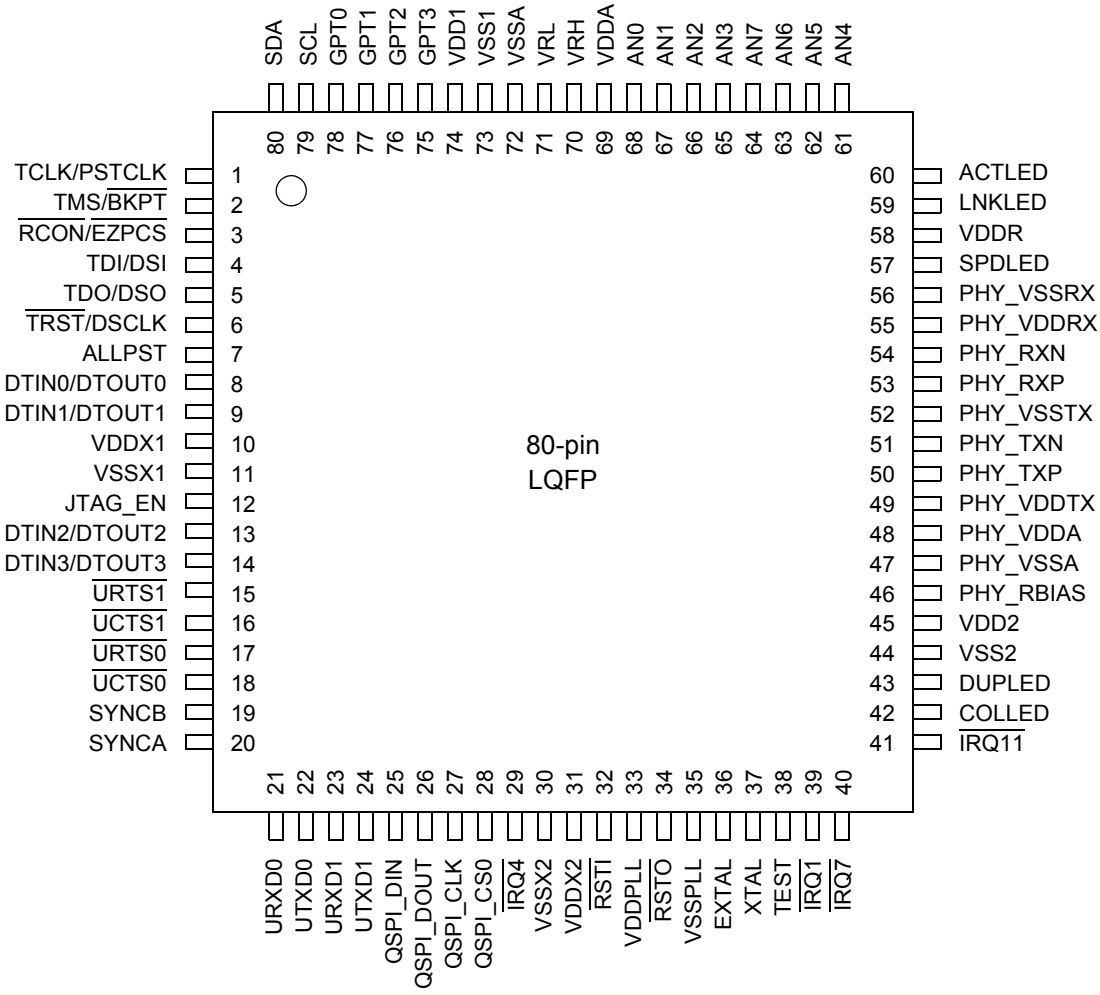


Figure 2. 80-pin LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 112-pin LQFP.

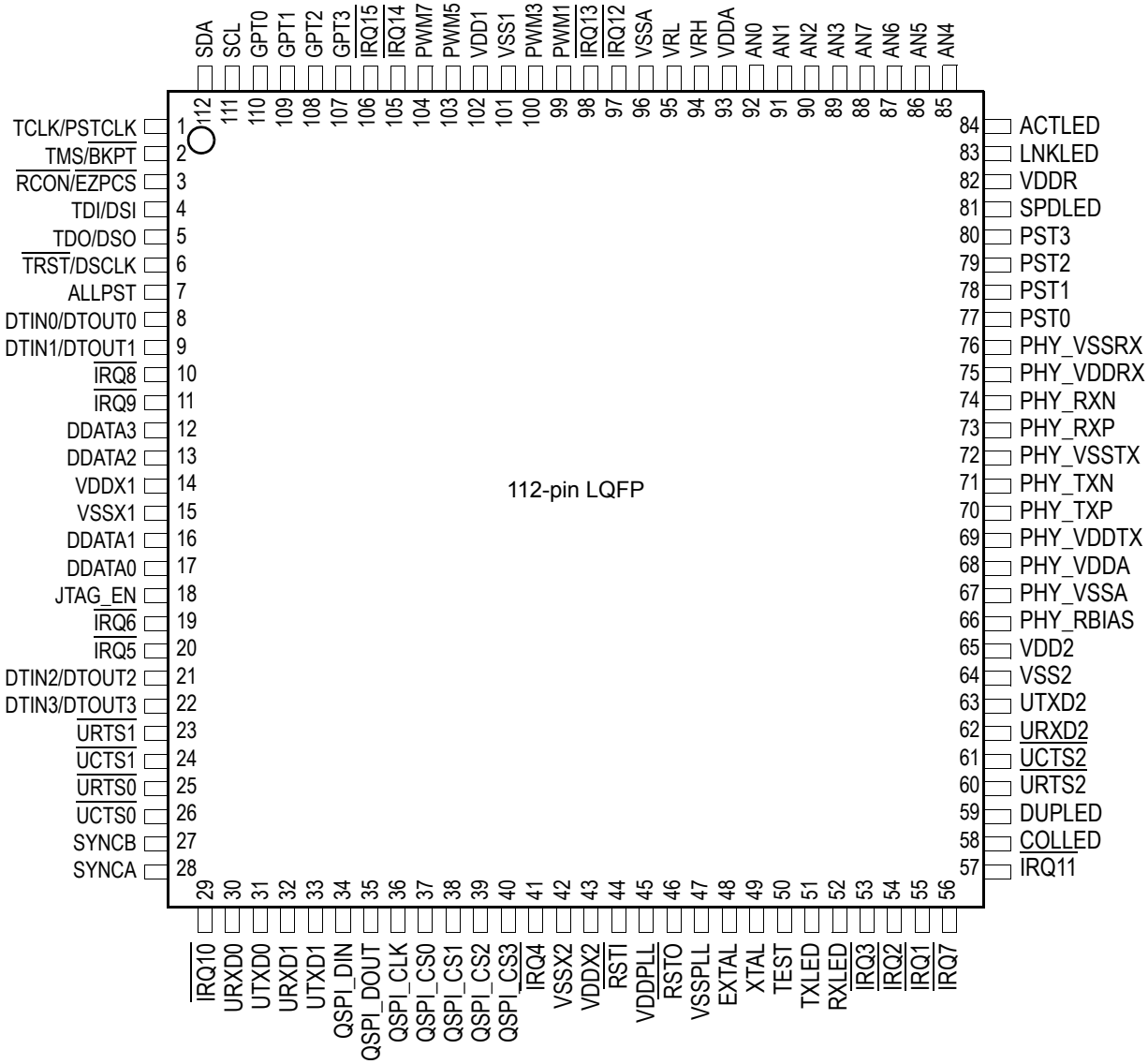


Figure 3. 112-pin LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 121 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11
A	TCLK	SDA	SCL	$\overline{\text{IRQ15}}$	$\overline{\text{IRQ14}}$	$\overline{\text{IRQ13}}$	VSSA	VDDA	AN1	AN7	AN5
B	TMS	$\overline{\text{RCON}}$	GPT0	GPT3	PWM5	PWM1	VRL	VRH	AN2	AN6	AN4
C	$\overline{\text{TRST}}$	TDO	TDI	GPT2	PWM7	PWM3	$\overline{\text{IRQ12}}$	AN0	AN3	LNKLED	ACTLED
D	DTIN1	DTIN0	ALLPST	GPT1	VDDX	VDDX	VDD	VDDR	PST2	PST3	SPDLED
E	DDATA3	$\overline{\text{IRQ9}}$	$\overline{\text{IRQ8}}$	VSS	VSS	VDDX	VSS	VDD	PST0	PST1	PHY_RXN
F	DDATA0	DDATA1	DDATA2	VSS	VSS	VSS	VSS	VSS	PHY_VSSRX	PHY_VDDRX	PHY_RXP
G	DTIN2	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	JTAG_EN	VDDX	VDDX	VDDX	PHY_VSSA	PHY_VSSTX	PHY_VDDTX	PHY_TXP
H	DTIN3	$\overline{\text{URTS0}}$	$\overline{\text{URTS1}}$	QSPI_DIN	QSPI_CS1	VDDX	TEST	TXLED	RXLED	PHY_VDDA	PHY_TXN
J	SYNCB	$\overline{\text{UCTS0}}$	$\overline{\text{UCTS1}}$	QSPI_DOUT	QSPI_CS2	$\overline{\text{RSTI}}$	XTAL	$\overline{\text{IRQ1}}$	COLLED	DUPLED	PHY_RBIAS
K	SYNCA	URXD0	URXD1	QSPI_CLK	QSPI_CS3	VDDPLL	VSSPLL	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ11}}$	$\overline{\text{URTS2}}$	URXD2
L	$\overline{\text{IRQ10}}$	UTXD0	UTXD1	QSPI_CS0	$\overline{\text{IRQ4}}$	$\overline{\text{RSTO}}$	EXTAL	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ7}}$	$\overline{\text{UCTS2}}$	UTXD2

Figure 4. 121 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
ADC[3]	AN7	—	—	PAN[7]	Low	—	—	A10	88	64
	AN6	—	—	PAN[6]	Low	—	—	B10	87	63
	AN5	—	—	PAN[5]	Low	—	—	A11	86	62
	AN4	—	—	PAN[4]	Low	—	—	B11	85	61
	AN3	—	—	PAN[3]	Low	—	—	C9	89	65
	AN2	—	—	PAN[2]	Low	—	—	B9	90	66
	AN1	—	—	PAN[1]	Low	—	—	A9	91	67
	AN0	—	—	PAN[0]	Low	—	—	C8	92	68
	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	K1	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	J1	27	19
	VDDA	—	—	—	N/A	N/A	—	A8	93	69
	VSSA	—	—	—	N/A	N/A	—	A7	96	72
	VRH	—	—	—	N/A	N/A	—	B8	94	70
	VRL	—	—	—	N/A	N/A	—	B7	95	71
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	L7	48	36
	XTAL	—	—	—	N/A	N/A	—	J7	49	37
	VDDPLL[5]	—	—	—	N/A	N/A	—	K6	45	33
	VSSPLL	—	—	—	N/A	N/A	—	K7	47	35
Debug Data	ALLPST	—	—	—	High	—	—	D3	7	7
	DDATA[3:0]	—	—	PDD[7:4]	High	—	—	E1, F3,F2, F1	12,13,16,17	—
	PST[3:0]	—	—	PDD[3:0]	High	—	—	D10, D9, E10, E9	80,79,78,77	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Ethernet LEDs	ACTLED	—	—	PLD[0]	PDSR[32]	PWOR[8]	—	C11	84	60
	COLLED	—	—	PLD[4]	PDSR[36]	PWOR[12]	—	J9	58	42
	DUPLED	—	—	PLD[3]	PDSR[35]	PWOR[11]	—	J10	59	43
	LNKLED	—	—	PLD[1]	PDSR[33]	PWOR[9]	—	C10	83	59
	SPDLED	—	—	PLD[2]	PDSR[34]	PWOR[10]	—	D11	81	57
	RXLED	—	—	PLD[5]	PDSR[37]	PWOR[13]	—	H9	52	—
	TXLED	—	—	PLD[6]	PDSR[38]	PWOR[14]	—	H8	51	—
	VDDR	—	—	—	—	—	—	D8	82	58
Ethernet PHY	PHY_RBIAS	—	—	—	—	—		J11	66	46
	PHY_RXN	—	—	—	—	—		E11	74	54
	PHY_RXP	—	—	—	—	—		F11	73	53
	PHY_TXN	—	—	—	—	—		H11	71	51
	PHY_TXP	—	—	—	—	—		G11	70	50
	PHY_VDDA[5]	—	—	—		N/A		H10	68	48
	PHY_VDDRX[5]	—	—	—		N/A		F10	75	55
	PHY_VDDTX[5]	—	—	—		N/A		G10	69	49
	PHY_VSSA	—	—	—		N/A		G8	67	47
	PHY_VSSRX	—	—	—		N/A		F9	76	56
	PHY_VSSTX	—	—	—		N/A		G9	72	52
I^2C	SCL	CANTX[4]	UTXD2	PAS[0]	PDSR[0]	—	Pull-Up[6]	A3	111	79
	SDA	CANRX[4]	URXD2	PAS[1]	PDSR[0]	—	Pull-Up[6]	A2	112	80
Interrupts[3]	IRQ15	—	—	PGP[7]	PSDR[47]	—	Pull-Up[6]	A4	106	—
	IRQ14	—	—	PGP[6]	PSDR[46]	—	Pull-Up[6]	A5	105	—
	IRQ13	—	—	PGP[5]	PSDR[45]	—	Pull-Up[6]	A6	98	—
	IRQ12	—	—	PGP[4]	PSDR[44]	—	Pull-Up[6]	C7	97	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Continued Interrupts[3]	IRQ11	—	—	PGP[3]	PSDR[43]	—	Pull-Up[6]	K9	57	41
	IRQ10	—	—	PGP[2]	PSDR[42]	—	Pull-Up[6]	L1	29	—
	IRQ9	—	—	PGP[1]	PSDR[41]	—	Pull-Up[6]	E2	11	—
	IRQ8	—	—	PGP[0]	PSDR[40]	—	Pull-Up	E3	10	—
	IRQ7	—	—	PNQ[7]	Low	—	Pull-Up[6]	L9	56	40
	IRQ6	—	FEC_RXER	PNQ[6]	Low	—	Pull-Up[6]	G3	19	—
	IRQ5	—	FEC_RXD[1]	PNQ[5]	Low	—	Pull-Up[6]	G2	20	—
	IRQ4	—	—	PNQ[4]	Low	—	Pull-Up[6]	L5	41	29
	IRQ3	—	FEC_RXD[2]	PNQ[3]	Low	—	Pull-Up[6]	L8	53	—
	IRQ2	—	FEC_RXD[3]	PNQ[2]	Low	—	Pull-Up[6]	K8	54	—
	IRQ1	SYNCA	PWM1	PNQ[1]	High	—	Pull-Up[6]	J8	55	39
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	G4	18	12
	TCLK/ PSTCLK	CLKOUT	—	—	High	—	Pull-Up[7]	A1	1	1
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[7]	C3	4	4
	TDO/DSO	—	—	—	High	N/A	—	C2	5	5
	TMS/$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	Pull-Up[7]	B1	2	2
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up	C1	6	6
Mode Selection	$\overline{\text{RCON}}$/EZPCS	—	—	—	N/A	N/A	Pull-Up	B2	3	3
PWM	PWM7	—	—	PTD[3]	PDSR[31]	—	—	C5	104	—
	PWM5	—	—	PTD[2]	PDSR[30]	—	—	B5	103	—
	PWM3	—	—	PTD[1]	PDSR[29]	—	—	C6	100	—
	PWM1	—	—	PTD[0]	PDSR[28]	—	—	B6	99	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
QSPI[3]	QSPI_DIN/ EZPD	CANRX[4]	URXD1	PQS[1]	PDSR[2]	PWOR[4]	—	H4	34	25
	QSPI_DOUT/EZPQ	CANTX[4]	UTXD1	PQS[0]	PDSR[1]	PWOR[5]	—	J4	35	26
	QSPI_CLK/ EZPCK	SCL	URTS1	PQS[2]	PDSR[3]	PWOR[6]	Pull-Up[8]	K4	36	27
	QSPI_CS3	SYNCA	SYNCB	PQS[6]	PDSR[7]	—	—	K5	40	—
	QSPI_CS2	—	FEC_TXCLK	PQS[5]	PDSR[6]	—	—	J5	39	—
	QSPI_CS1	—	FEC_TXEN	PQS[4]	PDSR[5]	—	—	H5	38	—
	QSPI_CS0	SDA	UCTS1	PQS[3]	PDSR[4]	PWOR[7]	Pull-Up[8]	L4	37	28
Reset[9]	RSTI	—	—	—	N/A	N/A	Pull-Up[9]	J6	44	32
	RSTO	—	—	—	high	—	—	L6	46	34
Test	TEST	—	—	—	N/A	N/A	Pull-Down	H7	50	38
Timers, 16-bit[3]	GPT3	FEC_TXD[3]	PWM7	PTA[3]	PDSR[23]	—	Pull-Up[10]	B4	107	75
	GPT2	FEC_TXD[2]	PWM5	PTA[2]	PDSR[22]	—	Pull-Up[10]	C4	108	76
	GPT1	FEC_TXD[1]	PWM3	PTA[1]	PDSR[21]	—	Pull-Up[10]	D4	109	77
	GPT0	FEC_TXER	PWM1	PTA[0]	PDSR[20]	—	Pull-Up[10]	B3	110	78
Timers, 32-bit	DTIN3	DTOUT3	PWM6	PTC[3]	PDSR[19]	—	—	H1	22	14
	DTIN2	DTOUT2	PWM4	PTC[2]	PDSR[18]	—	—	G1	21	13
	DTIN1	DTOUT1	PWM2	PTC[1]	PDSR[17]	—	—	D1	9	9
	DTIN0	DTOUT0	PWM0	PTC[0]	PDSR[16]	—	—	D2	8	8
UART 0[3]	$\overline{\text{UCTS0}}$	CANRX[4]	FEC_RXCLK	PUA[3]	PDSR[11]	—	—	J2	26	18
	$\overline{\text{URTS0}}$	CANTX[4]	FEC_RXDV	PUA[2]	PDSR[10]	—	—	H2	25	17
	URXD0	—	FEC_RXD[0]	PUA[1]	PDSR[9]	PWOR[0]	—	K2	30	21
	UTXD0	—	FEC_CRS	PUA[0]	PDSR[8]	PWOR[1]	—	L2	31	22

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
UART 1[3]	$\overline{\text{UCTS1}}$	SYNCA	URXD2	PUB[3]	PDSR[15]	—	—	J3	24	16
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	PUB[2]	PDSR[14]	—	—	H3	23	15
	URXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	K3	32	23
	UTXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	L3	33	24
UART 2	$\overline{\text{UCTS2}}$	—	—	PUC[3]	PDSR[27]	—	—	L10	61	—
	$\overline{\text{URTS2}}$	—	—	PUC[2]	PDSR[26]	—	—	K10	60	—
	URXD2	—	—	PUC[1]	PDSR[25]	—	—	K11	62	—
	UTXD2	—	—	PUC[0]	PDSR[24]	—	—	L11	63	—
FlexCAN	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19
VDD[5,11]	VDD	—	—	—	N/A	N/A	—	D7, E8	65,102	45,74
VDDX	VDDX	—	—	—	N/A	N/A	—	D5, D6, E6, G5, G6, G7, H6	14, 43	10, 31
VSS	VSS	—	—	—	N/A	N/A	—	E4, E5, E7,F4, F5, F6, F7, F8	64,101	44,73
VSSX	VSSX	—	—	—	N/A	N/A	—	—	15, 42	11, 30

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

1.3 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input.	I
Crystal	XTAL	Crystal oscillator output.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	—
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

1.6 External Interrupt Signals

Table 7 describes the external interrupt signals.

Table 7. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[15:1]	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 8 describes QSPI signals.

Table 8. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.8 Fast Ethernet Controller EPHY Signals

Table 9 describes the Fast Ethernet Controller (FEC) signals.

Table 9. Fast Ethernet Controller (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Twisted Pair Input +	RXP	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Input -	RXN	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Output +	TXN	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Twisted Pair Output -	TXP	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Bias Control Resistor	RBIAS	Connect a 12.4 kΩ (1.0%) external resistor, RBIAS, between the PHY_RBIAS pin and analog ground. Place this resistor as near to the chip pin as possible. Stray capacitance must be kept to less than 10 pF (>50 pF causes instability). No high-speed signals can be permitted in the region of RBIAS.	I
Activity LED	ACT_LED	Indicates when the EPHY is transmitting or receiving	O
Link LED	LINK_LED	Indicates when the EPHY has a valid link	O
Speed LED	SPD_LED	Indicates the speed of the EPHY connection	O
Duplex LED	DUPLED	Indicates the duplex (full or half) of the EPHY connection	O
Collision LED	COLLED	Indicates if the EPHY detects a collision	O
Transmit LED	TXLED	Indicates if the EPHY is transmitting	O
Receive LED	RXLED	Indicates if the EPHY is receiving	O

1.9 I^2C I/O Signals

Table 10 describes the I^2C serial interface module signals.

Table 10. I^2C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I^2C interface. Either it is driven by the I^2C module when the bus is in master mode or it becomes the clock input when the I^2C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I^2C interface.	I/O

1.10 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.11 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN*n*	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT*n*	Programmable output from the DMA timer modules.	O

1.12 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the A-to-D converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise	—
	V_{SSA}		—

1.13 General Purpose Timer Signals

Table 14 describes the General Purpose Timer Signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purppose timer module	I/O

1.14 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels	O

1.15 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock. Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint. Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals (PST[3:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input. Internally synchronized input that provides data input for the serial communication port to the debug module after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output. Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock. Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, PST, and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be re-enabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	—

Some of the V_{DD} and V_{SS} pins on the device are only to be used for noise bypass. Figure 5 shows a typical connection diagram. Pay particular attention to those pins which show only capacitor connections. Do not connect power supply voltage directly to these pins.

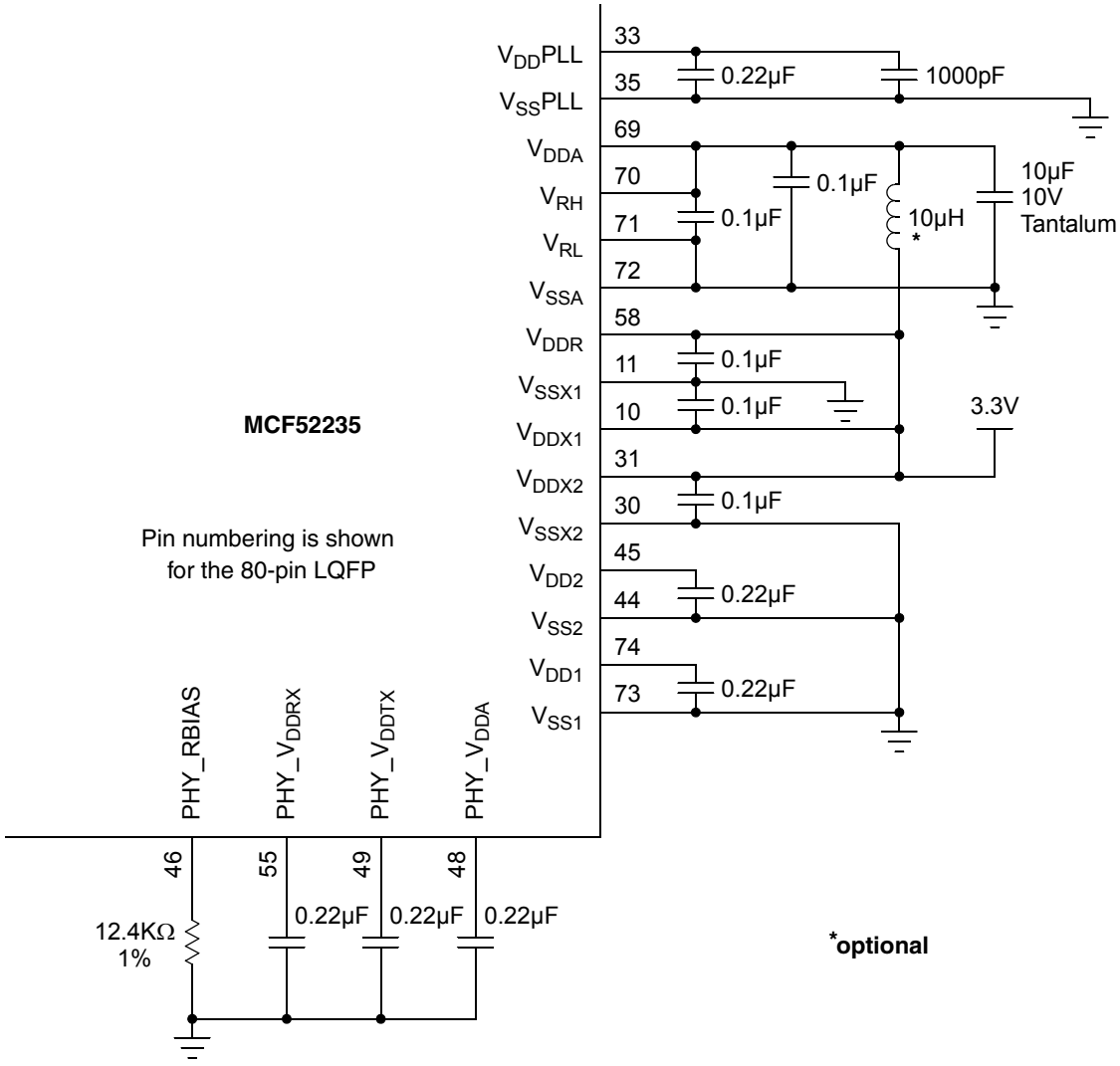


Figure 5. Suggested Connection Scheme for Power and Ground

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF52235, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3 Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values.

NOTE

The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

Table 20. Thermal Characteristics

Characteristic	Symbol	Package[1]	Value	Unit
Junction to ambient, natural convection	θ_{JA}	80-pin LQFP, four-layer board	36.0[2,3]	°C/W
		112-pin LQFP, four-layer board	35.0	
		121 MAPBGA, four-layer board	32	
		80-pin LQFP, one-layer board[1]	49.0[1]	
		121 MAPBGA, one-layer board[1]	56[1]	
		112-pin LQFP, one-layer board[1]	44.0[1]	
Junction to ambient (@200 ft/min)	θ_{JMA}	80-pin LQFP, four-layer board	30.0	°C/W
		112-pin LQFP, four-layer board	29.0	
		121 MAPBGA, four-layer board	28	
		80-pin LQFP, one-layer board[1]	39.0[1]	
		112-pin LQFP, one-layer board[1]	35.0[1]	
		121 MAPBGA, one-layer board[1]	46[1]	
Junction to board	θ_{JB}	80-pin LQFP	22.0[4]	°C/W
		112-pin LQFP	23.0	
		121 MAPBGA, four-layer board	18	
Junction to case	θ_{JC}	80-pin LQFP	6.0[5]	°C/W
		112-pin LQFP	6.0	
		121 MAPBGA	10	
Junction to top of package, natural convection	Ψ_{jt}	80-pin LQFP	2.0[6]	°C/W
		112-pin LQFP	2.0[6]	
		121 MAPBGA	2.0[6]	
Maximum operating junction temperature	T_j	All	130	°C

1 The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

2 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JMA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

where

- T_A = ambient temperature, °C
- Θ_{JMA} = package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$
- P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
- $P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications, PI/O < P_{INT} and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.2 ESD Protection

Table 21. ESD Protection Characteristics[1]

Characteristic	Symbol	Value	Units
ESD target for Human Body Model	HBM	1500 (ADC and EPHY pins) 2000 (All other pins)	V
ESD target for Charged Device Model	CDM	250	V
HBM circuit description	R_{series}	1500	ohms
	C	100	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (CDM) positive pulses negative pulses	 — —	 3 3	—
Interval of pulses (HBM)	—	1.0	sec
Interval of pulses (CDM)	—	0.2	sec

[1] A device is defined as a failure if the device no longer meets the device specification requirements after exposure to ESD pulses. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{in}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Weak internal pull-up device current, tested at V_{IL} max.[2]	I_{APU}	–10	–130	µA
Input capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load capacitance[4] Low drive strength High drive strength	C_L		 25 50	pF
DC injection current [3, 5, 6, 7] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single pin limit Total MCU limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

Table 23. Active Current Consumption Specifications

Characteristic	Symbol	Typical				Peak	Unit
		Running from SRAM, EPHY Off	Running from Flash, EPHY Off	Running from Flash, EPHY 10BaseT	Running from Flash, EPHY 100BaseT		
Active current, core and I/O PLL @25 MHz PLL @60 MHz	$I_{DDR}+I_{DDX}$ $+I_{DDA}$	 75 130	 82 138	 150 220	 260 310	 290 340	 mA
Analog supply current Normal operation Low-power STOP	I_{DDA}	 20 15	 20 15	 20 15	 20 15	 30 50	 mA μA

Table 24. Current Consumption Specifications in Low-Power Modes[1]

Mode[2]	PLL @25 MHz (typical)[3]	PLL @60 MHz (typical)[3]	PLL @60 MHz (peak)[4]	Unit
STOP mode 3 (STPMD[1:0]=11)	0.2		1.0	mA
STOP mode 2 (STPMD[1:0]=10)	7		—	
STOP mode 1 (STPMD[1:0]=01)	10	12	—	
STOP mode 0 (STPMD[1:0]=00)	10	12	—	
WAIT	16	27	—	
DOZE	16	27	—	
RUN	25	45	—	

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

2.4 Phase Lock Loop Electrical Specifications

Table 25. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 0.5 0	 25.0 60.0	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [2] External clock mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} 3.0[7]	V
EXTAL input low voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V
XTAL output high voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD} –1.0	 —	V
XTAL output low voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL load capacitance[8]		—	—	pF
PLL lock time[5,9]	t_{lpll}	—	500	µs
Power-up to lock time [5, 7,9] With crystal reference Without crystal reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	fLCK	–0.75	0.75	% f_{sys}
CLKOUT period Jitter [5, 6, 8, 10,11], measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over 2 ms interval)	C_{jitter}	 — —	 10 0.01	% f_{sys}

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 All internal registers retain data at 0 Hz.

3 Loss of reference frequency is the reference frequency detected internally that transitions the PLL into self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

[7] This value has been updated

[8] Load capacitance determined from crystal manufacturer specifications and include circuit board parasitics.

[9] Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTO}$ negating. If the crystal oscillator is the reference for the PLL, the crystal start up time must be added to the PLL lock time to determine the total start-up time.

[10] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval

[11] Based on slow system clock of 40 MHz measured at f_{sys} max.

2.5 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, timers, UARTs, FEC, and interrupts. When in GPIO mode, the timing specification for these pins is given in Table 26 and Figure 6.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 26. GPIO Timing

Num	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT high to GPIO output valid	t_{CHPOV}	—	10	ns
G2	CLKOUT high to GPIO output invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO input valid to CLKOUT high	t_{PVCH}	9	—	ns
G4	CLKOUT high to GPIO input invalid	t_{CHPI}	1.5	—	ns

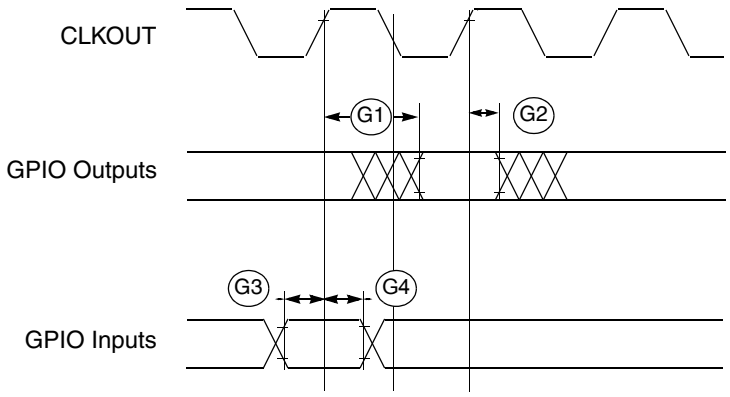


Figure 6. GPIO Timing

2.6 Reset Timing

Table 27. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT high	t_{RVCH}	9	—	ns
R2	CLKOUT high to $\overline{\text{RSTI}}$ input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT high to $\overline{\text{RSTO}}$ valid	t_{CHROV}	—	10	ns

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Therefore, $\overline{\text{RSTI}}$ must be held a minimum of 100ns.

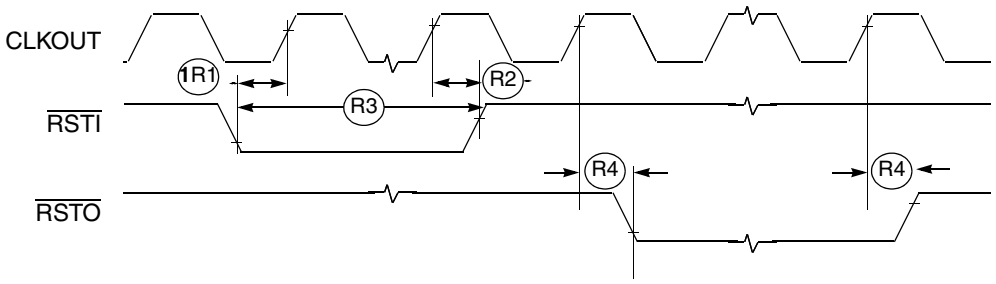


Figure 7. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.7 I²C Input/Output Timing Specifications

Table 28 lists specifications for the I²C input timing parameters shown in Figure 8.

Table 28. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 × t_{CYC}	—	ns
I2	Clock low period	8 × t_{CYC}	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 × t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 × t_{CYC}	—	ns
I9	Stop condition setup time	2 × t_{CYC}	—	ns

Table 29 lists specifications for the I²C output timing parameters shown in Figure 8.

Table 29. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 [1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2 [1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7 [1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 29. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 29 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 8 shows timing for the values in Table 28 and Table 29.

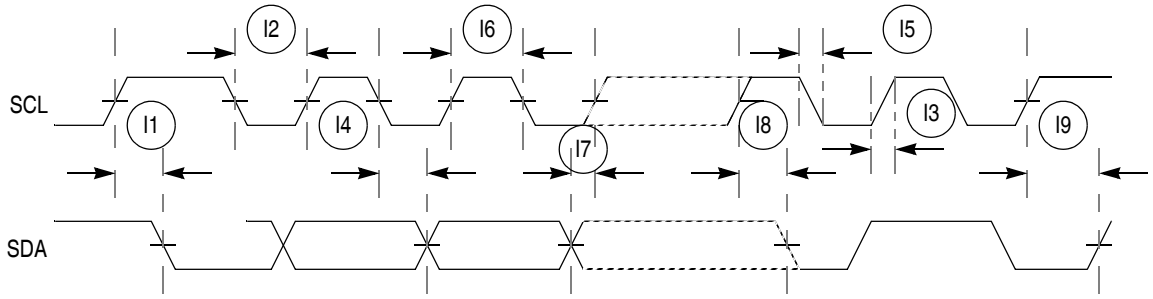


Figure 8. I^2C Input/Output Timings

2.8 EPHY Parameters

2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

Table 30. EPHY Timing Parameters

Num	Characteristic	Symbol	Value	Unit
E1	EPHY startup time	$t_{Start-Up}$	360	µs

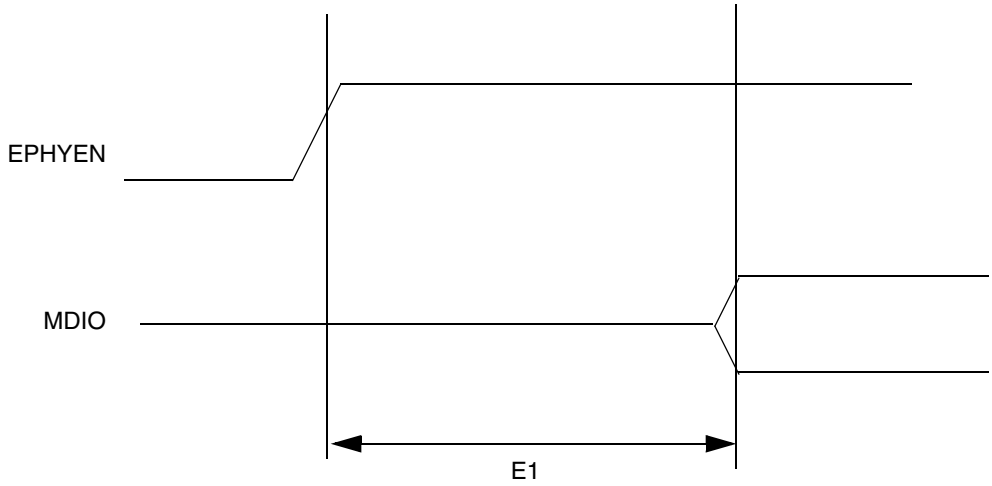


Figure 9. EPHY Timing

2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters

Characteristic	Symbol	Min	Typ[1]	Max	Units
COL (SQE) delay after TXEN off	t1	—	1.0	—	µs
COL (SQE) pulse duration	t2	—	1.0	—	µs

[1] Typical values are at 25°C.

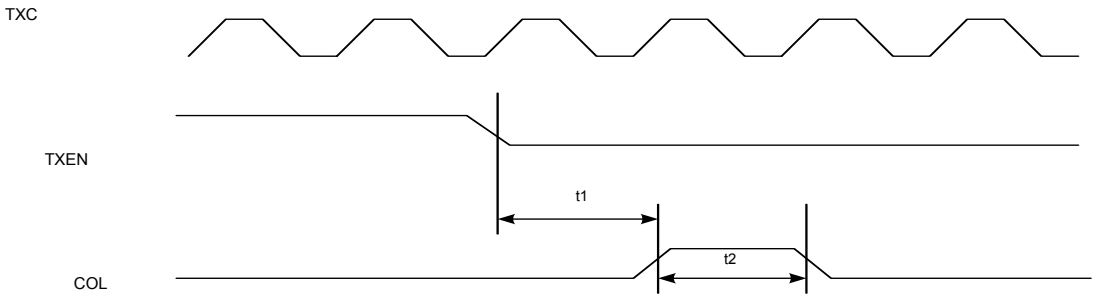


Figure 10. 10BASE-T SQE (Heartbeat) Timing

2.8.3 10BASE-T Jab and Unjab Timing

Table 32 and Figure 11 show the relevant 10BASE-T jab and unjab timing parameters.

Table 32. 10BASE-T Jab and Unjab Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units
Maximum transmit time	t1	—	98	—	ms
Unjab time	t2	—	525	—	ms

1 Typical values are at 25°C.

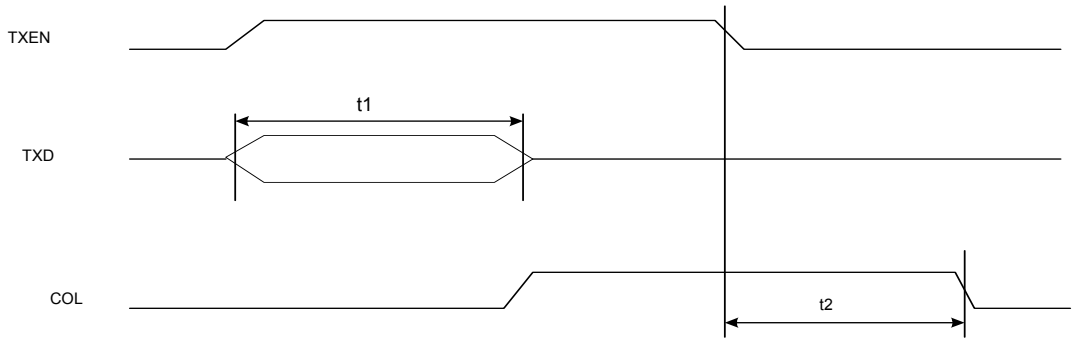


Figure 11. 10BASE-T Jab and Unjab Timing

2.8.4 Transceiver Characteristics

Table 33. 10BASE-T Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak differential output voltage	V_{OP}	2.2	2.5	2.8	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit timing jitter	—	0	2	11	ns	Using line model specified in the IEEE 802.3
Receive dc input impedance	Z_{in}	—	10	—	kΩ	0.0 < V_{in} < 3.3 V
Receive differential squelch level	$V_{squelch}$	300	400	585	mV	3.3 MHz sine wave input

Table 34. 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Transmit Peak Differential Output Voltage	V_{OP}	0.95	1.00	1.05	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit Signal Amplitude Symmetry	V_{sym}	98	100	102	%	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time	t_{rf}	3	4	5	ns	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time Symmetry	t_{rfs}	–0.5	0	+0.5	ns	See IEEE 802.3 for details
Transmit Overshoot/UnderShoot	V_{osh}	—	2.5	5	%	
Transmit Jitter	—	0	.6	1.4	ns	
Receive Common Mode Voltage	V_{cm}	—	1.6	—	V	V_{DDRX} = 2.5 V
Receiver Maximum Input Voltage	V_{max}	—	—	4.7	V	V_{DDRX} = 2.5 V. Internal circuits protected by divider in shutdown

2.9 Analog-to-Digital Converter (ADC) Parameters

Table 35 lists specifications for the analog-to-digital converter.

Table 35. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	Analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
	Monotonicity	Guaranteed			

Table 35. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 12	—	pF
X_{IN}	Input impedance	—	See Figure 12	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±11	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	—	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	75	—	dB
SINAD	Signal-to-noise plus distortion	—	65	—	dB
ENOB	Effective number OF bits	9.1	10.6	—	Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

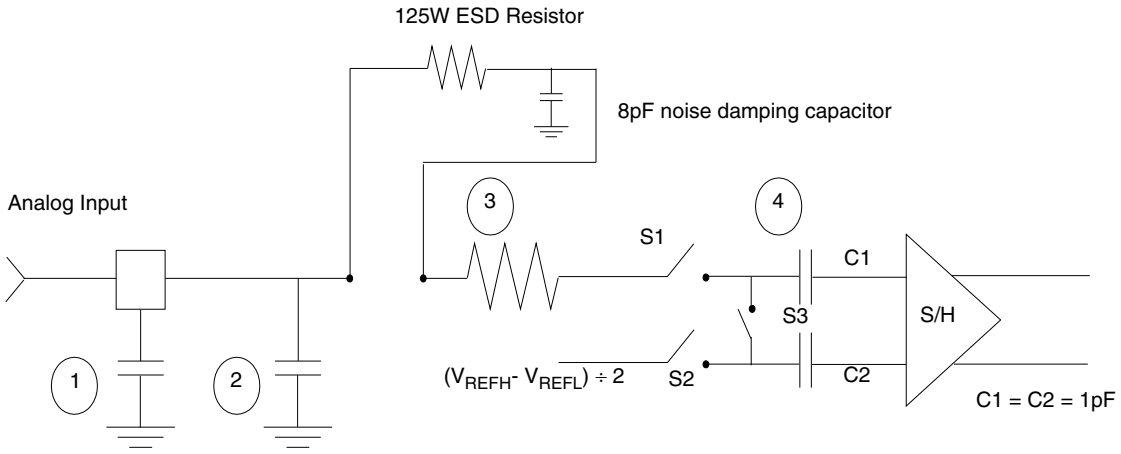
5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.9.1 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an ongoing input current, which is a function of the analog input voltage, V_{REF}, and the ADC clock frequency.



1 Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF

2 Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF

3 Equivalent resistance for the channel select mux; 100 ohms

4 Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF

5 Equivalent input impedance, when the input is selected = $\frac{1}{\text{ADC CLOCK RATE} \times (1.4 \times 10^{-12})}$

Figure 12. Equivalent Circuit for A/D Loading

2.10 DMA Timers Timing Specifications

Table 36 lists timer module AC timings.

Table 36. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

1 All timing references to CLKOUT are given to its rising edge.

2.11 EzPort Electrical Specifications

Table 37. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{cyc}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns

Table 37. EzPort Electrical Specifications (continued)

Name	Characteristic	Min	Max	Unit
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.12 QSPI Electrical Specifications

Table 38 lists QSPI timings.

Table 38. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (input hold)	9	—	ns

The values in Table 38 correspond to Figure 13.

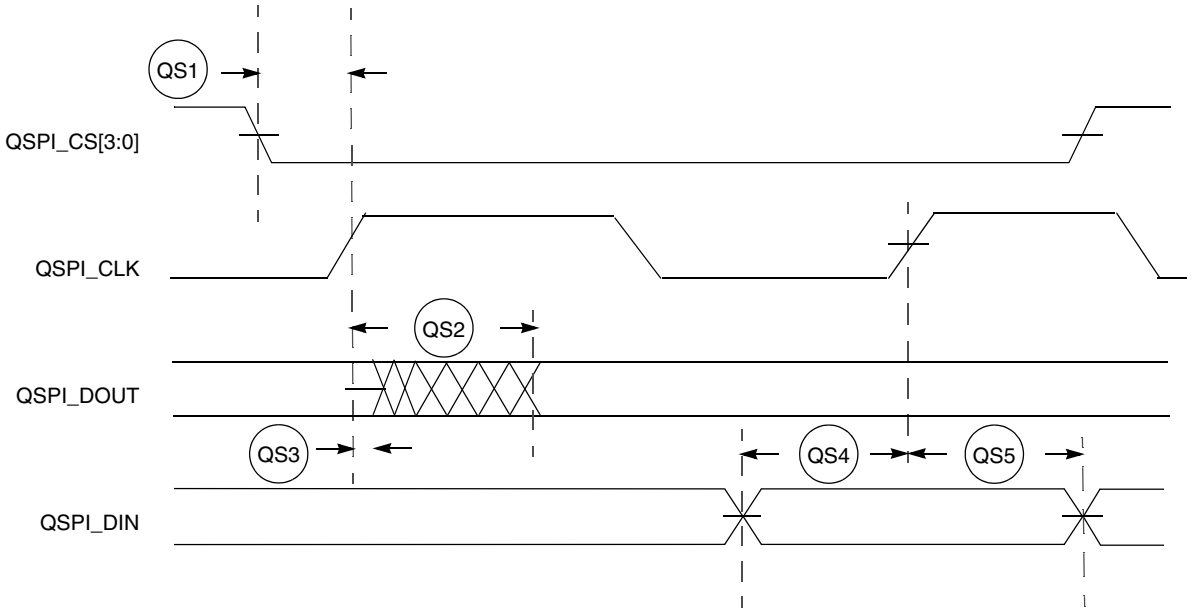


Figure 13. QSPI Timing

2.13 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

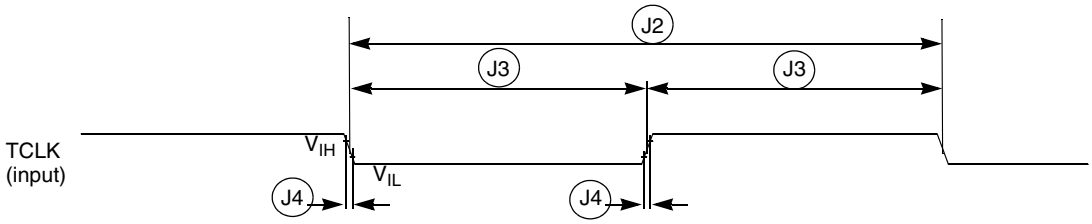


Figure 14. Test Clock Input Timing

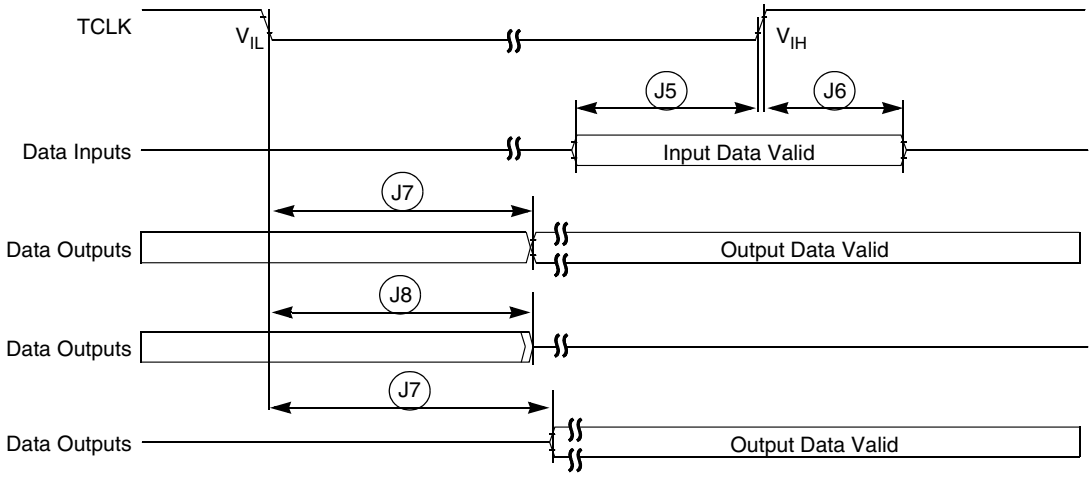


Figure 15. Boundary Scan (JTAG) Timing

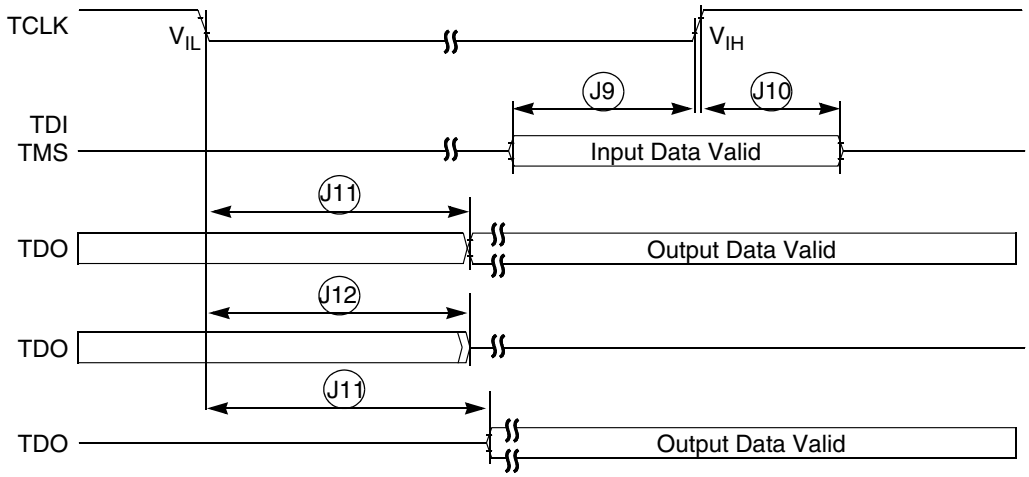


Figure 16. Test Access Port Timing

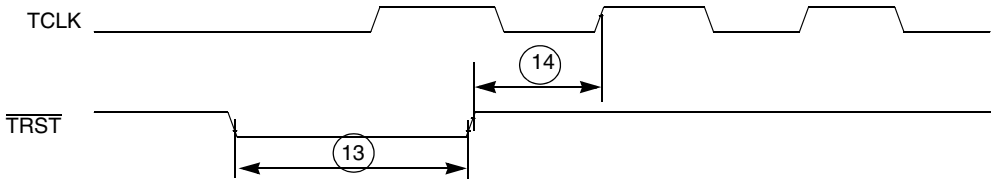


Figure 17. $\overline{\text{TRST}}$ Timing

2.14 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 19.

Table 40. Debug AC Timing Specification

Num	Characteristic	60 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 [1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5	—	ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 18 shows real-time trace timing for the values in Table 40.

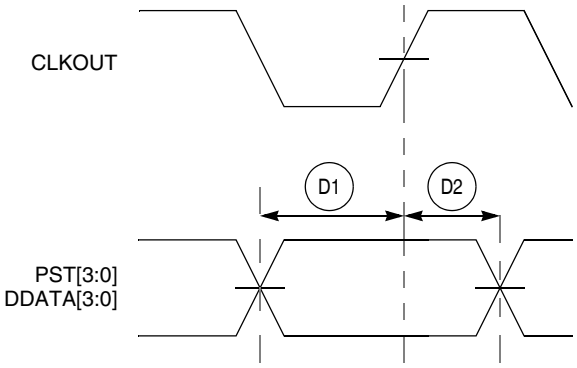


Figure 18. Real-Time Trace AC Timing

Figure 19 shows BDM serial port AC timing for the values in Table 40.

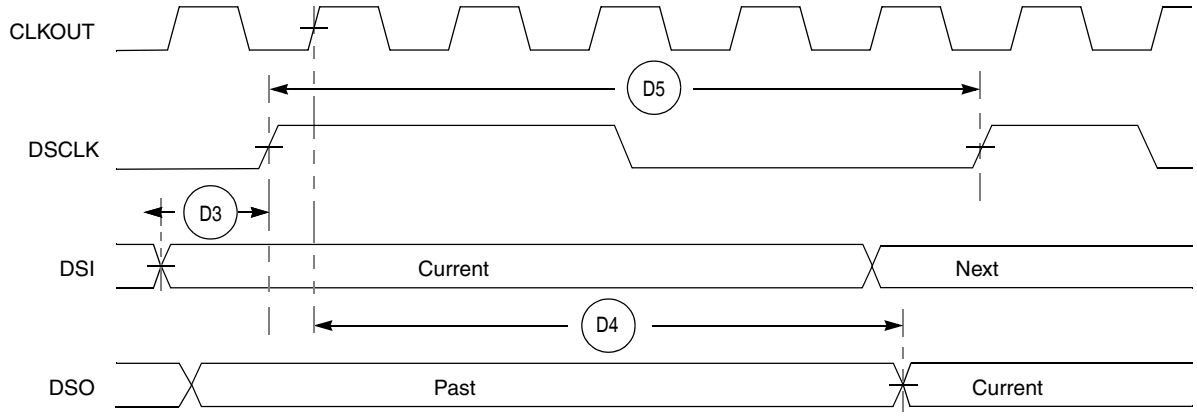
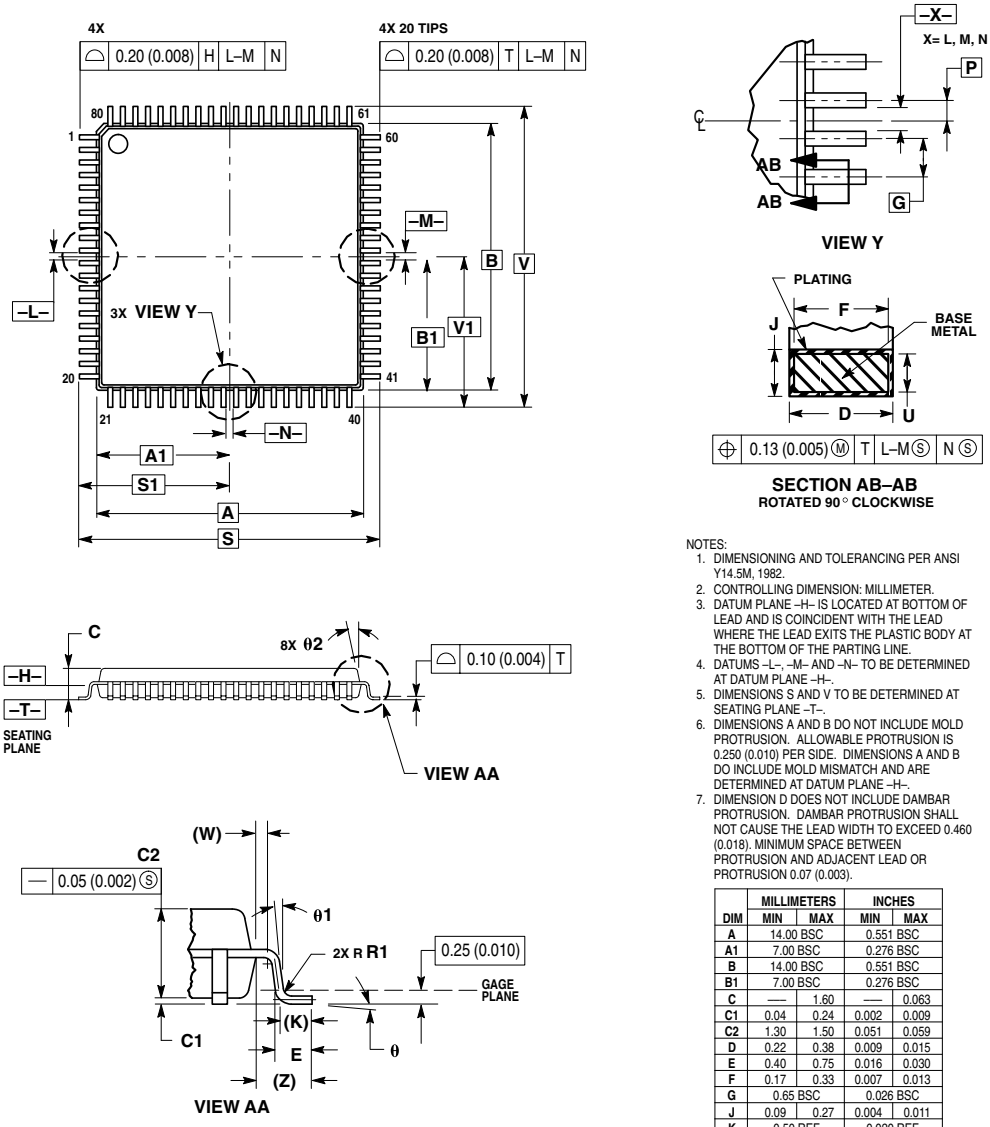


Figure 19. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the MCF52235 and its derivatives.

3.1 80-pin LQFP Package



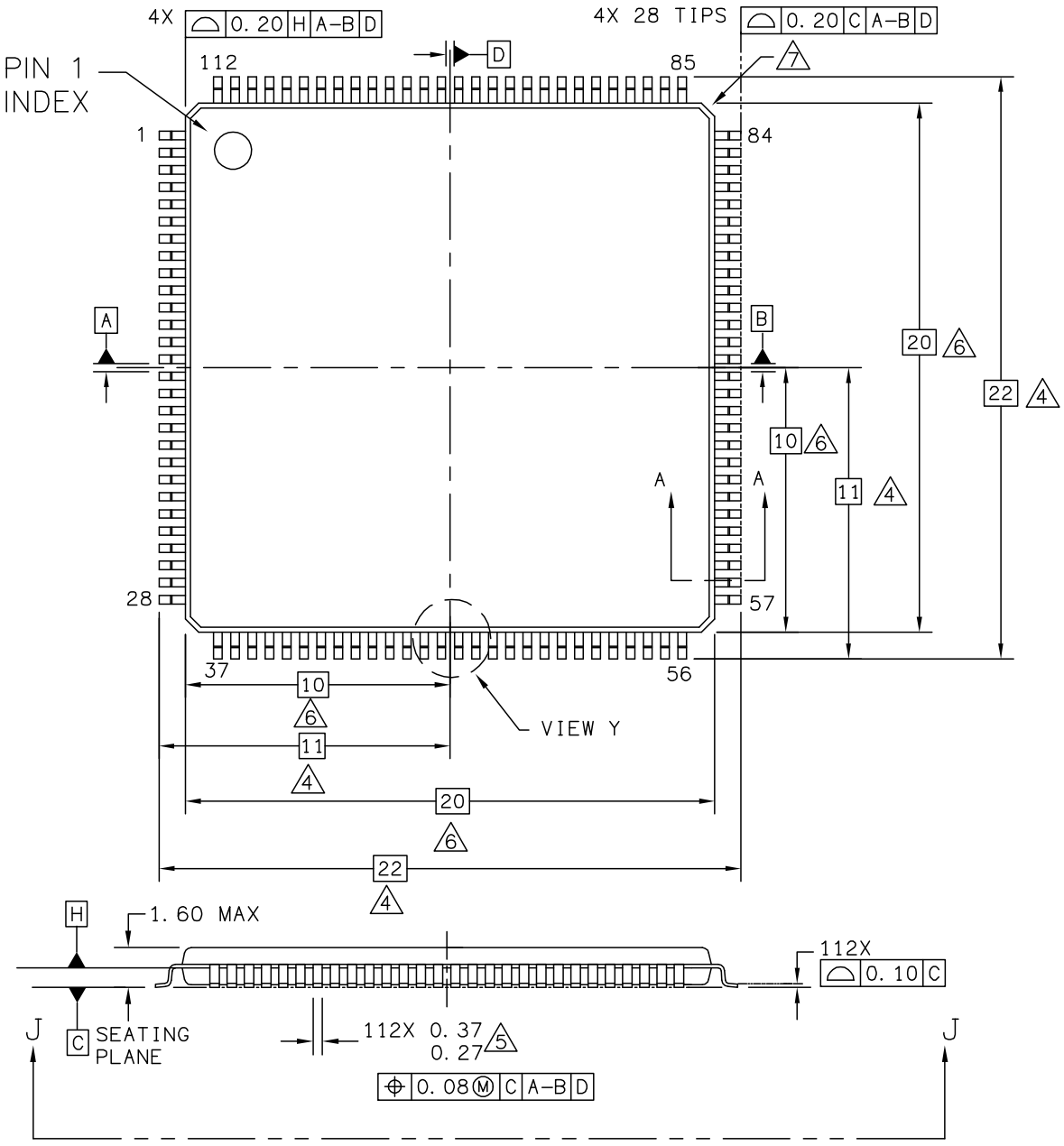
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

CASE 917A–02
ISSUE C

DATE 09/21/95

3.2 112-pin LQFP Package



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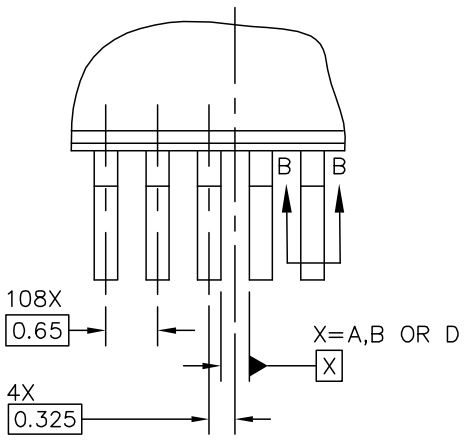
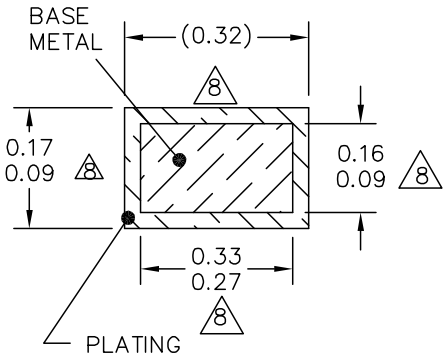
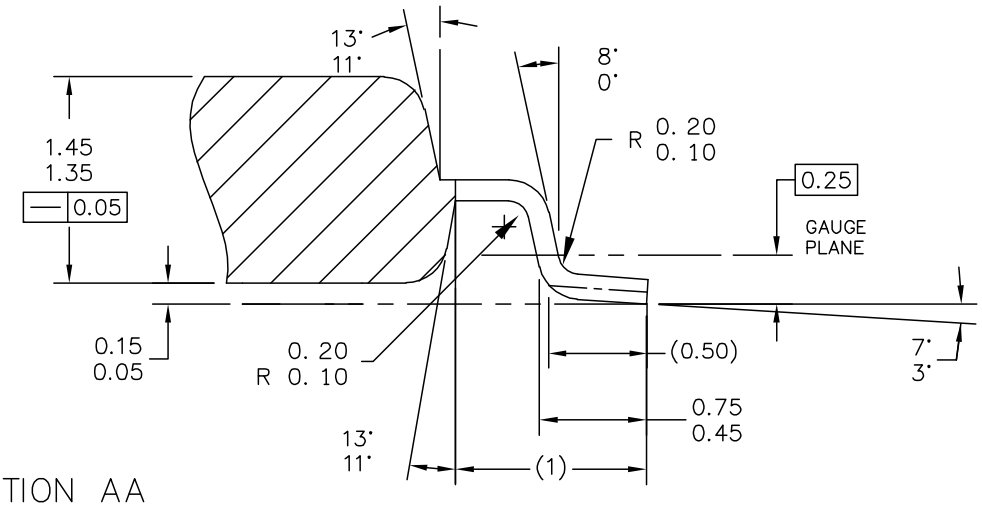
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987-02	25 MAY 2005
	STANDARD: JEDEC MS-026 BFA	



VIEW Y



SECTION B–B



SECTION AA

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TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

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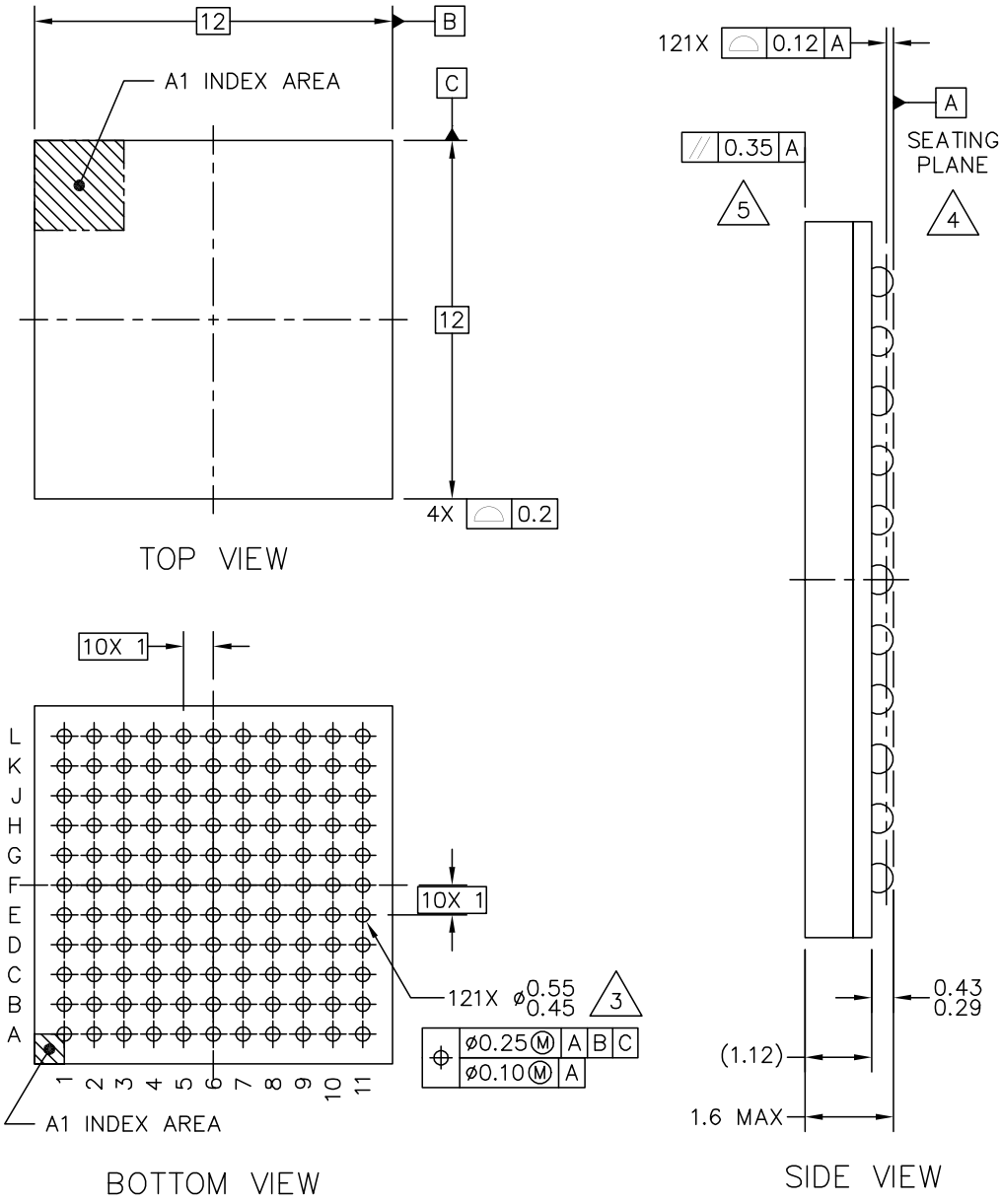
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

3.3 121 MAPBGA Package



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TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts

Table 41. Revision History (continued)

Revision	Description
8 Sep 2009	• Updated Table 25 — PLL Electrical Specifications.
8 April 2010	• Updated Table 37— EzPort Electrical Specifications
22 Mar 2011	• Updated Table Oscillator and PLL Electrical Specification. In EXTAL input high voltage updated VDD to 3.0
23-Mar-2011	• Changed EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, add a note this value has been updated. • Updated clock generation feature

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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