

# SPREAD SPECTRUM CLOCK GENERATOR

# ICS7151A-50

## Description

The ICS7151A-50 is a clock generator for EMI (Electromagnetic Interference) reduction. Spectral peaks are attenuated by modulating the system clock frequency. Down or center spread profiles are selectable. Down spread will not exceed the maximum frequency of an unspread clock, and center spread does not change the average operating frequency of the system

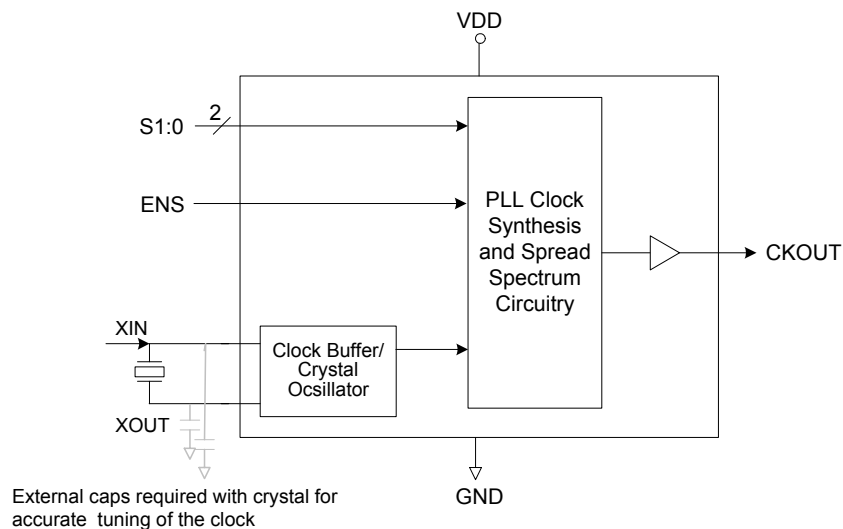
IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

## Features

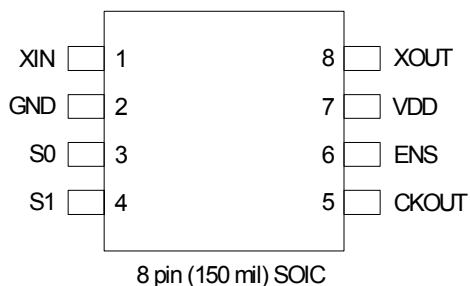
- Operating voltage of 3.3 V  $\pm$ 0.3 V
- Packaged in 8-pin SOIC
- Available in Pb (lead) free package
- Input frequency range of 16.5 to 33.4 MHz
- Output frequency ranges of 8.3 to 16.7 MHz
- Provides a spread spectrum clock output ( $\pm$ 0.5%,  $\pm$ 1.5% center spread; -1.0%, -3.0% down spread)
- Multiplication rate of x1/2
- Advanced, low-power CMOS process
- Pin compatible with the Fujitsu MB88151-500

**NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

## Block Diagram



## Pin Assignment



## Spread Direction and Percentage Select Table

| S1<br>Pin 4     | S0<br>Pin 3 | Spread<br>Direction | Spread<br>Percentage (%) |
|-----------------|-------------|---------------------|--------------------------|
| 0               | 0           | Center              | ±1.5                     |
| 0               | 1           | Center              | ±0.5                     |
| 1               | 0           | Down                | -1.0                     |
| 1               | 1           | Down                | -3.0                     |
| ENS<br>(note 1) |             | Modulation          |                          |
| 0               |             | No Modulation       |                          |
| 1               |             | Modulation          |                          |

Notes:

- Pin 1 has a pull-up resistor.

## Pin Descriptions

| Pin<br>Number | Pin<br>Name | Pin Type | Pin Description                               |
|---------------|-------------|----------|-----------------------------------------------|
| 1             | XIN         | Input    | Crystal pin/clock input pin.                  |
| 2             | GND         | Power    | Connect to ground.                            |
| 3             | S0          | Input    | Select pin 0. Spread modulation select.       |
| 4             | S1          | Input    | Select pin 1. Spread modulation select.       |
| 5             | CKOUT       | Output   | Clock output.                                 |
| 6             | ENS         | Input    | Modulation enable. Internal pull-up resistor. |
| 7             | VDD         | Power    | Connect to +3.3 V.                            |
| 8             | XOUT        | Output   | Crystal connection pin.                       |

## External Components

The ICS7151A-50 requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01 $\mu$ F must be connected between GND and VDD on pins 2 and 7, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

Series termination should be used on the clock output. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance) place a 27 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 25 $\Omega$ .

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01 $\mu$ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 27 $\Omega$  series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS7151A-50. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Crystal Information

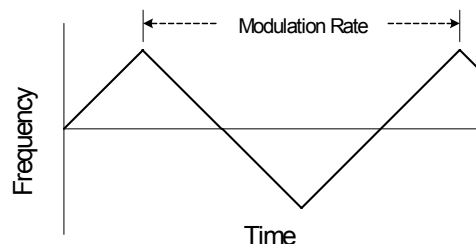
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation,  $C_L$  is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF  $[(16-6) \times 2]$  capacitors should be used.

## Spread Spectrum Profile

The ICS7151A-50 low EMI clock generator uses a triangular frequency modulation profile for optimal down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.

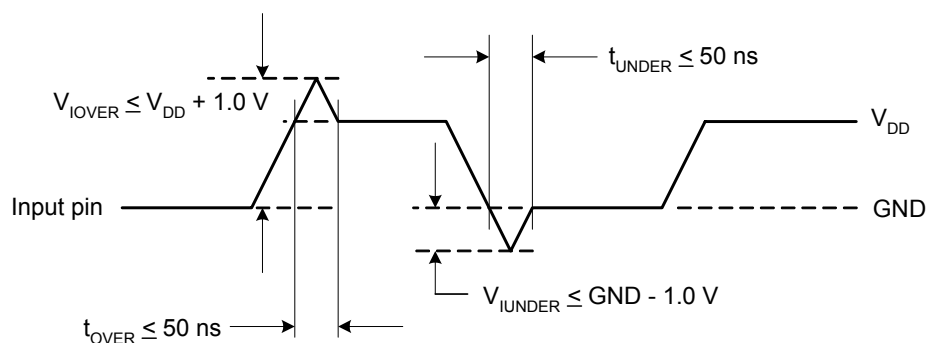


## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS7151A-50. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                       | Rating                                |
|--------------------------------------------|---------------------------------------|
| Supply Voltage, VDD                        | -0.5 to 4.0 V                         |
| All Inputs and Outputs (referenced to GND) | -0.5 V to VDD+0.5 V                   |
| Ambient Operating Temperature              | -40 to +85° C                         |
| Storage Temperature                        | -55 to +125° C                        |
| Junction Temperature                       | -40 to +125° C                        |
| Soldering Temperature                      | 260° C                                |
| Overshoot ( $V_{IOVER}$ )                  | VDD + 1.0 V ( $t_{OVER} \leq 50$ ns)  |
| Undershoot ( $V_{IUNDER}$ )                | GND - 1.0 V ( $t_{UNDER} \leq 50$ ns) |

### Overshoot/Undershoot



## Recommended Operation Conditions

| Parameter                                         | Min. | Typ. | Max. | Units |
|---------------------------------------------------|------|------|------|-------|
| Ambient Operating Temperature                     | -40  |      | +85  | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.0 | 3.3  | 3.6  | V     |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±0.3 V**, Ambient Temperature -40 to +85° C

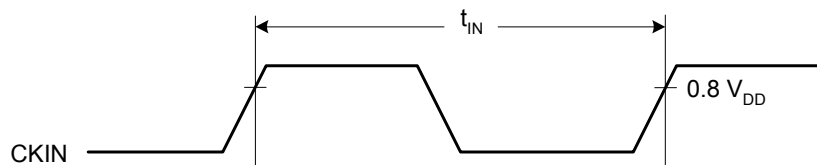
| Parameter              | Symbol          | Conditions                            | Min.      | Typ. | Max.       | Units |
|------------------------|-----------------|---------------------------------------|-----------|------|------------|-------|
| Operating Voltage      | VDD             |                                       | 3.0       | 3.3  | 3.6        | V     |
| Supply Current         | IDD             | No load, at 3.3 V,<br>output = 24 MHz |           | 10   | 14         | mA    |
| Input Frequency        |                 |                                       | 16.5      |      | 33.4       | MHz   |
| Input High Voltage     | V <sub>IH</sub> | XIN, S0, S1, ENS                      | VDD * 0.8 |      | VDD + 0.3  | V     |
| Input Low Voltage      | V <sub>IL</sub> | XIN, S0, S1, ENS                      | 0.0       |      | VDD * 0.20 | V     |
| Output High Voltage    | V <sub>OH</sub> | CKOUT, I <sub>OH</sub> = -4 mA        | 2.0       |      |            | V     |
| Output Low Voltage     | V <sub>OL</sub> | CKOUT, I <sub>OL</sub> = 4 mA         |           |      | 0.4        | V     |
| Input Capacitance      | C <sub>IN</sub> | XIN, S0, S1, ENS                      |           |      | 16         | pF    |
| Load Capacitance       | C <sub>L</sub>  | CKOUT, 8.3 to 66.7 MHz                |           |      | 15         | pF    |
|                        |                 | CKOUT, 66.7 to 100 MHz                |           |      | 10         | pF    |
|                        |                 | CKOUT, 100 to 133.4 MHz               |           |      | 7          | pF    |
| Input Pull-up Resistor | R <sub>PU</sub> | ENS                                   | 100       | 240  | 400        | kΩ    |

## AC Electrical Characteristics

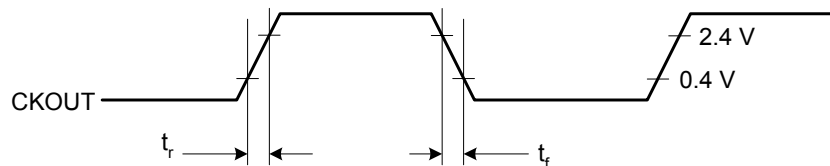
Unless stated otherwise, **VDD = 3.3 V ±0.3 V**, Ambient Temperature -40 to +85° C

| Parameter               | Symbol           | Conditions                                     | Min. | Typ. | Max. | Units |
|-------------------------|------------------|------------------------------------------------|------|------|------|-------|
| Oscillation Frequency   | f <sub>X</sub>   | Fundamental oscillation                        | 16.5 |      | 33.4 | MHz   |
| Input Frequency         | f <sub>IN</sub>  | XIN                                            | 16.5 |      | 33.4 | MHz   |
| Output Frequency        | f <sub>OUT</sub> | CKOUT, 2-frequency division                    | 8.3  |      | 16.7 | MHz   |
| Input Clock Duty Cycle  |                  | XIN, 16.5 to 33.4 MHz                          | 40   | 50   | 60   | %     |
| Output Clock Duty Cycle | t <sub>DCC</sub> | CKOUT, 1.5 V                                   | 40   |      | 60   | %     |
| Output Slew Rate        |                  | CKOUT, 0.4 to 2.4 V,<br>load capacitance 15 pF | 0.5  | TBD  | 3.0  | V/ns  |
| Cycle to Cycle Jitter   | t <sub>JC</sub>  | No load, standard deviation                    |      | TBD  | 200  | ps    |
| Lock Time               | t <sub>LK</sub>  | CKOUT                                          |      | 2    | 5    | ms    |
| Modulation Frequency    | f <sub>MOD</sub> | CKOUT=TBD                                      |      | 33   |      | kHz   |

### Input Frequency ( $f_{IN} = 1/t_{IN}$ )



### Output Slew Rate



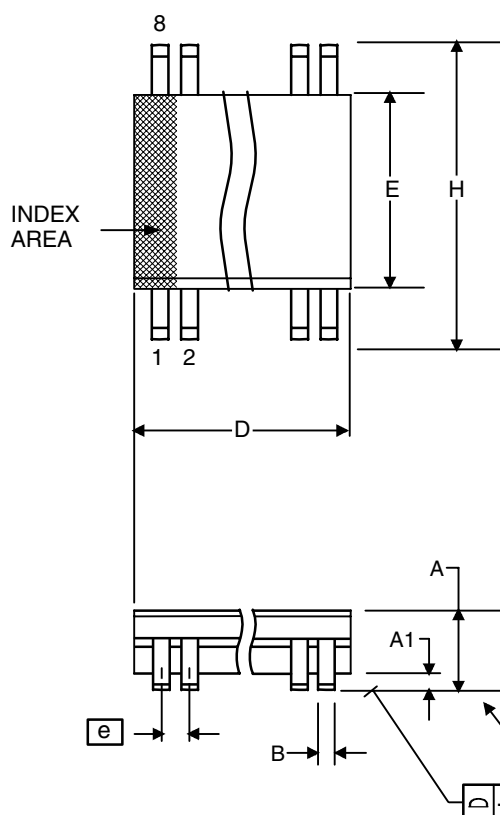
$$SR = (2.4 - 0.4) / t_r, SR = (2.4 - 0.4) / t_f$$

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units         |
|----------------------------------------|---------------|----------------|------|------|------|---------------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 150  |      | $^{\circ}C/W$ |
|                                        | $\theta_{JA}$ | 1 m/s air flow |      | 140  |      | $^{\circ}C/W$ |
|                                        | $\theta_{JA}$ | 3 m/s air flow |      | 120  |      | $^{\circ}C/W$ |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 40   |      | $^{\circ}C/W$ |

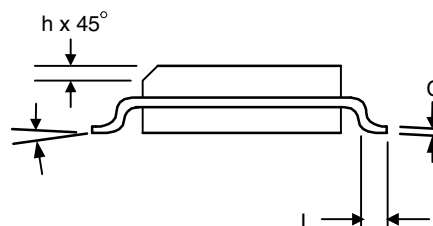
## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol   | Millimeters |      | Inches*     |       |
|----------|-------------|------|-------------|-------|
|          | Min         | Max  | Min         | Max   |
| A        | 1.35        | 1.75 | .0532       | .0688 |
| A1       | 0.10        | 0.25 | .0040       | .0098 |
| B        | 0.33        | 0.51 | .013        | .020  |
| C        | 0.19        | 0.25 | .0075       | .0098 |
| D        | 4.80        | 5.00 | .1890       | .1968 |
| E        | 3.80        | 4.00 | .1497       | .1574 |
| e        | 1.27 BASIC  |      | 0.050 BASIC |       |
| H        | 5.80        | 6.20 | .2284       | .2440 |
| h        | 0.25        | 0.50 | .010        | .020  |
| L        | 0.40        | 1.27 | .016        | .050  |
| $\alpha$ | 0°          | 8°   | 0°          | 8°    |

\*For reference only. Controlling dimensions in mm.



## \*Ordering Information

| Part / Order Number | Marking  | Shipping Packaging | Package    | Temperature   |
|---------------------|----------|--------------------|------------|---------------|
| 7151AM-50*          | 7151AM50 | Tubes              | 8-pin SOIC | 0 to +70° C   |
| 7151AM-50T*         | 7151AM50 | Tape and Reel      | 8-pin SOIC | 0 to +70° C   |
| 7151AM-50LF         | 151AM50L | Tubes              | 8-pin SOIC | 0 to +70° C   |
| 7151AM-50LFT        | 151AM50L | Tape and Reel      | 8-pin SOIC | 0 to +70° C   |
| 7151AMI-50*         | 151AMI50 | Tubes              | 8-pin SOIC | -40 to +85° C |
| 7151AMI-50T*        | 151AMI50 | Tape and Reel      | 8-pin SOIC | -40 to +85° C |
| 7151AMI-50LF        | 51AMI50L | Tubes              | 8-pin SOIC | -40 to +85° C |
| 7151AMI-50LFT       | 51AMI50L | Tape and Reel      | 8-pin SOIC | -40 to +85° C |

**NOTE:** EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

**Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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## Revision History

| Rev. | Originator | Date     | Description of Change               |
|------|------------|----------|-------------------------------------|
| A    | J. Sarma   | 10/20/05 | Rev A; new device/datasheet.        |
| B    |            | 11/04/09 | Added EOL note for non-green parts. |
|      |            |          |                                     |
|      |            |          |                                     |
|      |            |          |                                     |

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