SPOC+ 12V

BTS54040-LBA

SPI Power Controller

Data Sheet

Rev. 1.0, 2013-03-24

Automotive

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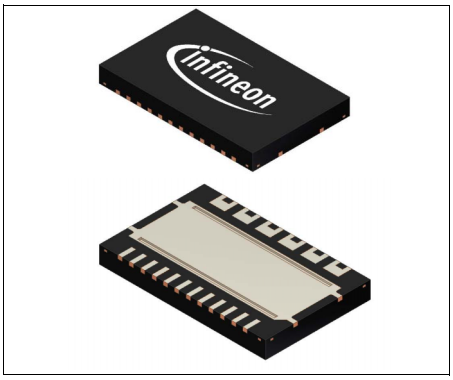
Table of Contents

List of Figures

List of Tables

1 Overview



TSON-24-3

Package	Marking
TSON-24-3	BTS54040-LBA

Features

- 8 bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for four channels
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Very low stand-by current
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Description

The SPOC+ BTS54040-LBA is a four channel high-side smart power switch in TSON-24-3 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive exterior lamps up to 27 W or the equivalent LED light.

Table 1-1 Product Summary

Operating Voltage Power Switch	V_S	5.5 … 28 V
Logic Supply Voltage	V_{DD}	3.8 … 5.5 V
Over Voltage Protection	$V_{S(AZ,min)}$	42 V
Maximum Stand-By Current at 25 °C	$I_{S(OFF)}$	3 µA
Maximum ON State Resistance at T_j = 150 °C Channel 1, 2, 3, 4	$R_{DS(ON,max)}$	78 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	2.5 MHz

Configuration and status diagnosis are done via SPI. An 8 bit serial peripheral interface (SPI) is used. The SPI is daisy chain capable.

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over temperature flag per output is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to V_S diagnosis.

All four channels can be configured to bulb or LED mode for maximum flexibility.

The SPOC+ BTS54040-LBA provides a fail-safe feature via a Limp Home Input (LHI) pin and direct INput pins.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

Applications

- High-side power switch for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for standard exterior lighting like position light, tail light, brake light, parking light, license plate light, indicators and equivalent in the LED technology
- Replaces electromechanical relays, fuses and discrete circuits

Protective Functions

- Reverse battery protection with external components
- Short circuit to ground protection
- Stable behavior at under voltage
- Current limitation
- Absolute and and dynamic temperature sensor
- Thermal shutdown with latch after a limited amount of retries
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio (k_{ILIS}) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode
- Feedback on over temperature via SPI
- Short circuit to V_S detection
- Monitoring of Input pins status

Application Specific Functions

- Fail-safe activation via LHI pin and control via input pins
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs
- LED mode selection available
- SPI with daisy chain capability
- Switch bypass monitoring for detecting short circuit to V_S

2 Block Diagram

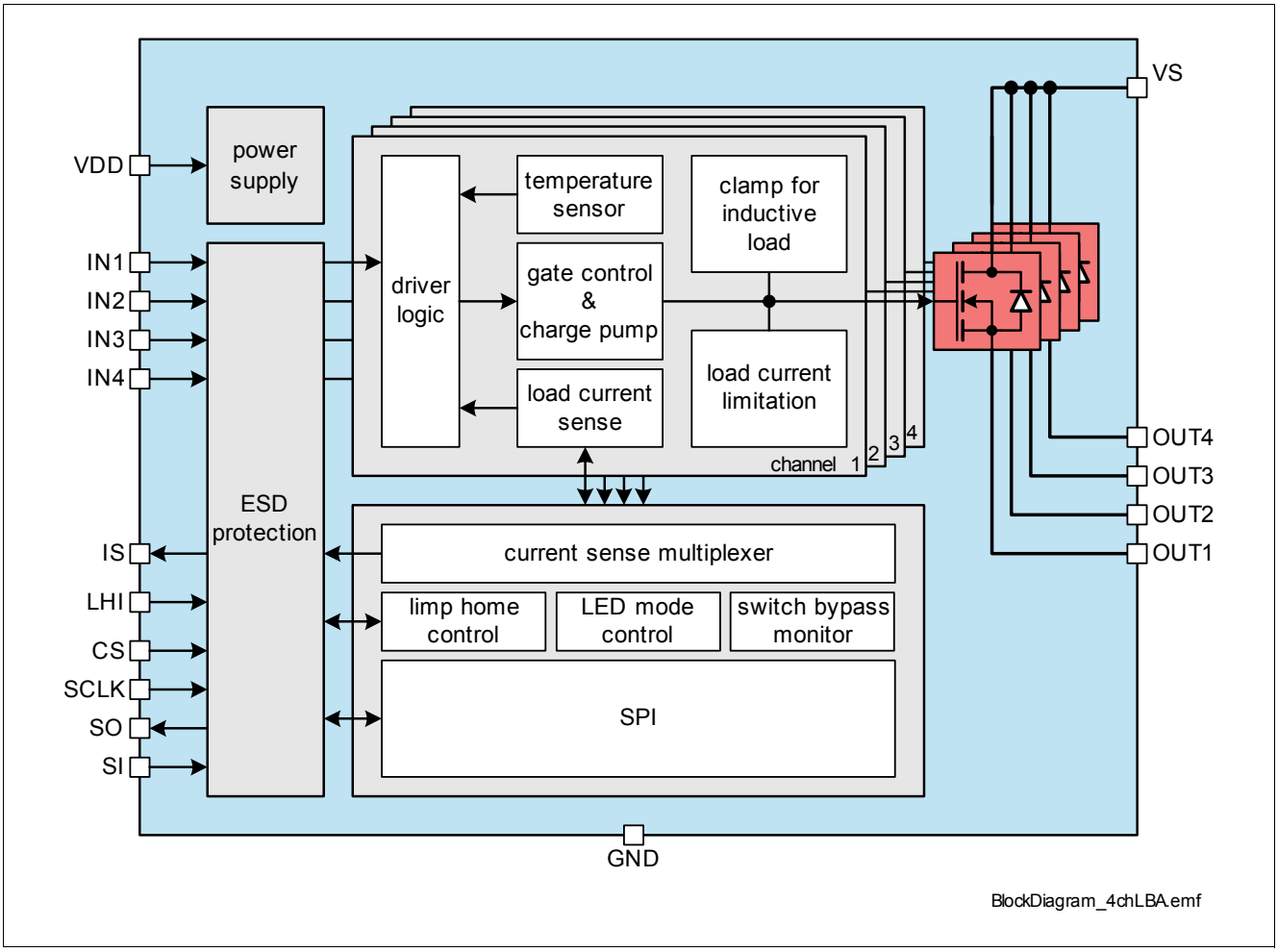


Figure 2-1 Block Diagram SPOC+ BTS54040-LBA

2.1 Terms

Figure 2-2 shows all terms used in this data sheet, with associated convention for positive values.

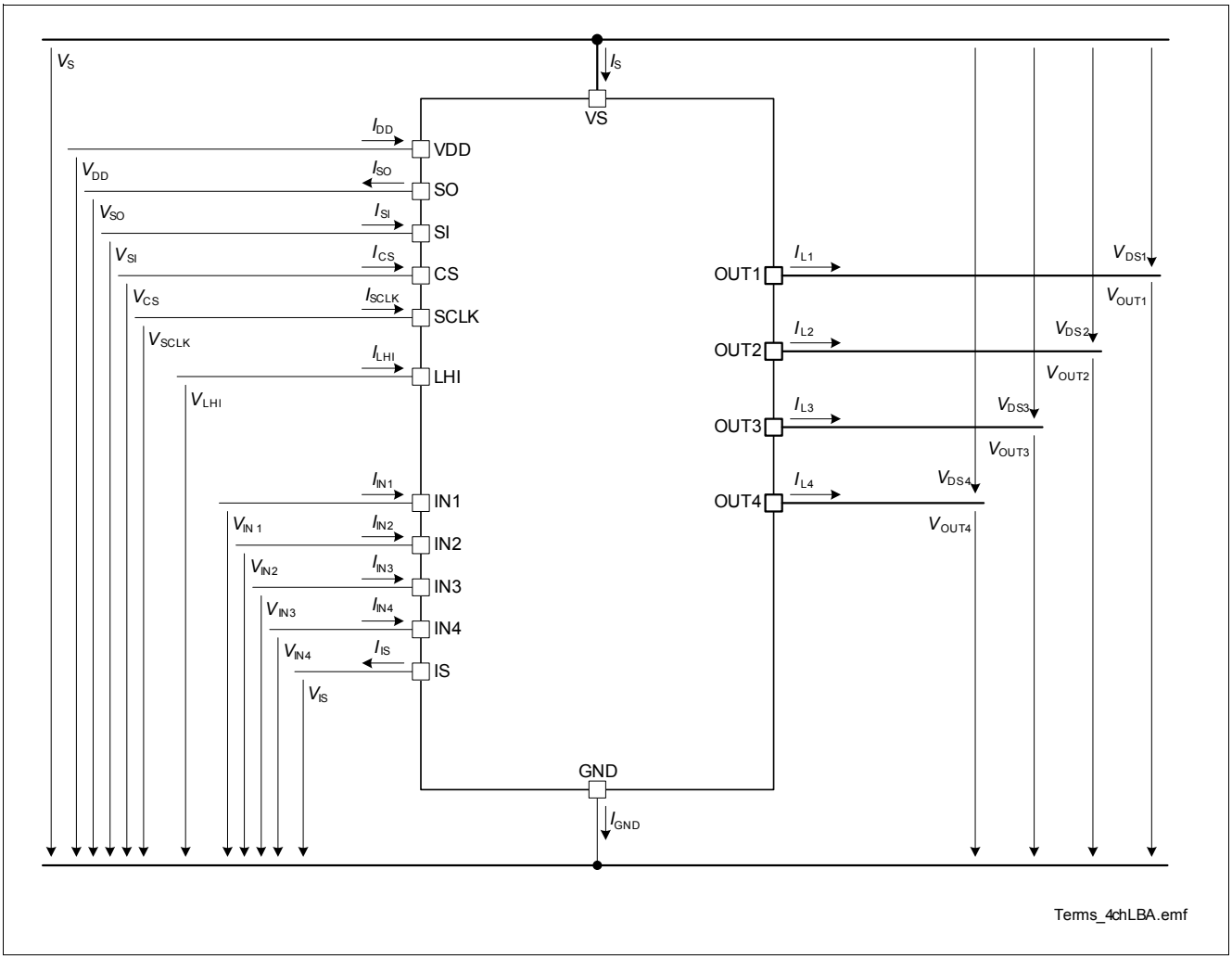


Figure 2-2 Voltage and Current Definition

In all tables of electrical characteristics, symbols related to channels without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS1} ... V_{DS4}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.STB`) with the exception of the bits in the Diagnosis frames which are marked only with `PARAMETER` (e.g. `VSMON`).

3 Pin Configuration

3.1 Pin Assignment SPOC+ BTS54040-LBA

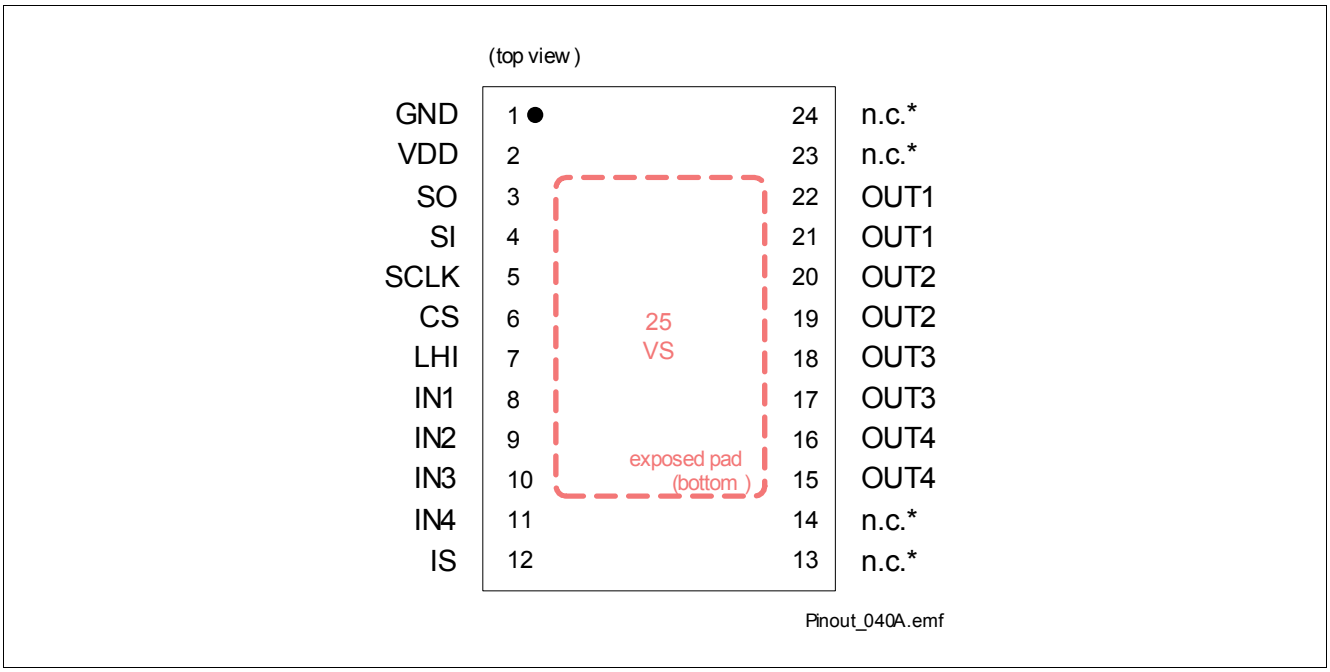


Figure 3-1 Pin Configuration TSON-24-3

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
25	VS	–	Positive power supply for high-side power switch
1	GND	–	Ground connection
2	VDD	–	Logic supply (5 V)
SPI & Diagnosis Pins			
3	SO	O	Serial output of SPI interface
4	SI	I	Serial input of SPI interface (“high” active)
5	SCLK	I	Serial clock of SPI interface (“high” active)
6	CS	I	Chip select of SPI interface (“low” active); Integrated pull up do VDD
12	IS	O	Current sense output signal
Limp Home Input Pin (integrated pull-down, leave unused Limp Home Input pin unconnected)			
7	LHI	I	Limp home activation signal ("high" active)
Parallel Input Pins (integrated pull-down, leave unused pins unconnected)			
8	IN1	I	Input signal of channel 1 ("high" active)
9	IN2	I	Input signal of channel 2 ("high" active)
10	IN3	I	Input signal of channel 3 ("high" active)
11	IN4	I	Input signal of channel 4 ("high" active)
Power Output Pins			
21, 22 [1)]	OUT1	O	Protected high-side power output of channel 1
19, 20 [1)]	OUT2	O	Protected high-side power output of channel 2
17, 18 [1)]	OUT3	O	Protected high-side power output of channel 3
15, 16 [1)]	OUT4	O	Protected high-side power output of channel 4
Not connected Pins			
13, 14	n.c.*	–	Not connected, internally not bonded, shorted together
23, 24	n.c.*	–	Not connected, internally not bonded, shorted together

1) All outputs pins of each channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_j = -40 to +150 °C; all voltages with respect to ground

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 1, 2, 3, 4: R_L = 6.8 Ω (33 Ω when **LGCR.LED**n = 1)

Table 4-1 Absolute Maximum Ratings [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage							
Power supply voltage	V_S	-0.3		28	V	–	P_4.1.1
Logic supply voltage	V_{DD}	-0.3		5.5	V	–	P_4.1.2
Reverse polarity voltage	$-V_{S(rev)}$	–		16	V	[2)] T_{jStart} = 25 °C t ≤ 2 min. See **Chapter 10** for setup	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(SC)}$	0		24	V	[3)] R_{ECU} = 20 mΩ l = 0 or 5 m R_{Cable} = 16 mΩ/m L_{Cable} = 1 µH/m	P_4.1.4
Permanent short circuit Number channel activations All channels	n_{RSC1}	-		100	k	[3)] V_{DD} = 5 V t_{ON} = 300ms	P_4.1.6
Voltage at power transistor	V_{DS}	–		42	V	–	P_4.1.8
Supply voltage for load dump protection	$V_{S(LD)}$	–		42	V	[4)] R_I = 2 Ω t = 400 ms	P_4.1.9
Current through ground pin	I_{GND}	-100		25	mA	t ≤ 2 min.	P_4.1.10
Current through VDD pin	I_{DD}	-25		12	mA	t ≤ 2 min.	P_4.1.11
Power Stages							
Load current	$\|I_L\|$	–		$I_{L(LIM)}$	A	[5)]	P_4.1.12
Maximum energy dissipation single pulse - $I_{L(nom)}$ Channel 1, 2, 3, 4	E_{AS}	–		45	mJ	[6)] $T_{j(0)}$ = 150 °C $I_{L(0)}$ = $I_{L(nom)}$ = P_6.6.17	P_4.1.15
Diagnosis Pin							
Voltage at sense pin IS	V_{IS}	-0.3		V_S	V	–	P_4.1.24
Current through sense pin IS	I_{IS}	-10		40	mA	t ≤ 2 min.	P_4.1.25
Input Pins							

Table 4-1 Absolute Maximum Ratings (cont'd)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage at input pins	V_{IN}	-0.3		6.0	V	–	P_4.1.26
Current through input pins	I_{IN}	-0.75		0.75	mA	–	P_4.1.27
Current through input pins	I_{IN}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.28
SPI Pins							
Voltage at chip select pin	V_{CS}	-0.3		6.0	V	–	P_4.1.29
Current through chip select pin	I_{CS}	-0.75		0.75	mA	–	P_4.1.30
Current through chip select pin	I_{CS}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.31
Voltage at serial input pin	V_{SI}	-0.3		6.0	V	–	P_4.1.32
Current through serial input pin	I_{SI}	-0.75		0.75	mA	–	P_4.1.33
Current through serial input pin	I_{SI}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.34
Voltage at serial clock pin	V_{SCLK}	-0.3		6.0	V	–	P_4.1.35
Current through serial clock pin	I_{SCLK}	-0.75		0.75	mA	–	P_4.1.36
Current through serial clock pin	I_{SCLK}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.37
Current through serial output pin SO	I_{SO}	-0.75		0.75	mA	–	P_4.1.38
Current through serial output pin SO	I_{SO}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.39
Limp Home Input Pin							
Voltage at Limp Home Input pin	V_{LHI}	-0.3		6.0	V	–	P_4.1.40
Current through Limp Home Input pin	I_{LHI}	-0.75		0.75	mA	–	P_4.1.41
Current through Limp Home Input pin	I_{LHI}	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.42
Temperatures							
Junction temperature	T_j	-40		150	°C	–	P_4.1.45
Dynamic temperature increase while switching	ΔT_j	–		60	K	–	P_4.1.46
Storage temperature	T_{stg}	-55		150	°C	–	P_4.1.47
ESD Susceptibility							
ESD susceptibility HBM OUT pins vs. VS	V_{ESD}	-4		4	kV	7) HBM	P_4.1.48
ESD susceptibility HBM all pins vs. VDD	V_{ESD}	-1.5		1.5	kV	7) HBM	P_4.1.54
ESD susceptibility HBM other pins vs. GND incl. OUT pins vs. GND	V_{ESD}	-2		2	kV	7) HBM	P_4.1.49
ESD Resistivity to GND	V_{ESD}	-500		500	V	8) CDM	P_4.1.51
ESD Resistivity Pin 1, 12, 13, 24 (corner pins) to GND	$V_{ESD1, 12, 13, 24}$	-750		750	V	8) CDM	P_4.1.52

1) Not subject to production test, specified by design.

2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability at the end of this document.
4) R_I is the internal resistance of the load dump pulse generator.
5) Current limitation is a protection feature. Protection features are not designed for continuous repetitive operation.
6) Pulse shape represents inductive switch off: $I_{D(t)} = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$
7) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001-2010
8) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4-2 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	2	–	K/W	1) $T_{j(0)}$ = 105 °C measured to pin 25	P_4.2.1
Junction to Ambient	R_{thJA}	–	21	–	K/W	1)2) $T_{j(0)}$ = 105 °C	P_4.2.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

5 Power Supply

The SPOC+ BTS54040-LBA is supplied by two voltage sources: V_S and V_{DD}. The V_S supply line is used by the power switches. The V_{DD} supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins V_{DD} and GND is recommended as shown in **Chapter 10**.

There is a power-on reset function implemented for the V_{DD} logic power supply which affect SPI registers status (see P_5.3.17), and a undervoltage shutdown for V_S influencing the status of the outputs (see P_5.3.2 and **Chapter 7.4** for further details). After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as V_{DD} is provided in the specified range independent of V_S. The first SPI transmission after a reset contains at pin SO the Standard Diagnosis information, with the transmission error bit **TER** set.

5.1 Power Supply Modes

The following table shows all possible power supply modes for V_S, V_{DD} and the pin LHI.

Power Supply Modes	Off	Off	SPI on	Reset	Off	Limp Home Mode without SPI	Normal operation	Limp Home Mode with SPI[1)]
V_S	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V
V_{DD}	0 V	0 V	5 V	5 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	5 V	0 V	5 V
Power stage, protection	–	–	–	–	–	✓[2)]	✓	✓[3)]
Limp Home	–	–	–	–	–	✓	–	✓
SPI (logic)	–	–	✓	Reset	Reset	Reset	✓	Reset
Stand-by current	–	–	–	–	✓	–	✓[4)]	–
Idle current	–	–	–	–	–	–	✓[5)]	–
Diagnosis	–	–	–	–	–	–	✓	✓[6)]

1) SPI read only.
2) Protection with unlimited reactivation and without latch off.
3) Protection with limited reactivation and latch off.
4) When **DCR.MUX** = 111_B
5) When all channels are in OFF-state and **DCR.MUX** ≠ 111_B.
6) Current sense disabled in Limp Home Mode.

5.1.1 Stand-by Mode

Stand-by mode is entered as soon as the current sense multiplexer (**DCR.MUX**) is in default (stand-by) position[1)]. As soon as stand-by mode is entered, register **STB** is set. All channels are deactivated in stand-by mode. Refer to the **Chapter 5.2.3** for further information.

5.1.2 Idle Mode

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and V_{DD} supply is available.

1) Not affected by the inputs state

5.1.3 Device Wake-up

To wake-up the device, the current sense multiplexer (**DCR.MUX**) is programmed to a value different from default position (stand-by).

Limp Home Input (LHI = “high”) will wake-up the device and is working without V_{DD} supply. As a result, channels can be activated via the dedicated input pins.

5.2 Reset

There are several reset triggers implemented in the device. They reset the SPI registers and errors flags to their default values.

The first SPI transmission after any kind of reset contains at pin SO the Standard Diagnosis information, the transmission error bit **TER** is set.

5.2.1 Power-On Reset

The power-on reset is released, when V_{DD} voltage level is higher than $V_{DD(min)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

5.2.2 Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as **HWCR.RST** bit is set to 1, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$ plus reset command delay time $t_{d(RST)}$.

5.2.3 Limp Home Mode

The Limp Home Mode will be activated as soon as the pin LHI is set to “high” for a time longer than $t_{LHI(ac)}$.

In Limp Home Mode, the SPI write-registers are reset. To prevent unexpected SPI reset by a non consistent signal at LHI pin, V_S monitoring is implemented.

The monitoring allows in Limp Home Mode, to reset the SPI write-registers, if LHI is set to “high” for longer than $t_{LHI(ac)}$ and $V_S > V_{SMON}$ (P_5.3.12). Otherwise any glitch on LHI is filtered and has no effect on the SPI.

After an SPI reset, Output OUTn will follow the input INn configuration only for the channels where an direct INput pin is present. All other channels will be switched OFF. For application example refer to **Chapter 10**. The SPI interface is operating normally, so the Limp Home register bit LHI as well as the error flags can be read, but any write command will be ignored.

For the protection functions in Limp Home Mode, refer to **Chapter 7.1.1**.

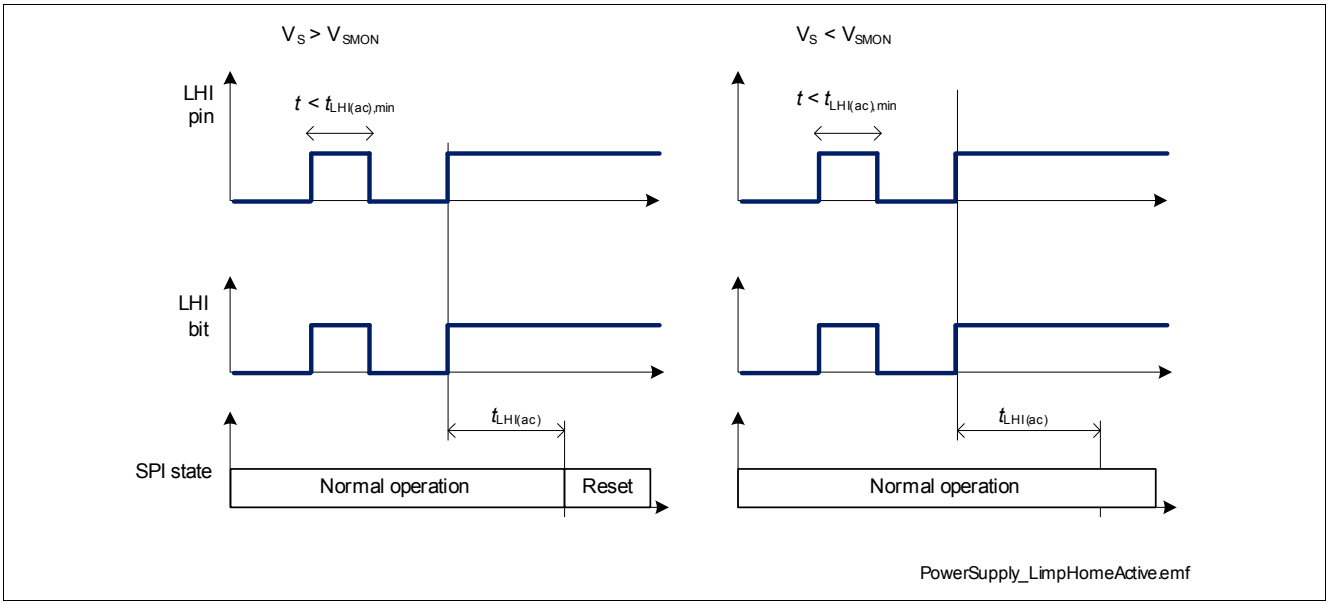


Figure 5-1 Limp Home Activation as function of V_S

5.3 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
Typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 1, 2, 3, 4: R_L = 6.8 Ω (33 Ω when **LGCR.LED**n = 1)

Table 5-1 Electrical Characteristics Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Operating voltage power switch	$V_{S(OP)}$	5.5	–	28[1)]	V	V_{DS} < 0.5 V	P_5.3.1
Undervoltage shutdown	$V_{S(UV)}$	–	–	4.5	V	OUTn = ON From V_{DS} < 1 V to I_{Ln} = 0 A (see **Figure 7-4**)	P_5.3.2
Undervoltage shutdown Hysteresis	$V_{S(HYS)}$	–	350	–	mV	[1)]	P_5.3.3
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	0.1	3	µA	[1)] V_{DD} = 0 V V_{LHI} = 0 V T_j = 25 °C	P_5.3.7
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	0.1	3	µA	[1)] V_{DD} = 0 V V_{LHI} = 0 V T_j ≤ 85 °C	P_5.3.8
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	4	58	µA	V_{DD} = 0 V V_{LHI} = 0 V T_j = 150 °C	P_5.3.26
Idle current for whole device with loads, all channels off.	$I_{VS(idle)}$	–	2.5	8	mA	V_{DD} = 5 V **DCR.MUX** = 110_B	P_5.3.10
Operating current for whole device	I_{GND}	–	7	25	mA	f_{SCLK} = 0 MHz	P_5.3.27
V_S threshold for Limp Home validation	V_{SMON}	0.6	1.2	1.8	V	**VSMON** = 1	P_5.3.12
VDD pin							
Logic supply voltage	V_{DD}	3.8	–	5.5[1)]	V	f_{SCLK} = 2 MHz	P_5.3.13
Logic supply current Normal operation	I_{DD}	–	125	270	µA	f_{SCLK} = 0 MHz V_{CS} = V_{DD}= 5 V **DCR.MUX** ≠ 111_B	P_5.3.14
Logic Stand-by current	$I_{DD(STB)}$	–	40	90	µA	f_{SCLK} = 0 MHz V_{CS} = V_{DD}= 5 V **DCR.MUX** = 111_B	P_5.3.16

Table 5-1 Electrical Characteristics Power Supply (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-On reset threshold voltage	$V_{DD(PO)}$	2.0	2.8	3.8	V	SI = 0 V SCLK = 0 V CS = 0 V SO from 0 to Z	P_5.3.17
LHI Input Characteristics							
L-input level at pin LHI	$V_{LHI(L)}$	-0.3	–	1.0	V	**LHI** = 1 (see **Chapter 9.6.1**)	P_5.3.18
H-input level at pin LHI	$V_{LHI(H)}$	2.6	–	6.0	V	–	P_5.3.19
L-input current through pin LHI	$I_{LHI(L)}$	3	27	75	µA	V_{LHI} = 1.0 V	P_5.3.20
H-input current through pin LHI	$I_{LHI(H)}$	7	30	75	µA	V_{LHI} = 2.6 V	P_5.3.21
Timings							
Power-On wake up time	$t_{WU(PO)}$	–	200	–	µs	1)	P_5.3.22
Limp Home acknowledgement time	$t_{LHI(ac)}$	5	–	200	µs	V_{DD} = 5 V polling of Standard Diagnosis (see **Chapter 9.6.1**) until **LHI** = **STB** = 1	P_5.3.23
Reset command delay time	$t_{d(RST)}$	–	–	100	µs	1)	P_5.3.25

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing at V_S = 13.5 V, V_{DD} = 4.3 V and T_j = 25 °C

6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs with charge pumps. There are four channels implemented in the device. Each channel can be switched on via SPI register `OUT` or via an input pin, when available. All channels provide a load type configuration for bulbs or LEDs in register `LGCR` (see **Chapter 9.7.3**). The load type configuration can be changed in ON- as well as in OFF-state.

6.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage V_S as well as on the junction temperature T_j. **Figure 6-1** and **Figure 6-2** show those dependencies. The behavior in reverse polarity mode is described in **Chapter 7**.

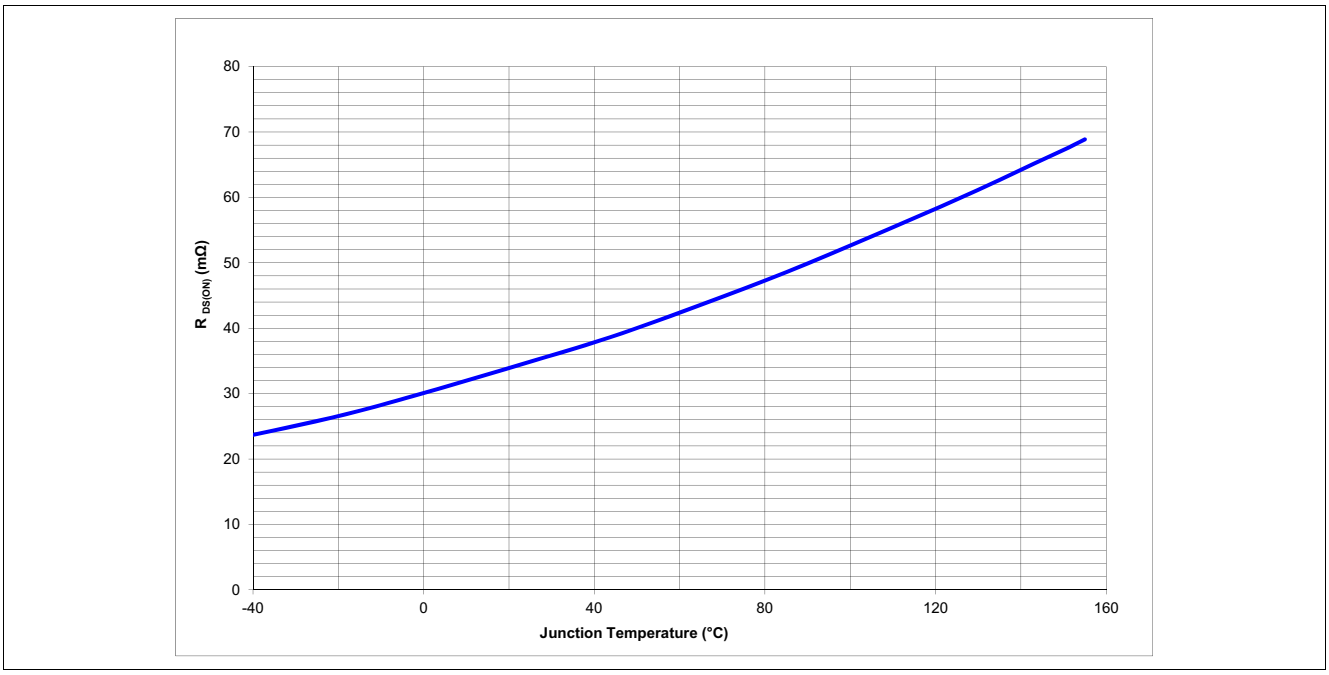


Figure 6-1 Typical On-State Resistance as function of T_j (all channels)

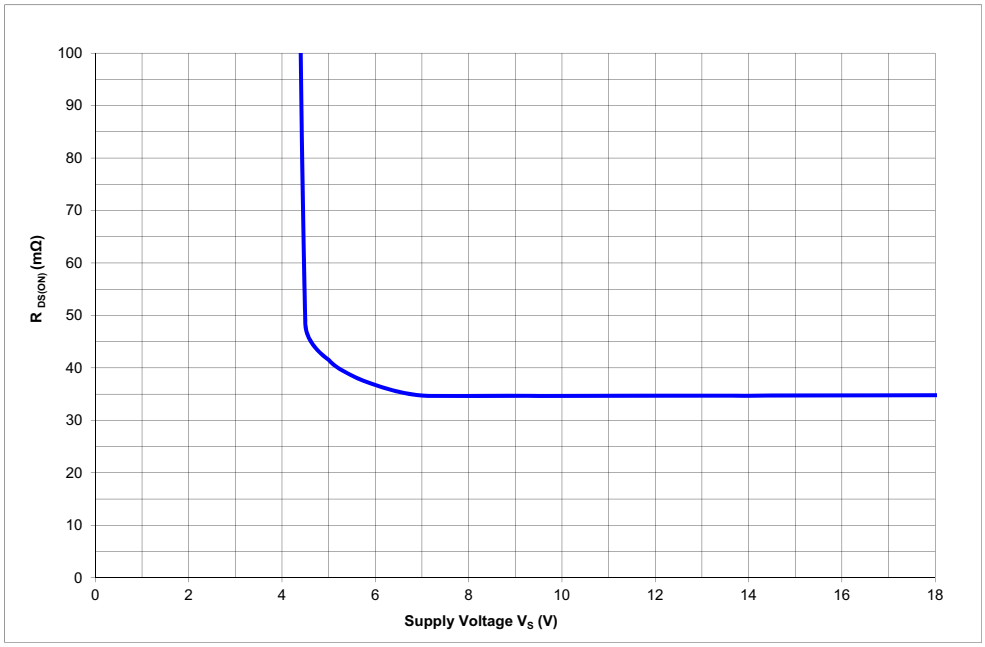


Figure 6-2 Typical On-State Resistance as function of V_S (all channels)

6.2 Input Circuit

There are two ways of using the input pins in combination with the OUT register by programming bit **HWCR.COL** in register HWCR (see **Chapter 9.7.5**).

- **HWCR.COL** = 0: A channel is switched ON either by the according OUT register bit or by the input pin.
- **HWCR.COL** = 1: A channel is switched ON by the according OUT register bit only, when the input pin is "high". In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register OUT (see **Chapter 9.7.1**).

The default state (**HWCR.COL** = 0) is the OR-combination of the input signal and the SPI-bit. In Limp Home Mode (LHI pin set to “high”) the combinatorial logic is switched to OR-mode to enable a channel activation via the input pins only.

Figure 6-3 shows the complete input switch matrix.

The zener diode protects the input circuit against ESD pulses. The current sink to ground ensures that the input signal is low in case of an open input pin.

6.3 Input Status Monitor

The level of the input stage can be monitored via the input status monitor. The input status is indicated in the OUT register for the available input pin. After setting the bit **SWCR.SWR**, the readout the output register OUT shows the state of the input pins.

The input status monitor is operational only when SPOC+ BTS54040-LBA *is not in stand-by operation. During stand-by operation this function is not supported.*

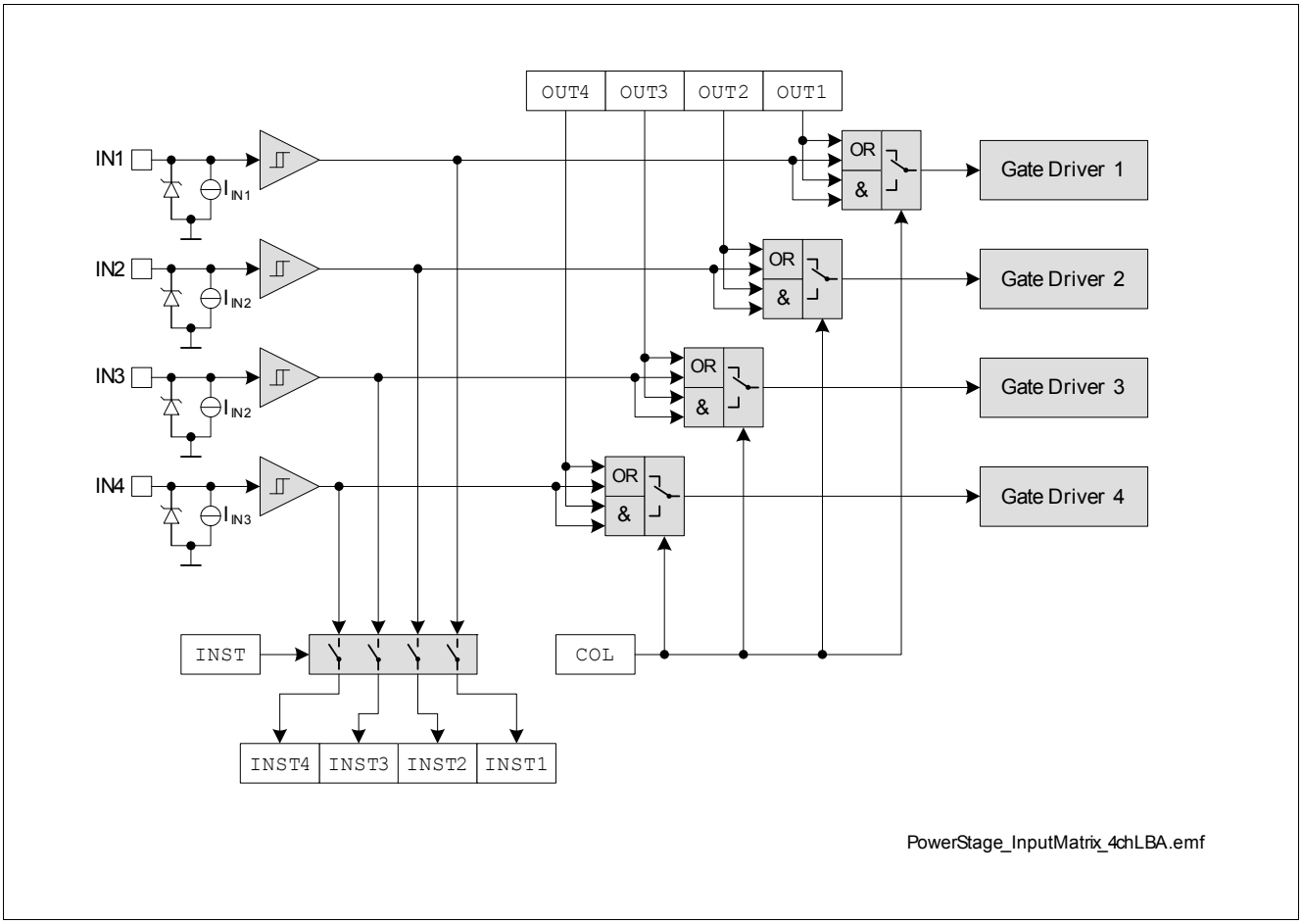


Figure 6-3 Input Switch Matrix

6.4 Power Stage Output

The power stages are built to be used in high side configuration (Figure 6-4).

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission. Defined slew rates allow lowest EMC emissions during PWM operation at low switching losses.

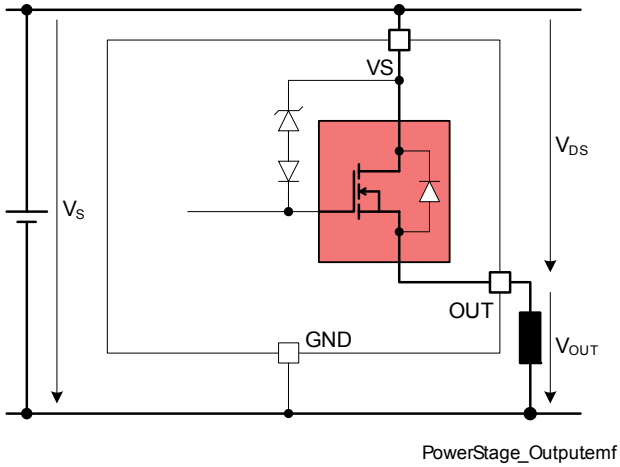


Figure 6-4 Power Stage Output

6.4.1 Bulb and LED Mode

All four channels can be configured in bulb and LED mode via the SPI initialization registers LGCR when **SWCR.SWR** = 0. The default state is **LGCR.LED**n = 0. During LED mode the following parameters are changed for an optimized functionality with LED loads: ON-state resistance $R_{DS(ON)}$, switching timings ($t_{delay(ON)}$, $t_{delay(OFF)}$, t_{ON}, t_{OFF}), slew rates dV/dt_{ON} and dV/dt_{OFF}, load current protections $I_{L(LIM)}$ and current sense ratio k_{ILIS}.

6.4.2 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

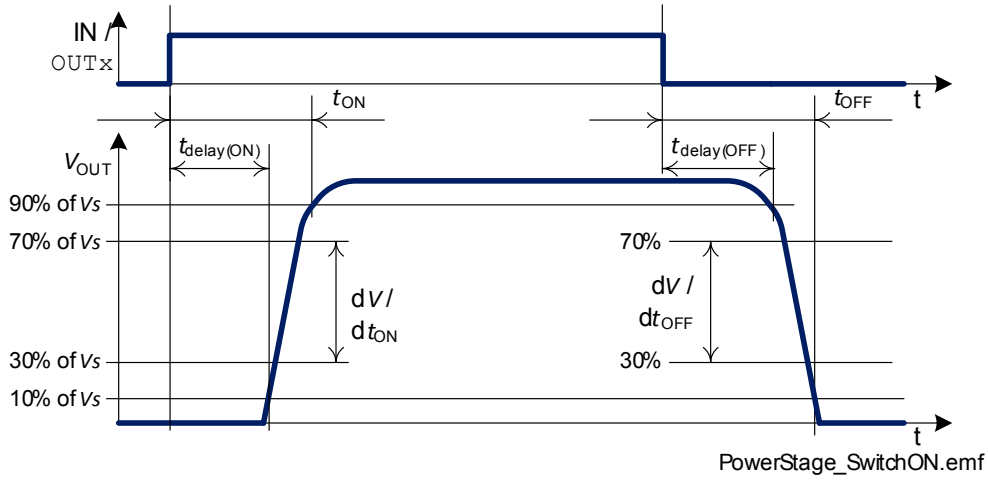


Figure 6-5 Switching a Load (resistive)

6.4.3 Switching Inductive Loads

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, there is a voltage clamp mechanism implemented which limits that negative output voltage to a certain level ($V_{DS(CL)}$ (**Chapter 6.5**)). See **Figure 6-4** for details.Please refer also to **Chapter 7.3**. The maximum allowed load inductance is limited.

6.4.4 Switching Channels in Parallel

In case of appearance of a short circuit with channels in parallel driving a single load, SPOC+ BTS54040-LBA output stages are not synchronized in the restart event. When all channels connected to the same load are in temperature limitation, the channel which has cooled down the fastest doesn´t wait for the other ones to be cooled down as well to restart. Thus, it is not recommended to use the device with channels in parallel.

6.5 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
Typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 1, 2, 3, 4: R_L = 6.8 Ω (33 Ω when **LGCR.LED**n = 1)

Table 6-1 Electrical Characteristics Power Stages

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Characteristics							
On-State resistance Channel 1, 2, 3, 4	$R_{DS(ON)}$	–	39	–	mΩ	[1] V_S = 9 V to 18 V I_L = 2.6 A T_j = 25 °C **LGCR.LED**n = 0	P_6.6.9
On-State resistance Channel 1, 2, 3, 4	$R_{DS(ON)}$	–	–	78	mΩ	V_S = 9 V to 18 V I_L = 2.6 A T_j = 150 °C **LGCR.LED**n = 0	P_6.6.10
On-State resistance Channel 1, 2, 3, 4	$R_{DS(ON)}$	–	137	–	mΩ	[1] V_S = 9 V to 18 V I_L = 0.6 A T_j = 25 °C **LGCR.LED**n = 1	P_6.6.11
On-State resistance Channel 1, 2, 3, 4	$R_{DS(ON)}$	–	–	275	mΩ	V_S = 9 V to 18 V I_L = 0.6 A T_j = 150 °C **LGCR.LED**n = 1	P_6.6.12
Nominal load current Channel 1, 2, 3, 4 (all channels active)	$I_{L(nom)}$	–	2	–	A	[1] T_A = 85 °C T_j < 150 °C	P_6.6.17
Output clamp	$V_{DS(CL)}$	42	47	54	V	I_L = 20 mA	P_6.6.19
Output leakage current per channel T_j ≤ 85°C Channel 1, 2, 3, 4	$I_{L(OFF)}$	–	0.02	0.5	µA	[2] V_{IN} = 0 V or floating **OUT.OUT**n = 0 T_j ≤ 85°C Stand-by or idle mode	P_6.6.22
Output leakage current per channel T_j = 150°C Channel 1, 2, 3, 4	$I_{L(OFF)}$	–	1.5	10	µA	V_{IN} = 0 V or floating **OUT.OUT**n = 0 T_j = 150°C Stand-by or idle mode	P_6.6.26
Input Characteristics							
L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–	P_6.6.28
H-input level	$V_{IN(H)}$	2.6	–	6.0	V	–	P_6.6.29

Table 6-1 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
L-input current	$I_{IN(L)}$	3	27	75	µA	V_{IN} = 1.0 V	P_6.6.30
H-input current	$I_{IN(H)}$	7	30	75	µA	V_{IN} = 2.6 V	P_6.6.31
Timings							
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) Channel 1, 2, 3, 4	$t_{delay(ON)}$	10	30	70	µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.36
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) Channel 1, 2, 3, 4	$t_{delay(ON)}$	3	10	25	µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.37
Turn-OFF delay to 90% V_S (Logical propagation delay from input INn to output OUTn) Channel 1, 2, 3, 4	$t_{delay(OFF)}$	10	30	70	µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.43
Turn-OFF delay to 90% V_S (Logical propagation delay from input INn to output OUTn) Channel 1, 2, 3, 4	$t_{delay(OFF)}$	3	10	25	µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.44
Turn-ON time to 90% V_S Channel 1, 2, 3, 4	t_{ON}	30	75	180	µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.50
Turn-ON time to 90% V_S Channel 1, 2, 3, 4	t_{ON}	10	25	55	µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.51
Turn-OFF time to 10% V_S Channel 1, 2, 3, 4	t_{OFF}	30	75	180	µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.57
Turn-OFF time to 10% V_S Channel 1, 2, 3, 4	t_{OFF}	10	25	55	µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.58

Table 6-1 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn-ON/OFF matching Channel 1, 2, 3, 4	t_{ON} - t_{OFF}	-30	0	50	µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.68
Turn-ON/OFF matching Channel 1, 2, 3, 4	t_{ON} - t_{OFF}	-20	0	20	µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.69
Turn-ON slew rate 30% to 70% V_S Channel 1, 2, 3, 4	dV/ dt_{ON}	0.1	0.25	0.5	V/µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.75
Turn-ON slew rate 30% to 70% V_S Channel 1, 2, 3, 4	dV/ dt_{ON}	0.35	0.88	1.75	V/µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.76
Turn-OFF slew rate 70% to 30% V_S Channel 1, 2, 3, 4	-dV/dt_{OFF}	0.1	0.25	0.5	V/µs	V_S = 13.5 V **LGCR.LED**n = 0	P_6.6.82
Turn-OFF slew rate 70% to 30% V_S Channel 1, 2, 3, 4	-dV/dt_{OFF}	0.35	0.88	1.75	V/µs	V_S = 13.5 V **LGCR.LED**n = 1	P_6.6.83
Output Voltage Drop							
Output voltage drop limitation at small load currents Channel 1, 2, 3, 4	$V_{DS(NL)}$	-	10	25	mV	I_L = 50 mA **LGCR.GBR**n = 1	P_6.6.94

1) Not subject to production test, specified by design.

2) Tested at T_j = -40 °C

7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1 Over Load Protection

The load current I_L is limited by the device itself in case of over load or short circuit to ground. There are multiple steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that $V_{OUT} = V_S - V_{DS}$. Please refer to following figures for details.

Current limitation to the value $I_{L(LIM)}$ is realized by increasing the resistance of the output channel, which leads to fast DMOS temperature rise.

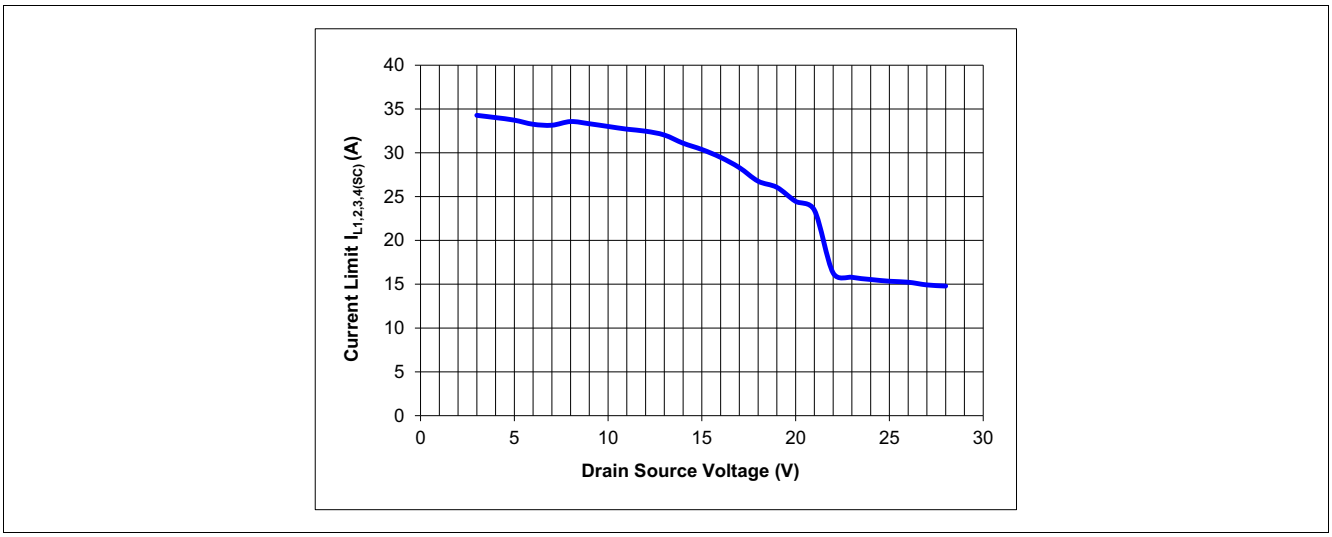


Figure 7-1 Current Limitation Channels 1, 2, 3, 4 (typical values)

7.1.1 Over Temperature Protection

Each channel incorporates both an absolute $T_{j(SC)}$ and a dynamic $\Delta T_{j(SW)}$ temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value.

Each time a channel is switched OFF the error counter of that channel will be incremented by one. The number of automatic reactivations is limited by n_{retry}. If this number of retries is reached the channel turns OFF and latches OFF.

The error information related to the given channel will be available on the Standard Diagnosis and Errors Diagnosis. After switching OFF and latching OFF, the only way to switch ON again, is to clear all thermal counters and errors on all channels by setting **HWCR.CTC** bit to 1. If the channel is active (either **OUT.OUT**n = 1 or INn = 1) it will be turned on immediately after the SPI command.

For the condition $n < n_{retry}$ the counter of automatic reactivations will be reset by every channel activation if **HWCR.RCR** bit is set to 1.

In Limp Home Mode, the thermal counters of the protection functions are still operative only if V_{DD} is provided in the specified range. Otherwise the counters are not active and all channels are in „unlimited restart“ mode.

It is not possible to reset the counters using **HWCR.CTC** bit as long as the SPI is in Limp Home Mode, even if the V_{DD} is provided.

Refer to **Figure 7-2** and **Figure 7-3** for details.

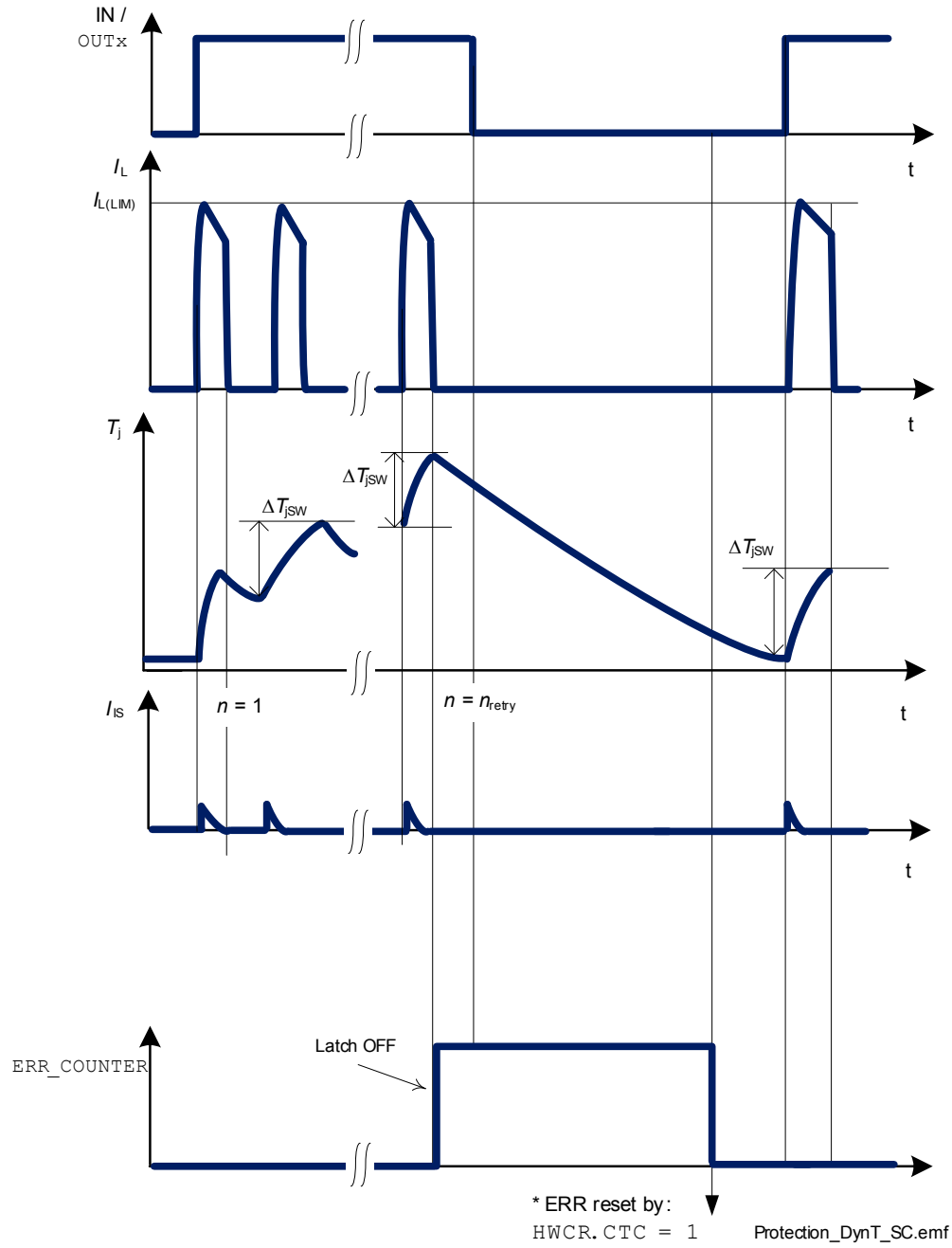


Figure 7-2 Dynamic Temperature Sensor Operations - Short Circuit

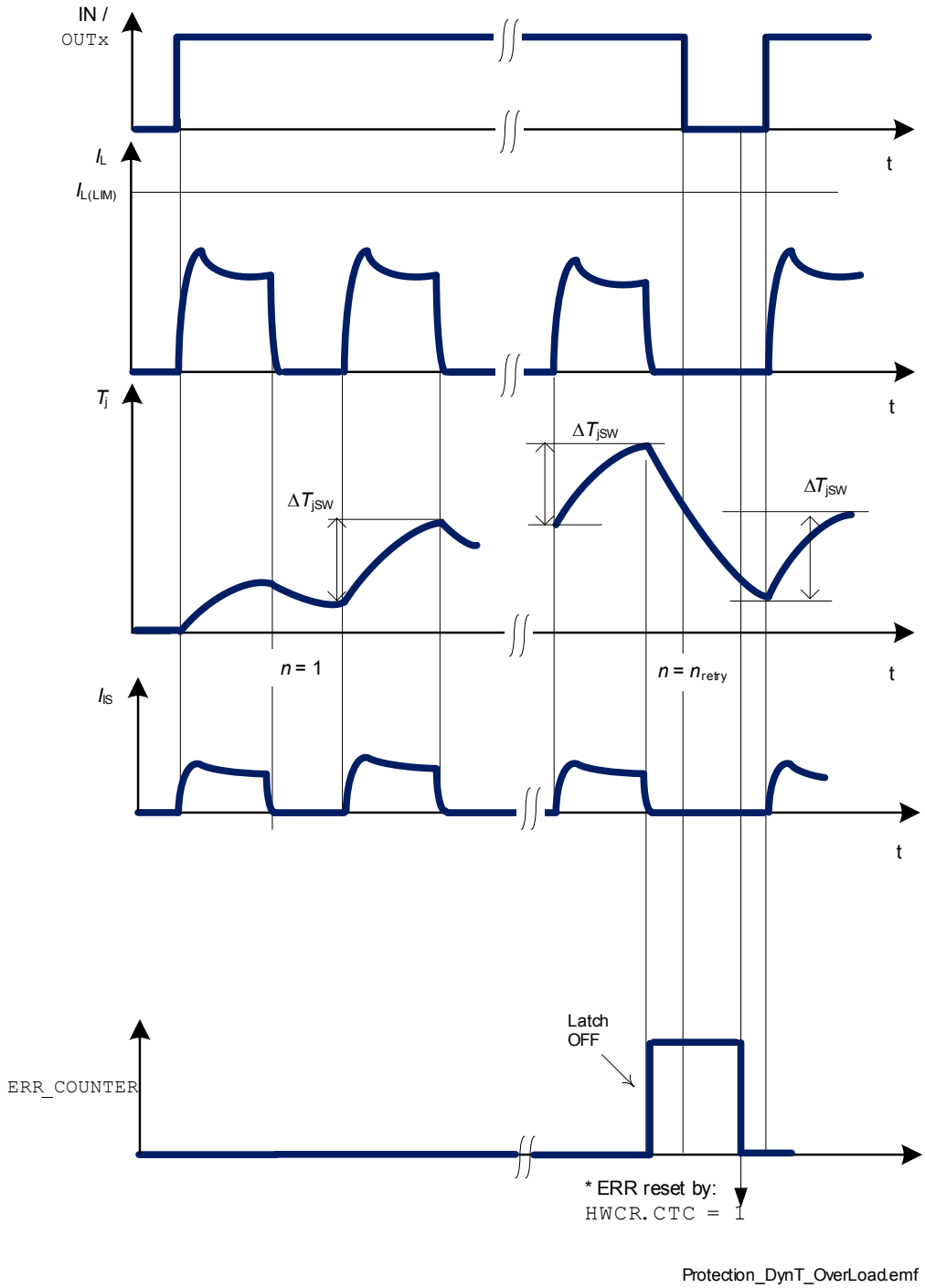


Figure 7-3 Dynamic Temperature Sensor Operations - Overload Condition

7.2 Reverse Polarity Protection

In reverse polarity condition, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads.The current through ground pin GND, sense pin IS, logic power supply pin V_{DD}, SPI pins, input pins and Limp Home Input pin has to be limited as well (please refer to the maximum ratings listed on **Chapter 4.1**).

Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.

7.3 Over Voltage Protection

In the case of supply voltages between $V_{S(SC)max}$ and $V_{S(AZ)}$ the output transistors are still operational and follow the input or the OUT register. Parameters are not warranted and lifetime is reduced compared to nominal voltage supply.

In addition to the output clamp for inductive loads as described in **Chapter 6.4.3**, there is a clamp mechanism available for over voltage protection for the logic and all channels.

7.4 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can takes place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the nominal range. **Figure 7-4** sketches the undervoltage mechanism.

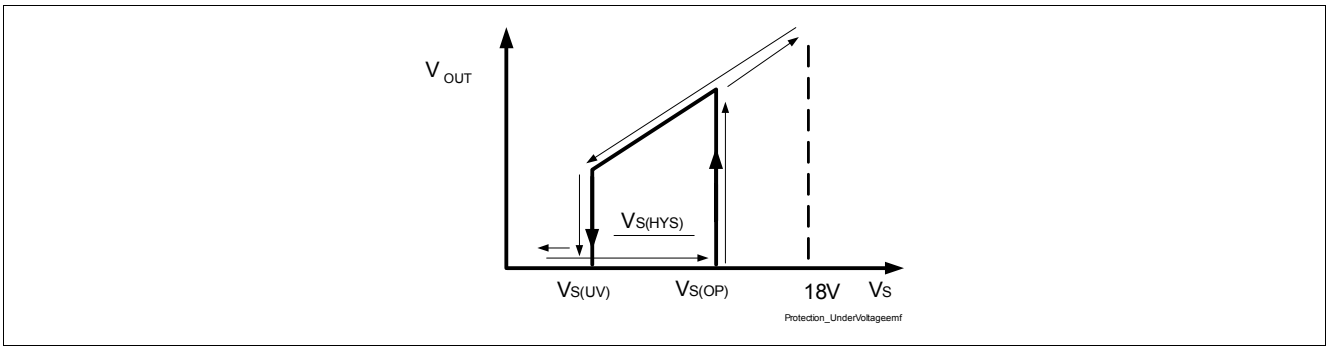


Figure 7-4 Undervoltage Behavior

7.5 Loss of Ground

In case of complete loss of the device ground connection, but loads connected to ground, the SPOC+ BTS54040-LBA securely changes to or stays in OFF-state. Please refer to **Chapter 10** where an application setup is described.

7.6 Loss of V_S

In case of loss of V_S connection in ON-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from V_S to ground. For example, a suppressor diode is recommended between V_S and GND.

7.7 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 1, 2, 3, 4: R_L = 6.8 Ω (33 Ω when **LGCR.LED**n = 1)

Table 7-1 Electrical Characteristics Protection Functions

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over Load Protection							
Load current limitation Channel 1, 2, 3, 4	$I_{L(LIM)}$	25	32	44	A	1) V_{DS} = 5 V **LGCR.LED**n = 0	P_7.7.9
Load current limitation Channel 1, 2, 3, 4	$I_{L(LIM)}$	–	16	–	A	1) V_{DS} = 26 V **LGCR.LED**n = 0	P_7.7.10
Load current limitation Channel 1, 2, 3, 4	$I_{L(LIM)}$	6.5	9	16	A	V_{DS} = 5 V T_j = -40 °C **LGCR.LED**n = 1	P_7.7.11
Load current limitation Channel 1, 2, 3, 4	$I_{L(LIM)}$	–	4.5	–	A	1) V_{DS} = 26 V **LGCR.LED**n = 1	P_7.7.12
Over Temperature Protection							
Thermal shut down temperature	$T_{j(SC)}$	150	170	200	°C	1)	P_7.7.14
Thermal hysteresis of thermal shutdown	$\Delta T_{j(SC)}$	–	20	–	K	1)	P_7.7.15
Dynamic temperature increase limitation while switching	$\Delta T_{j(SW)}$	–	80	–	K	1)	P_7.7.16
Number of automatic retries at dynamic temperature sensor or over temperature shut down	n_{retry}	–	8	9		1)	P_7.7.17
Reverse Polarity							
Drain source diode voltage during reverse polarity Channel 1, 2, 3, 4	$V_{DS(REV)}$	400	650	800	mV	$I_L = I_{L(nom)}$ = P_6.6.17 T_j = 150 °C	P_7.7.20
Over Voltage							
Overvoltage protection	$V_{S(AZ)}$	42	47	54	V	I_S = 4 mA	P_7.7.22

1) Not subject to production test, specified by design.

8 Diagnosis

For diagnosis purpose, the SPOC+ BTS54040-LBA provides a current sense signal at pin IS and a diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

Please refer to **Figure 8-1** for details.

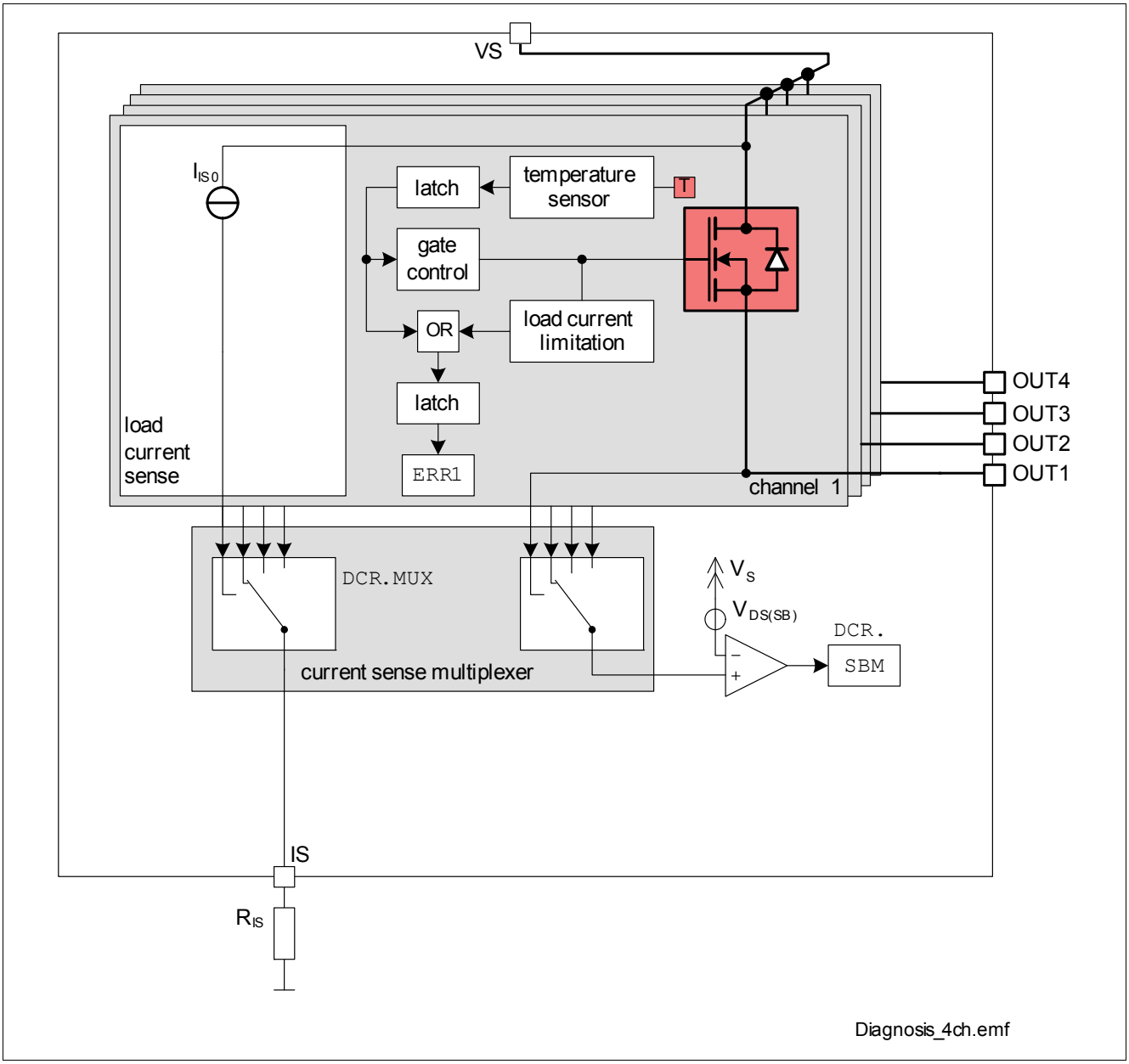


Figure 8-1 Block Diagram: Diagnosis

For diagnosis feedback at different operation modes, please see **Table 8-1**.

Table 8-1 Operation Modes [1)]

Operation Mode	Input Level OUT.OUTn	Output Level V_{OUT}	Current Sense I_{IS}	Error Flag ERR_COUNTERn[2)]	DCR.SBM bit
Normal Operation (**Channel OFF**)	L / 0 (OFF-state)	GND	Z	0	1
Short Circuit to GND		GND	Z	0	1
Thermal shut down		Z	Z	0[2)]	X
Short Circuit to V_S		V_S	Z	0	0
Open Load		Z	Z	0	X
Normal Operation (**Channel ON**)	H / 1 (ON-state)	~V_S	I_L / k_{ILIS}	0	0
Current Limitation		< V_S	Z	0	X
Dynamic or Absolute Thermal Limitation → Channel switched OFF		Z	Z	0	X
Dynamic or Absolute Thermal Limitation n_{retry} reached → Channel latched OFF		Z	Z	1[2)]	X
Short Circuit to GND		~GND	Z	0	1
Short Circuit to V_S		V_S	< I_L / k_{ILIS}	0	0
Open Load		V_S	Z	0	0

1) L = “low” level, H = "high" level, Z = high impedance, potential depends on leakage currents and external circuit. X = undefined.

2) The over temperature flag is set latched and can be cleared by setting **HWCR.CTC** bit to 1.

8.1 Diagnosis Word at SPI

Diagnostic information about the status of each channel are provided through SPI. In the Standard Diagnosis the **ERR_MUX** bit reports if there is a channel which had already enough restarts to reach the maximum allowed number of retries n_{retry} (P_7.7.17). If 2 or more channels are latched OFF due to that, **ERR_MUX** bits aren´t enough to identify which channels are OFF. In such cases, it is possible to get an overview channel by channel using **ERR_COUNTER** bits in Errors Diagnosis (see **Chapter 9.6.2**)

8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

8.2.1 Current Sense Signal

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided during ON-state as long as no failure mode occurs.The ratio k_{ILIS} can be adjusted to the load type (LED or bulb) via SPI register `LGCR`. The accuracy of the ratio k_{ILIS} depends on the load current and temperature.Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use resistors 1.5 kΩ < R_{IS} < 5 kΩ. A typical value is 2.7 kΩ.

The current sense signal of a channel is not active when the channel is OFF or when the protection functions (current limitation, over temperature or dynamic temperature sensors) are active. If the maximum number of automatic reactivations n_{retry} is reached ($n = n_{retry}$), the current sense signal of the affected channel is deactivated until the reset the counters by setting **HWCR.CTC** bit to 1.

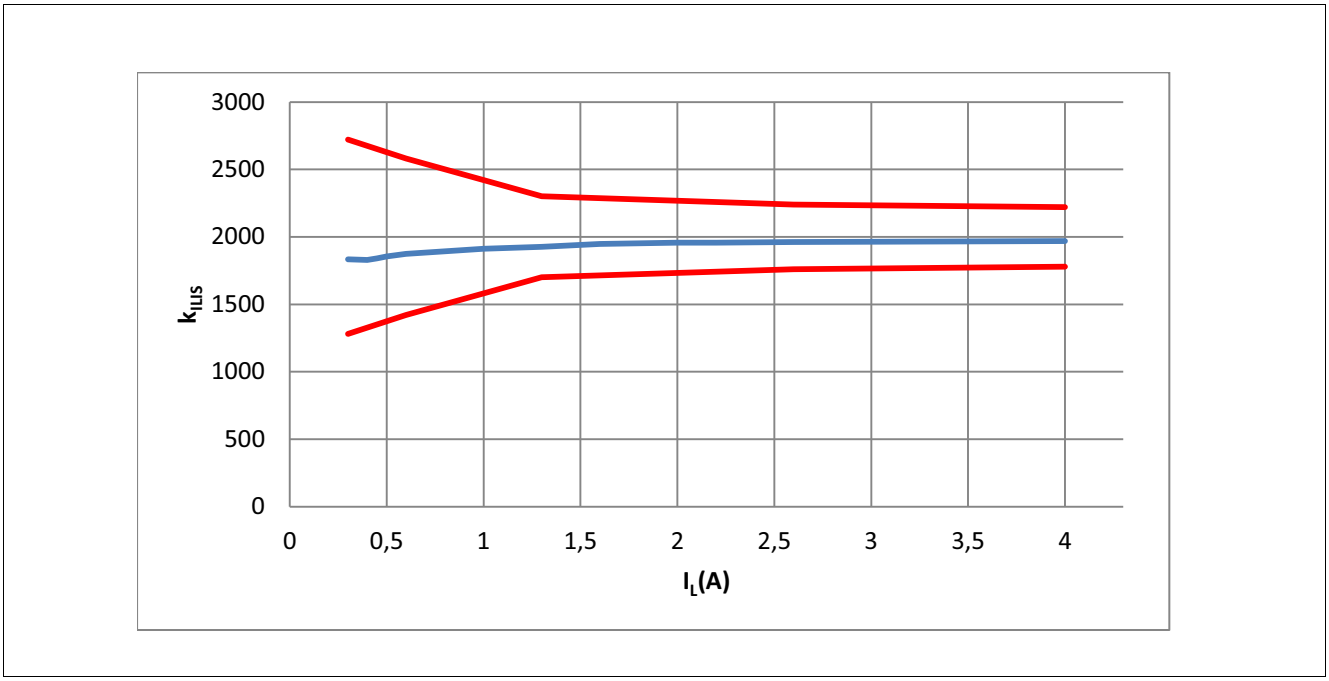


Figure 8-2 Current Sense Ratio k_{ILIS} Channel 1, 2, 3, 4 (Bulb mode)

Note: The curves show the behavior based on characterization data.

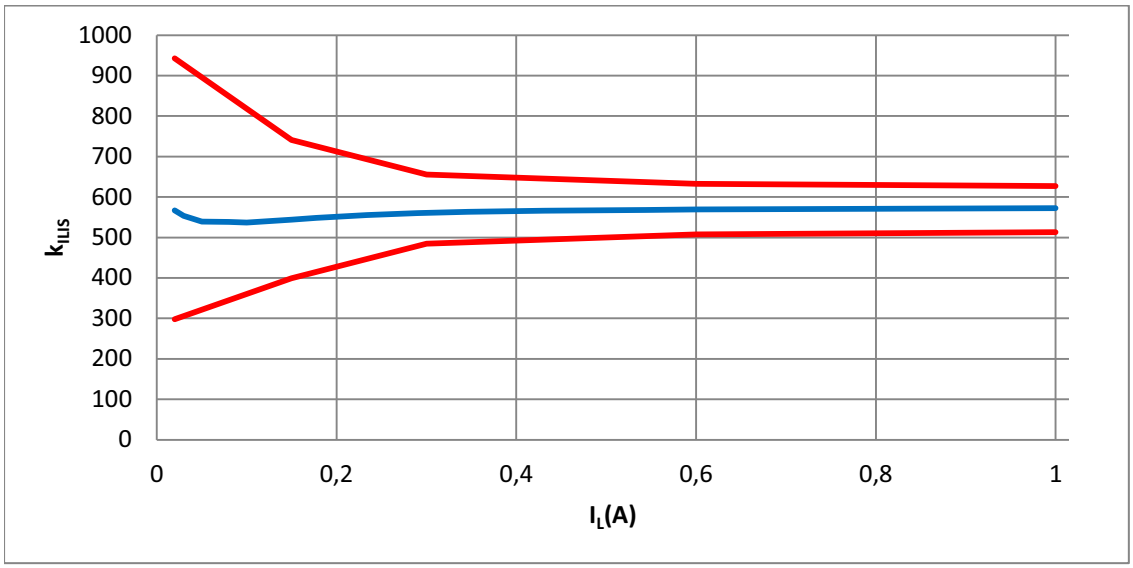


Figure 8-3 Current Sense Ratio k_{ILIS} Channel 1, 2, 3, 4 (LED mode)

Note: The curves show the behavior based on characterization data.

Details about timings between the current sense signal I_{IS} and the output voltage V_{OUT} and the load current I_L can be found in **Figure 8-4**.

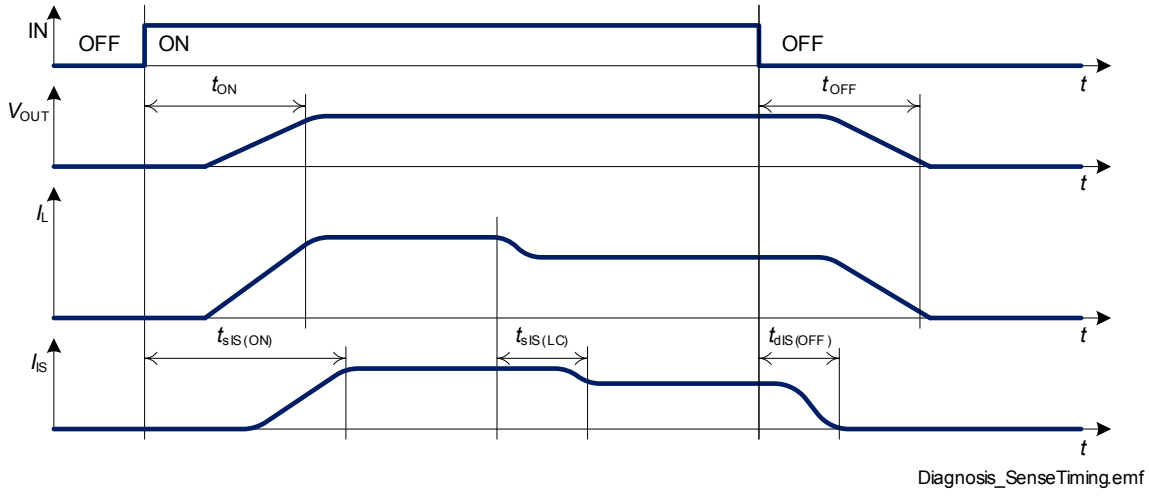


Figure 8-4 Current Sense Signal Timings

8.2.2 Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC+ BTS54040-LBA that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register **DCR.MUX**. The sense current also can be disabled by SPI register **DCR.MUX**. For details on timing of the current sense multiplexer, please refer to **Figure 8-5**.

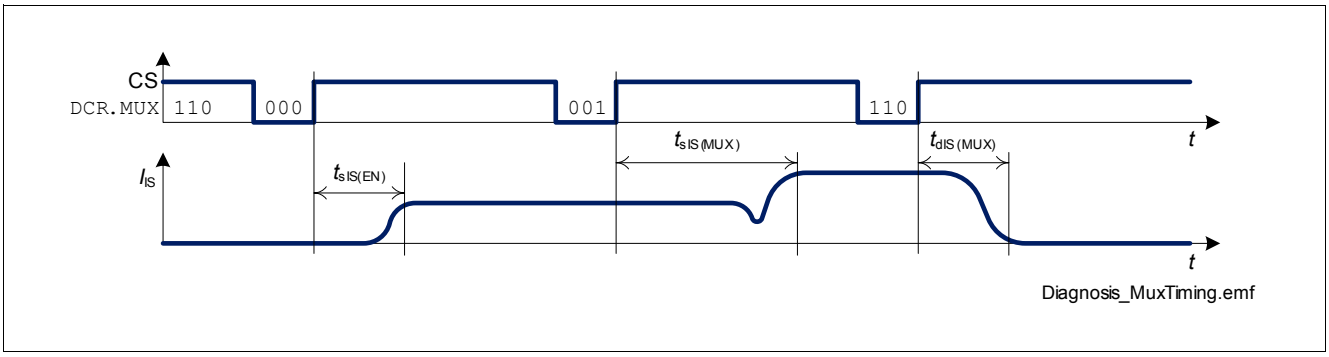


Figure 8-5 Current Sense Multiplexer Timings

8.3 Switch Bypass Monitor Diagnosis

To detect short circuit to V_S, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and V_S in ON-state, the current flows through the power transistor as well as through the short circuit (bypass) with undefined share between the two. As a result, the current sense signal shows lower values than expected by the load current. In OFF-state, the output voltage remains close to V_S potential which leads to a small V_{DS}.

The switch bypass monitor compares the threshold $V_{DS(SB)}$ with the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (**DCR.MUX**). The result of the comparison can be read in SPI register **DCR.SBM**.

8.4 Gate Back Regulation

To increase the current sense accuracy, the Gate Back Regulation (GBR) function is implemented. This function is active by default. According to output current, GBR function can be left active or disabled. **Table 8-2** indicates for which output currents this is necessary in order to fulfill the desired current accuracy.

The circuitry that controls GBR function can be deactivated with the following SPI command sequence:

- **SWCR.SWR** = 1 (11001100_B)
- **LGCR.GBR**n = 0 ($1101aaaa_B$ where "$aaaa$"$_B$ is the new value for **LGCR.GBR** bits
- (optional but recommended: **SWCR.SWR** = 0 (11000100_B)

Refer to **Chapter 9.7** for more details.

8.5 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C

Typical values: V_S = 13.5 V, V_{DD}= 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 1, 2, 3, 4: R_L = 6.8 Ω (33 Ω when **LGCR.LED**n = 1)

Measurement setup used for k_{ILIS} (unless otherwise specified):

When I_L ≤ 1.3 A all channels are ON at the same time with equal I_L

When I_L ≥ 2.0 A only the measured channel is ON, all other channels have I_L = 0

Table 8-2 Electrical Characteristics Diagnosis

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition Channel 1, 2, 3, 4 LGCR.LEDn = 0							
Current sense ratio I_{L03} = 300 mA	k_{ILIS03}	-36	2000	+36	%	–	P_8.5.49
Current sense ratio I_{L05} = 600 mA	k_{ILIS05}	-29	2000	+29	%	–	P_8.5.51
Current sense ratio I_{L07} = 1.3 A	k_{ILIS07}	-15	2000	+15	%	–	P_8.5.53
Current sense ratio I_{L09} = 2.6 A	k_{ILIS09}	-12	2000	+12	%	–	P_8.5.55
Current sense ratio I_{L10} = 4 A	k_{ILIS10}	-11	2000	+11	%	–	P_8.5.56
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition Channel 1, 2, 3, 4 LGCR.LEDn = 1							
Current sense ratio I_{L00} = 20 mA	k_{ILIS00}	-52	620	+52	%	–	P_8.5.57
Current sense ratio I_{L02} = 150 mA	k_{ILIS02}	-30	570	+30	%	–	P_8.5.59
Current sense ratio I_{L03} = 300 mA	k_{ILIS03}	-15	570	+15	%	–	P_8.5.60
Current sense ratio I_{L05} = 600 mA	k_{ILIS05}	-11	570	+11	%	–	P_8.5.62
Current sense ratio I_{L06} = 1 A	k_{ILIS06}	-10	570	+10	%	–	P_8.5.63
Sense pin maximum voltage	$V_{IS(AZ)}$	42	47	54	V	I_{IS} = 5 mA	P_8.5.75
Current Sense Drift Over Current and Temperature per Device							

Table 8-2 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense drift over current and temperature per device Channel 1, 2, 3, 4	$\Delta k_{ILIS(T)}$	-8	–	8	%	1) k_{ILIS09} versus k_{ILIS07} LGCR.LEDn = 0	P_8.5.80
Current sense drift over current and temperature per device Channel 1, 2, 3, 4	$\Delta k_{ILIS(T)}$	-9.5	–	9.5	%	1) k_{ILIS05} versus k_{ILIS03} LGCR.LEDn = 1	P_8.5.81
Current Sense Drift of Unaffected Channel during Inverse Current of other Channels One channel with $I_{L(IC)}$ = - I_{Ln} , all other channels with I_{Ln} DCR.MUX ≠ <111, 110> and set to sense any of the channels not in Inverse current condition							
Current sense drift of unaffected channels during inverse current of one channel	$\Delta k_{ILIS(IC)}$	-20	–	20	%	1) I_{L1} = 2.6 A I_{L2} = 2.6 A I_{L3} = 2.6 A I_{L4} = 2.6 A	P_8.5.84
Sense Pin - Currents							
Maximum steady state current sense output current Channel 1, 2, 3, 4	$I_{IS(MAX)}$	3.8	–	15	mA	V_{IS} = 0 V V_S ≥ 8 V	P_8.5.88
Current sense leakage / offset current	$I_{IS(en)}$	–	–	3.2	µA	I_L = 0 mA LGCR.GBR = ON DCR.MUX ≠ <111,110>$_B$	P_8.5.90
Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	0.01	1	µA	I_{L2} = 2.6 A DCR.MUX = 110$_B$	P_8.5.98
Sense Pin - Timings							
Current sense settling time after channel activation Channel 1, 2, 3, 4	$t_{sIS(ON)}$	–	–	250	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ LGCR.LEDn = 0	P_8.5.103
Current sense settling time after channel activation Channel 1, 2, 3, 4	$t_{sIS(ON)}$	–	–	100	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ LGCR.LEDn = 1	P_8.5.104
Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$	–	–	25	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ	P_8.5.106

Table 8-2 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense settling time after change of load current Channel 1, 2, 3, 4	$t_{sIS(LC)}$	–	–	25	µs	1) I_L = 2.6 A to 1.3 A V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LED**n = 0	P_8.5.111
Current sense settling time after change of load current Channel 1, 2, 3, 4	$t_{sIS(LC)}$	–	–	25	µs	1) I_L = 1.0 A to 0.6 A V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LED**n = 1	P_8.5.112
Current sense settling time after current sense activation	$t_{sIS(EN)}$	–	–	25	µs	R_{IS} = 2.7 kΩ I_{L2} = 2.6 A **DCR.MUX**: $110_B \rightarrow 001_B$	P_8.5.114
Current sense settling time after multiplexer channel change	$t_{sIS(MUX)}$	–	–	25	µs	R_{IS} = 2.7 kΩ I_{L2} = 2.6 A I_{L3} = 4 A **DCR.MUX**: $001_B \rightarrow 010_B$	P_8.5.115
Current sense deactivation time	$t_{dIS(MUX)}$	–	–	25	µs	1) R_{IS} = 2.7 kΩ **DCR.MUX**: $010_B \rightarrow 110_B$	P_8.5.116
Switch Bypass Monitor							
Switch bypass monitor threshold	$V_{DS(SB)}$	1.5	3.3	4.5	V	OFF state	P_8.5.117

1) Not subject to production test, specified by design.

9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CS. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CS indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CS. A modulo 8 counter ensures that data is taken only when a multiple of 8 bit has been transferred. The interface provides daisy chain capability with 8 bit SPI devices.

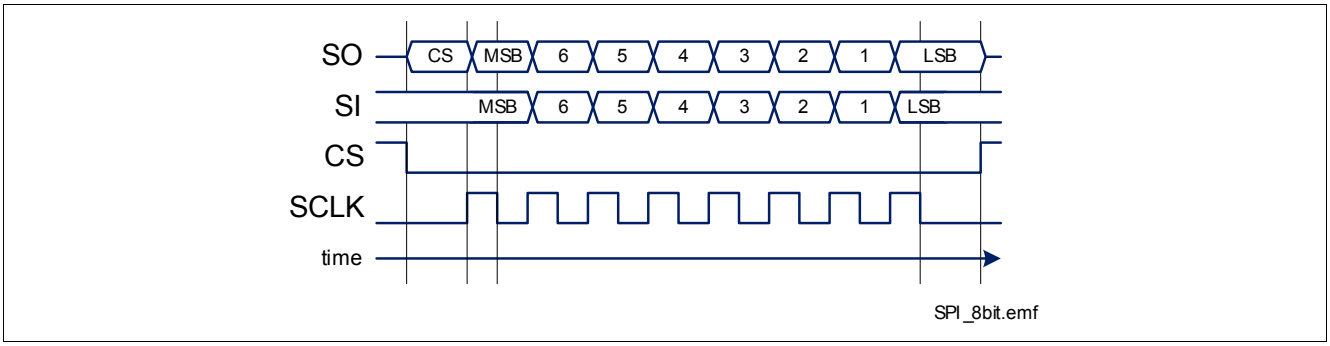


Figure 9-1 Serial Peripheral Interface

9.1 SPI Signal Description

CS - Chip Select

The system micro controller selects the SPOC+ BTS54040-LBA by means of the CS pin. Whenever the pin is in “low” state, data transfer can take place. When CS is in "high" state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CS “high” to “low” Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to "high" or “low” state depending on the signal level at pin SI.

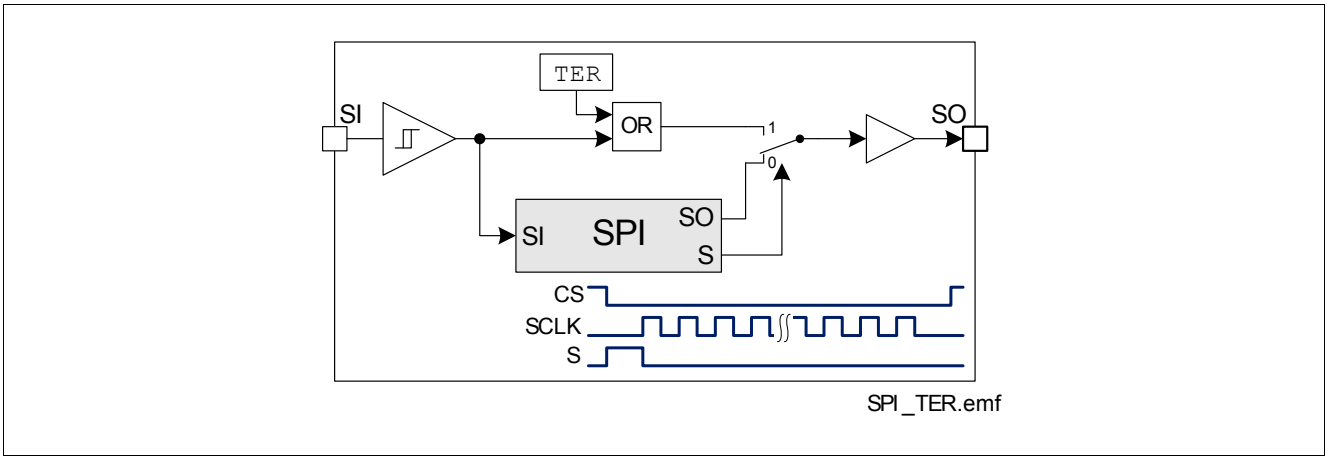


Figure 9-2 Combinatorial Logic for TER Flag

CS “low” to "high" Transition

- Command decoding is only done, when after the falling edge of CS exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select CS makes any transition, otherwise the command may be not accepted.

SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 9.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CS pin goes to “low” state. New data will appear at the SO pin following the rising edge of SCLK.

For the SPI Diagnosis readout operation the transmission error flag (TER) appears in positions D8 and D6 on SO pin while for other readout operations it is only in position D8.

Please refer to **Chapter 9.5** for further information.

SO	**TER**	**7**	**TER / 6**	**5**	**4**	**3**	**2**	**1**	**0**

9.2 Daisy Chain Capability

The SPI of SPOC+ BTS54040-LBA provides daisy chain capability. In this configuration several devices are activated by the same CS signal MCS. The SI line of one device is connected with the SO line of another device (see **Figure 9-3**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

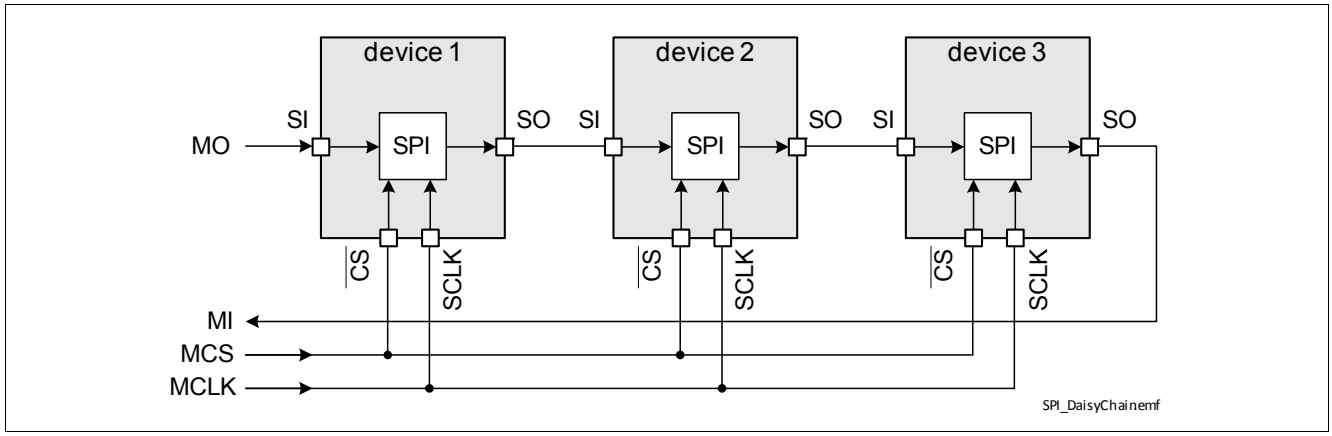


Figure 9-3 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CS line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCS line must turn “high” (see **Figure 9-4**).

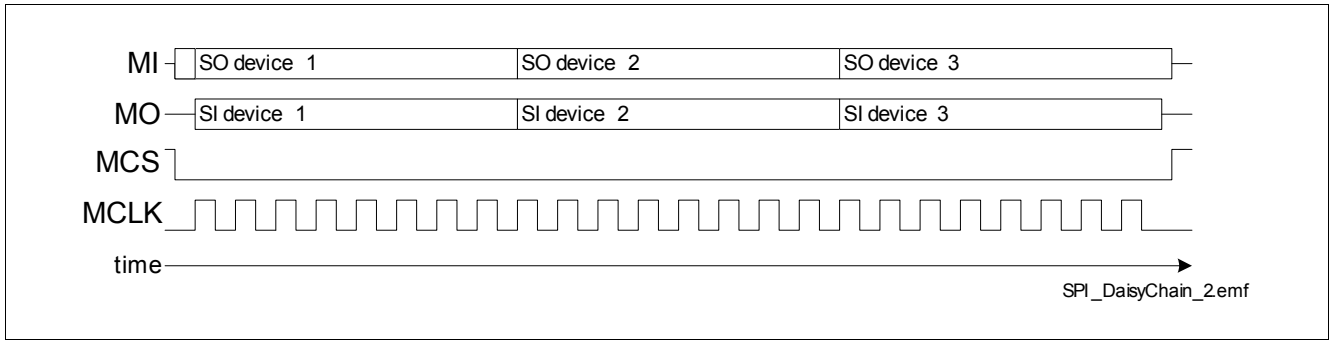


Figure 9-4 Data Transfer in Daisy Chain Configuration

9.3 Timing Diagrams

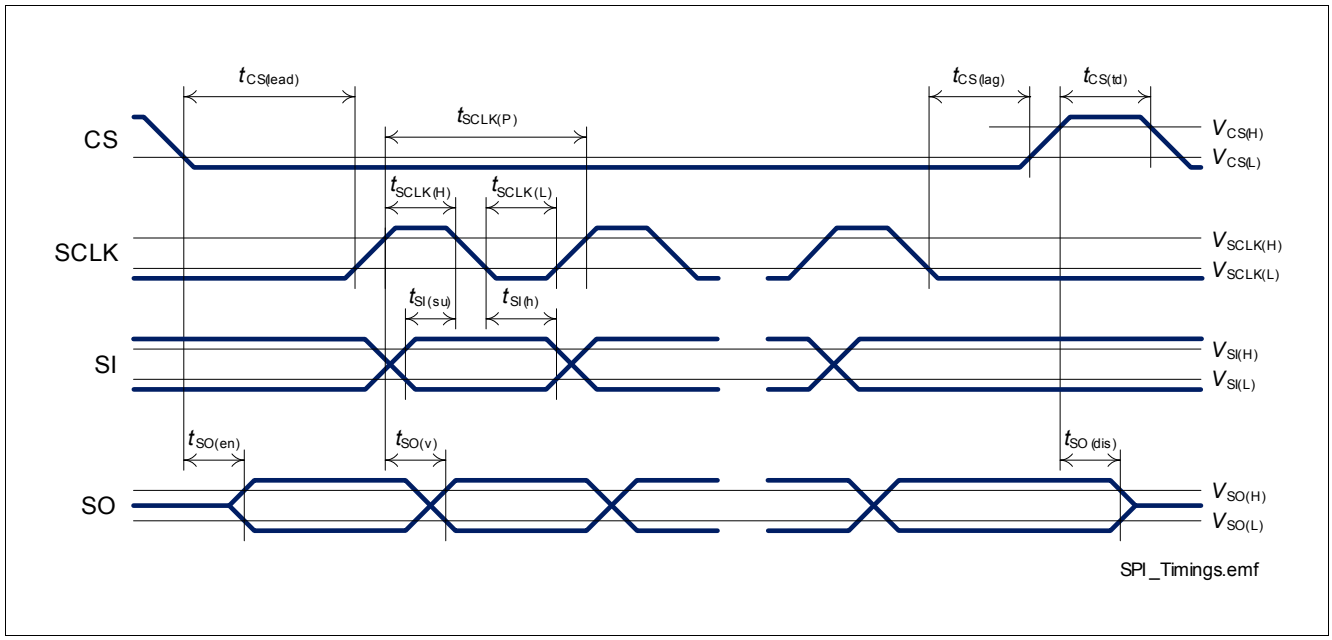


Figure 9-5 Timing Diagram SPI Access

9.4 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, T_j = -40 °C to +150 °C, V_{DD} = 3.8 V to 5.5 V
Typical values: V_S = 13.5 V, T_j = 25 °C, V_{DD} = 4.3 V

Table 9-1 Electrical Characteristics Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CS, SCLK, SI) - L Level of pin							
CS	$V_{CS(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.1
SCLK	$V_{SCLK(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.2
SI	$V_{SI(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.3
Input Characteristics (CS, SCLK, SI) - H Level of pin							
CS	$V_{CS(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.4
SCLK	$V_{SCLK(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.5
SI	$V_{SI(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.6
L-input pull-up current at CS pin	$-I_{CS(L)}$	7	30	75	µA	V_{DD} = 4.3 V V_{CS} = 1.0 V	P_9.4.7
H-input pull-up current at CS pin	$-I_{CS(H)}$	3	27	75	µA	V_{DD} = 4.3 V V_{CS} = 2.6 V	P_9.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	3	27	75	µA	V_{SCLK} = 1.0 V V_{DD} = 4.3 V	P_9.4.9
SI	$I_{SI(L)}$	3	27	75	µA	V_{SI} = 1.0 V V_{DD} = 4.3 V	P_9.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	7	30	75	µA	V_{SCLK} = 2.6 V V_{DD} = 4.3 V	P_9.4.11
SI	$I_{SI(H)}$	7	30	75	µA	V_{SI} = 2.6 V V_{DD} = 4.3 V	P_9.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	–	0.5	V	I_{SO} = -0.5 mA	P_9.4.13
H level output voltage	$V_{SO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{SO} = 0.5 mA V_{DD} = 4.3 V	P_9.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CS} =V_{DD} V_{SO} = 0 V V_{SO} = V_{DD}	P_9.4.15
Timings							
Enable lead time (falling CS to rising SCLK)	$t_{CS(lead)}$	200	–	–	ns	–[1)]	P_9.4.16
Enable lag time (falling SCLK to rising CS)	$t_{CS(lag)}$	200	–	–	ns	–[1)]	P_9.4.17
Transfer delay time (rising CS to falling CS)	$t_{CS(td)}$	1	–	–	µs	–[1)]	P_9.4.18

Table 9-1 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output enable time (falling CS to SO valid)	$t_{SO(en)}$	–	–	1	µs	1) C_L = 20 pF	P_9.4.19
Output disable time (rising CS to SO tristate)	$t_{SO(dis)}$	–	–	1	µs	1) C_L = 20 pF	P_9.4.20
Serial clock frequency	f_{SCLK}	0	–	2.5	MHz	–1)	P_9.4.22
Serial clock period	$t_{SCLK(P)}$	400	–	–	ns	–1)	P_9.4.24
Serial clock "high" time	$t_{SCLK(H)}$	200	–	–	ns	–1)	P_9.4.26
Serial clock "low" time	$t_{SCLK(L)}$	200	–	–	ns	–1)	P_9.4.28
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	80	–	–	ns	–1)	P_9.4.30
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	80	–	–	ns	–1)	P_9.4.32
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	200	ns	1) C_L = 20 pF	P_9.4.34

1) Not subject to production test, specified by design

9.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 9-6**. SI line represents the frame sent from the µC and SO line is the answer provided by SPOC+ BTS54040-LBA. The “(previous response)” means that the frame sent back depends on the command frame sent from the µC before.

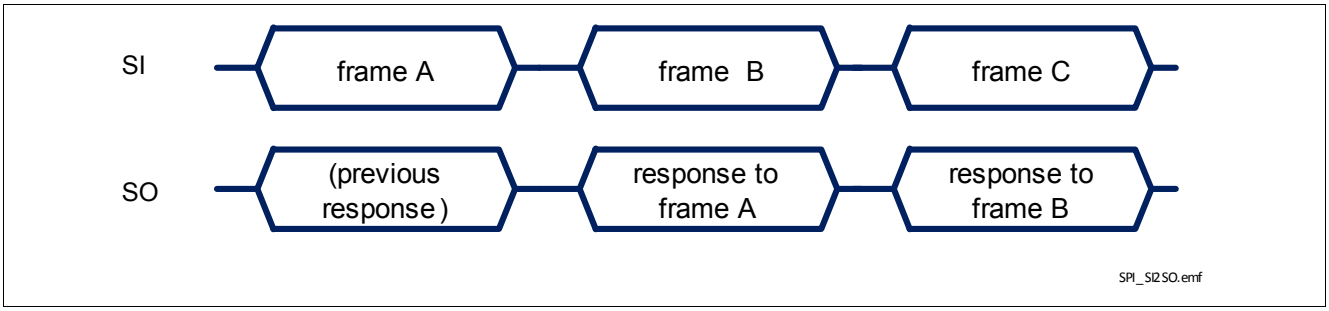


Figure 9-6 Relationship between SI and SO during SPI communication

The SPI protocol will provide the answer to a command frame only with the next trasmission triggered by the µC. Although the biggest majority of commands and frames implemented in SPOC+ BTS54040-LBA can be decoded without the knowledge of what happened before, it is advisable to consider what the µC sent in the previous transmission to decode SPOC+ BTS54040-LBA response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:

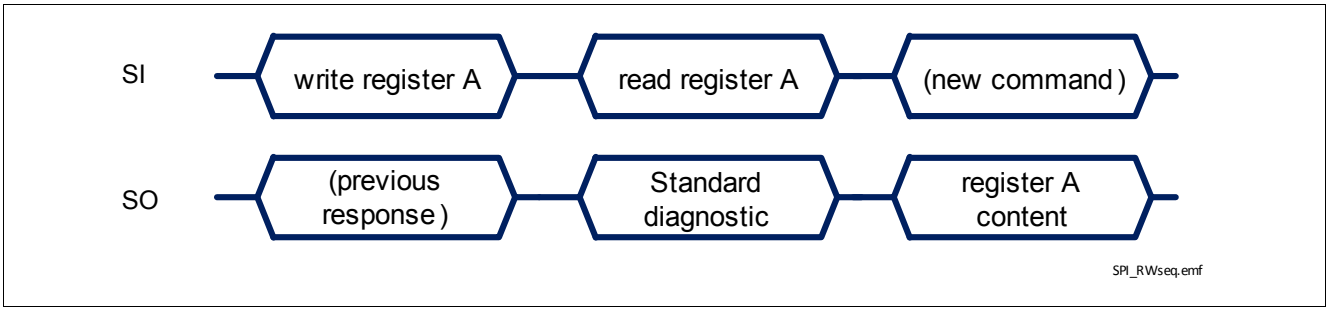


Figure 9-7 Register content sent back to µC

There are 2 special situations where the frame sent back to the µC doesn´t depend on the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8), shown in **Figure 9-8**
- when BTS54040-LBA logic supply comes out of Power-On reset condition, as shown in **Figure 9-9**

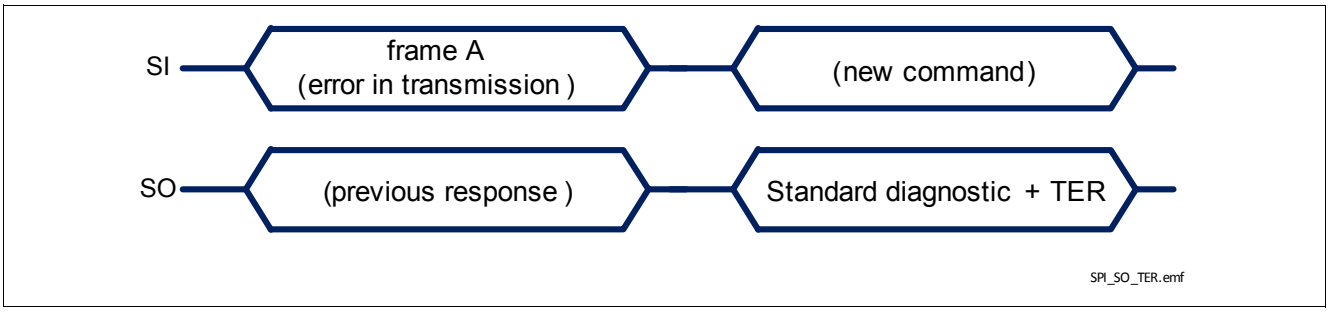


Figure 9-8 BTS54040-LBA response after a error in transmission

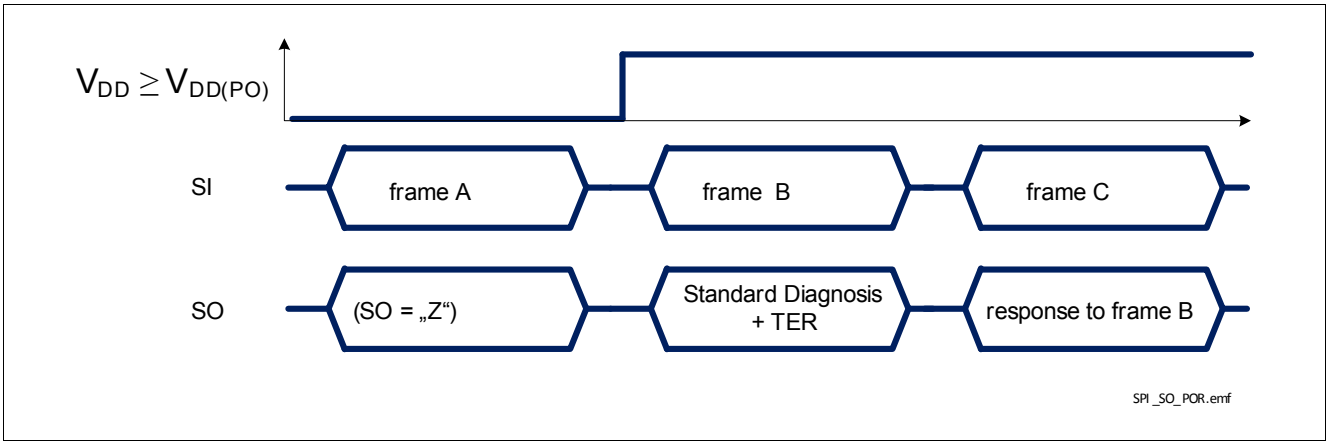


Figure 9-9 BTS54040-LBA response after coming out of Power-On reset at V_{DD}

A summary of all possible SPI commands is presented in **Table 9-2**, including the answer that SPOC+ BTS54040-LBA will send back at the next transmission.

Table 9-2 SPI Command summary

Requested Operation	Frame sent to SPOC+ (SI pin)	Frame received from SPOC+ (SO pin) with the next command
Write OUT register	$100xaaaa_B$ where: “$xaaaa_B$” = new OUT register content (“xx_B” = don´t care)	$0aaaaaaa_B$ (Standard Diagnosis)
Read OUT register	$00xx0000_B$ (“xx_B” = don´t care)	$10aaaaaa_B$ (“$aaaaaa_B$” = OUT register content)
Write Configuration register	$11aabbbb_B$ where: “aa_B” = register address “$bbbb_B$” = new register content	$0aaaaaaa_B$ (Standard Diagnosis)
Read Configuration register	$01aa0000_B$ where: “aa_B” = register address	$11aabbbb_B$ where: “aa_B” = register address “$bbbb_B$” = register content
Read Standard Diagnosis	$0xxx0001_B$ (“xxx_B” = don´t care)	$0aaaaaaa_B$ (Standard Diagnosis)
Read Error Diagnosis	$0xxx0011_B$ (“xxx_B” = don´t care)	$00aaaaaa_B$ (Errors Diagnosis)

9.6 SPI Diagnosis Registers

9.6.1 Standard Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	TER	LHI	STB	VSMON	ERR_MUX			50_H

Field	Bits	Type	Description
TER	6	r	**Transmission Error** 0_B (default) Previous transmission was successful (modulo 8 clocks received) 1_B Previous transmission failed or first transmission after reset
LHI	5	r	**Limp Home monitor** 0_B (default) Normal mode operation 1_B Limp Home Mode
STB	4	r	**Standby mode monitor** 0_B (default) Normal mode operation 1_B Standby mode
VSMON	3	r	**V_S monitor** 0_B (default) V_S always > V_{SMON} since last Standard Diagnosis readout 1_B V_S < V_{SMON} at least once
ERR_MUX	X	r	**Diagnosis of Channel n in error** 000_B (default) No latch off 001_B Channel one latch off 010_B Channel two latch off 011_B Channel three latch off 100_B Channel four latch off 101_B Not used 110_B Not used 111_B More than one channel latch off

Notes:

1. *V_S monitoring is disabled in Stand-by mode (MUX = „111“) to allow SPI configuration without V_S voltage applied.*
2. *As long as V_S < V_{SMON} the SPI command is not taken over by the SPI. TER and VSMON bits are set.*

9.6.2 Errors Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	0	0	1	ERR_COUNTER4	ERR_COUNTER3	ERR_COUNTER2	ERR_COUNTER1	10_H

Field	Bits	Type	Description
ERR_COUNTERn n = 4 to 1	X	r	**Diagnosis of Channel n** 0_B (default) No failure 1_B Over temperature counter reached to n_{retry}

9.7 SPI Configuration Registers

9.7.1 Output Configuration Register

SWCR.SWR = 0

Bit	7	6	5	4	3	2	1	0	
Name	**W = 1 R = 0**	**RB**	**5**	**4**	**3**	**2**	**1**	**0**	**Default**
OUT	W/R	0	0	x	OUT4	OUT3	OUT2	OUT1	80_H

SWCR.SWR = 1

Bit	7	6	5	4	3	2	1	0	
Name	**W = 1 R = 0**	**RB**	**5**	**4**	**3**	**2**	**1**	**0**	**Default**
OUT	R	0	LHI	1	INST4	INST3	INST2	INST1	90_H

9.7.2 Swap Configuration Register

Bit	7	6	5	4	3	2	1	0	Default
Name	**W = 1 R = 0**	**RB**	**ADDR**		**3**	**2**	**1**	**0**	
SWCR	W/R	1	0	0	SWR	1	0	0	$C4_H$

9.7.3 LED Mode Configuration Register

SWCR.SWR = 0

Name	W = 1 R = 0	RB	ADDR		3	2	1	0	Default
LGCR	W/R	1	0	1	LED4	LED3	LED2	LED1	$D0_H$

9.7.4 Gate Back Regulation Register

SWCR.SWR = 1

Name	W = 1 R = 0	RB	ADDR		3	2	1	0	Default
LGCR	W/R	1	0	1	GBR4	GBR3	GBR2	GBR1	DF_H

9.7.5 Hardware Configuration Register

Name	W = 1 R = 0	RB	ADDR		3	2	1	0	Default
HWCR	R	1	1	0	RCR	COL	STB	0	$E2_H$
	W	1	1	0	RCR	COL	RST	CTC	-

9.7.6 Diagnosis Control Register

Name	W = 1 R = 0	RB	ADDR		3	2	1	0	Default
DCR	R	1	1	1	SBM	MUX			$F7_H$
	W	1	1	1	0	MUX			-

Field	Bits	Type	Description
RB	6	rw	**Register Bank** 0_B (default) Read / write to the OUTn channel 1_B Read / write to the other register
OUT.OUTn n = 4 to 1	n-1	rw	**Output Control Register of Channel n**[1)] 0_B (default) OFF 1_B ON
OUT.INSTn n = 4 to 1	n-1	r	**Input Status Monitor Channel n** 0_B (default) Input signal “low” 1_B Input signal "high"
LGCR.LEDn n = 4 to 1	n-1	rw	**Set LED Mode for Channel n**[2)] 0_B (default) Channel n is in bulb mode 1_B Channel n is in LED mode
LGCR.GBRn n = 4 to 1	n-1	rw	**Gate Back Regulation for Channel n** 0_B Gate back regulation for Channel n is forced OFF 1_B (default) Gate back regulation for Channel n is active
HWCR.CTC	0	w	**Clear Thermal Counter** 0_B (default) Thermal and over current latches are untouched 1_B Command: Clear all thermal and over current latches
HWCR.RST	1	w	**Reset Command** 0_B (default) Normal operation 1_B Execute reset command
HWCR.STB	1	r	**Standby Mode** 0_B Device is awake 1_B (default) Device is in Standby mode
HWCR.COL	2	rw	**Input Combinatorial Logic Configuration** 0_B (default) Input signal OR-combined with according OUT register bit[3)] 1_B Input signal AND-combined with according OUT register bit
HWCR.RCR	3	w	**Retry Counter Reset** 0_B (default) Retry Counter is reset only for **HWCR.CTC**=1 (and V_{DD} reset) 1_B Retry Counter is reset for every IN-pin or OUT-bit "high" to “low” transition for nretry < 8 and also for **HWCR.CTC**=1 (and V_{DD} reset)
SWCR.SWR	1	rw	**Switch Register** 0_B (default) LED and OUT transmitted 1_B GBR and INST transmitted

Field	Bits	Type	Description
DCR.SBM	3	r	**Switch Bypass Monitor**[3] 0_B $V_{DS}<V_{DS(SB)}$ 1_B $V_{DS}>V_{DS(SB)}$
DCR.MUX	2:0	rw	**Set Current Sense Multiplexer Configuration in OFF-state** 000_B IS pin is high impedance 001_B IS pin is high impedance 010_B IS pin is high impedance 011_B IS pin is high impedance 100_B IS pin is high impedance 101_B IS pin is high impedance 110_B IS pin is high impedance 111_B Stand-by mode (IS pin is high impedance) **Set Multiplexer Configuration in ON-state** 000_B Current sense of channel 1 is routed to IS pin 001_B Current sense of channel 2 is routed to IS pin 010_B Current sense of channel 3 is routed to IS pin 011_B Current sense of channel 4 is routed to IS pin 101_B IS pin is high impedance 110_B IS pin is high impedance 111_B Stand-by mode (IS pin is high impedance))

1) If **SWCR.SWR** = 1 every readout of the register shows the state of the channels' input pins (**OUT.INST** bits).
2) if **SWCR.SWR** = 1 every read or write operation done on the register will affect **LGCR.GBR** bits instead of **LGCR.LED** bits
3) In Limp Home Mode (LHI = 1) the combinatorial logic is switched to OR-mode.

9.8 SPI Registers Overview

Address	Name	Description
00	SWCR	**Swap Configuration Register**
01	LGCR	**LED Mode configuration Register** if **SWCR.SWR** = 0
		Gate Back Regulation Register if **SWCR.SWR** = 1
10	HWCR	**Hardware Configuration Register**
11	DCR	**Diagnosis Control Register**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**		
Name	**$\overline{W}$ = 1 $\overline{R}$ = 0**								**SWR**	**Default**
SWCR	W/R	1	0	0	SWR	1	0	0	-	$C4_H$
OUT	W/R	0	0	x	OUT4	OUT3	OUT2	OUT1	0	80_H
OUT	R	0	LHI	1	INST4	INST3	INST2	INST1	1	90_H
LGCR	W/R	1	0	1	LED4	LED3	LED2	LED1	0	$D0_H$
LGCR	W/R	1	0	1	GBR4	GBR3	GBR2	GBR1	1	DF_H
HWCR	R	1	1	0	RCR	COL	STB	0	-	$E2_H$
	W	1	1	0	RCR	COL	RST	CTC	-	-
DCR	R	1	1	1	SBM	MUX			-	$F7_H$
	W	1	1	1	0	MUX			-	-
STD_DIAG	0	TER	LHI	STB	VSMON	ERR_MUX			-	50_H
DIAG_ERR_COUNTER	0	0	0	1	ERR_COUNTER4	ERR_COUNTER3	ERR_COUNTER2	ERR_COUNTER1	-	10_H

10 Application Description

The following Figure describs a typical operating circuit. It shall not be considered as a warranty of a certain functionality, condition or quality of the device. The **Table 10-1** shows suggested component values and purposes.

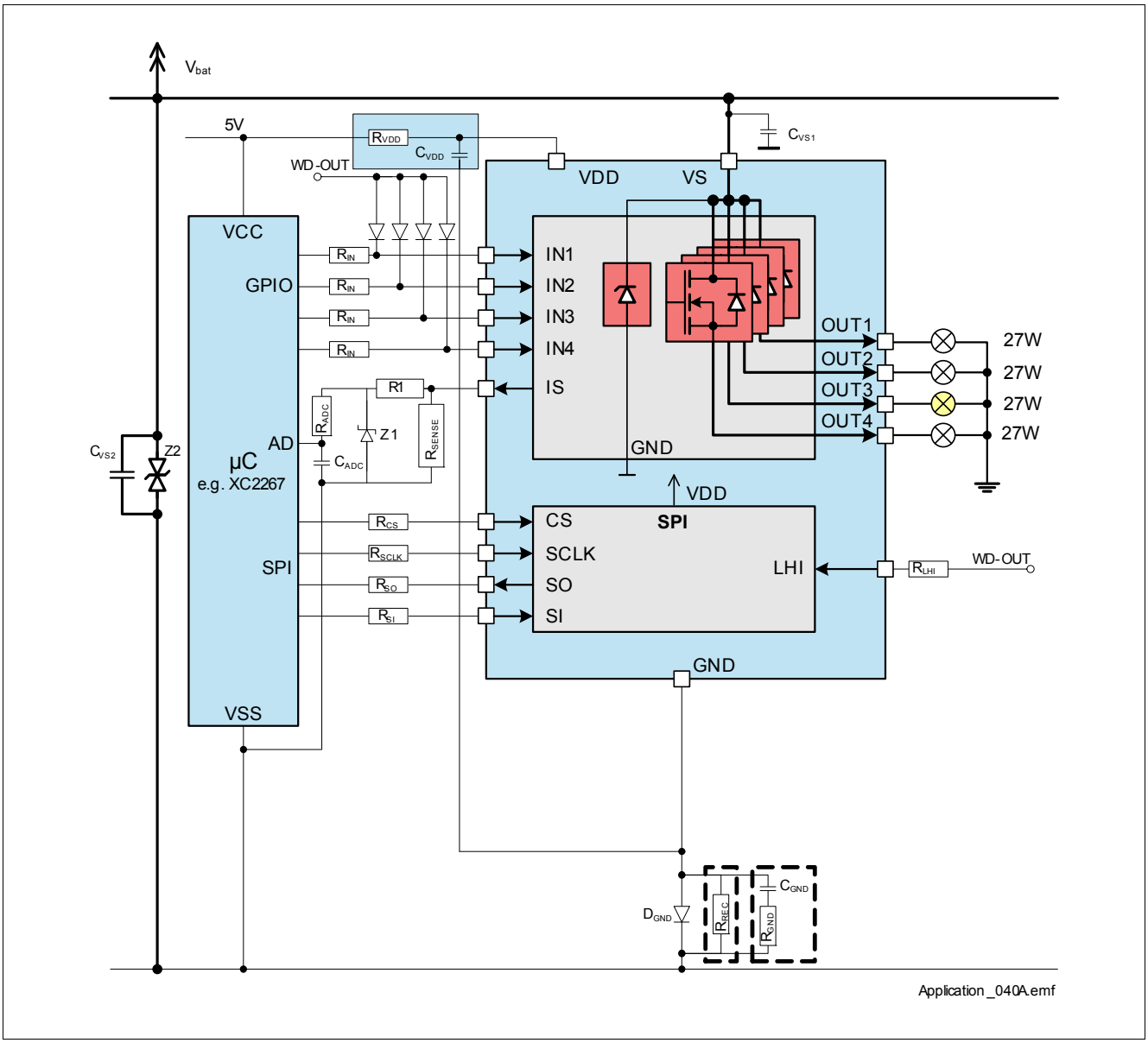


Figure 10-1 Application Circuit Example

Table 10-1 Suggested Component values

Reference	Value	Purpose
R_{VDD}	500 Ω	Device logic protection
R_{IN}	8 kΩ	Protection of the µC during overvoltage, reverse polarity and loss of ground
R_1	4.7 kΩ	Protection resistor for overvoltage, reverse polarity and loss of ground. Value to be tuned with µC specification
R_{IS}	2.7 kΩ	Sense resistor
R_{ADC}	1 kΩ	µC-ADC voltage spikes filtering
R_{CS}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SCLK}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SO}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SI}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{LHI}	8 kΩ	Protection of the µC during overvoltage and reverse polarity
C_{ADC}	1 nF	µC-ADC voltage spikes filtering
C_{VDD}	100 nF	Logic supply voltage spikes filtering
C_{VS1}	68 nF	Battery voltage spikes filtering
C_{VS2}	100 nF	Battery voltage spikes filtering
C_{GND}	8.2 nF	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
R_{GND}	100 Ω	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
R_{REC}	1 kΩ	Ground voltage recycling path (optional for providing a recycle path in case of loss of Battery)
Z_1	7 V	Protection of µC during overvoltage. Zener diode
Z_2	P6SMB30	Protection of device during overvoltage. Zener diode
D	BAS70	Protection of device during reverse polarity. Schottky diode

11 Package Outlines SPOC+ BTS54040-LBA

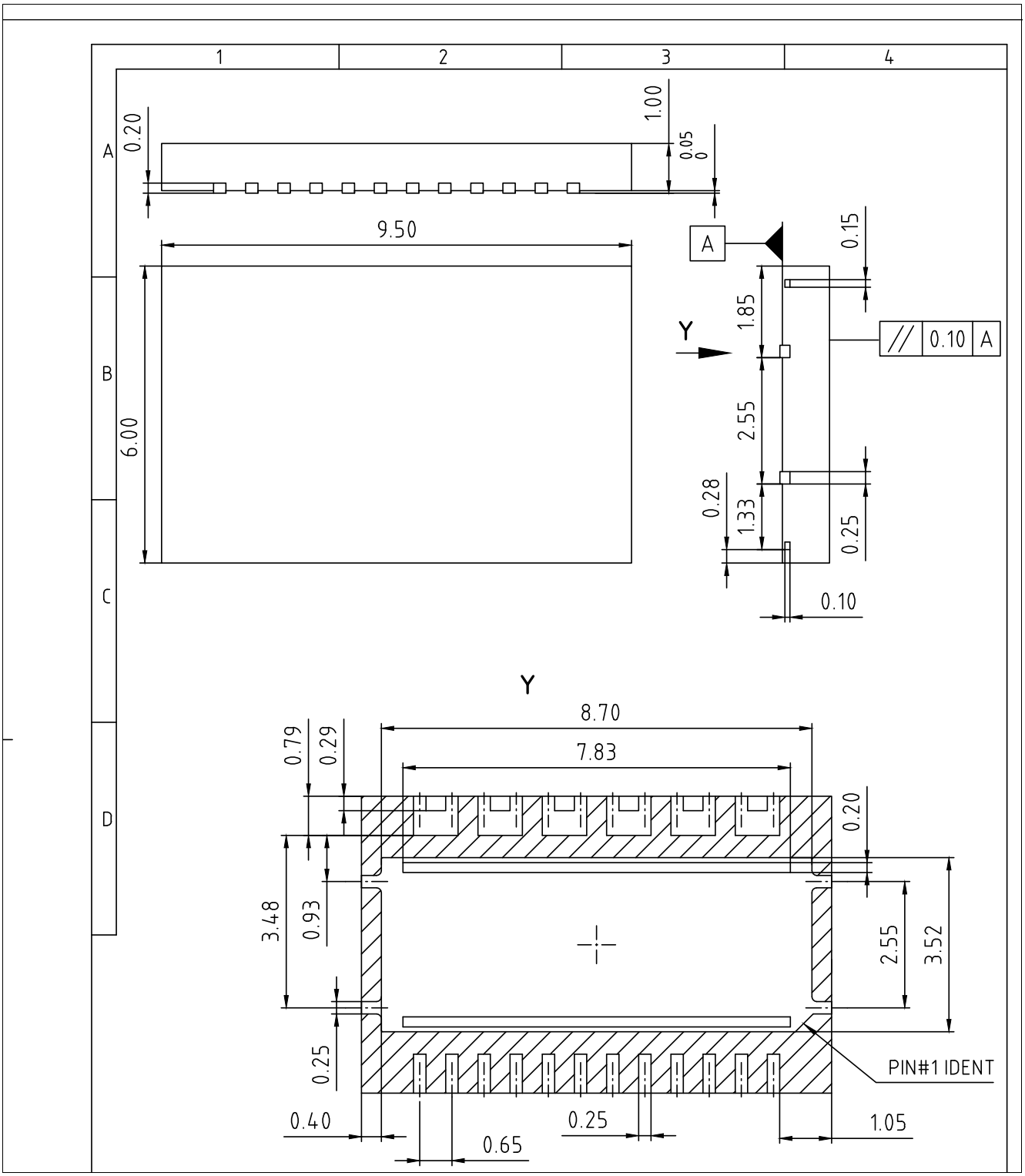


Figure 11-1 TSON-24-3 Package drawing

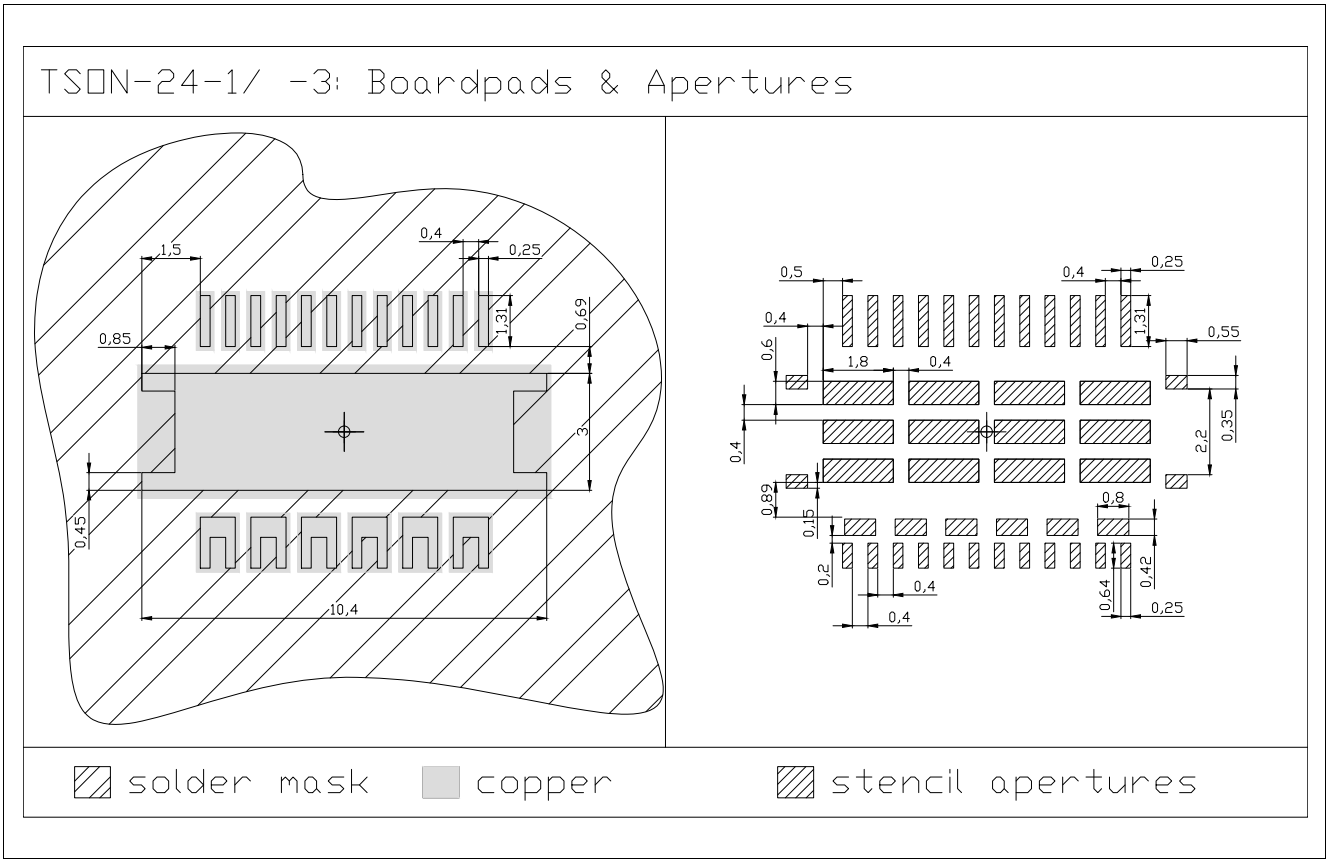


Figure 11-2 TSON-24-3 Package pads and stencil

Green Product (RoHS Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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