

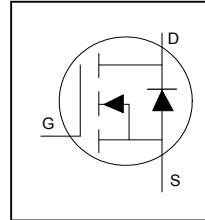
**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

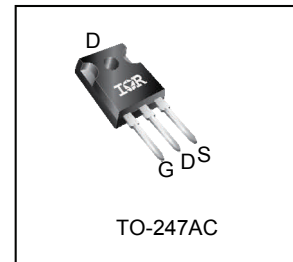
**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET

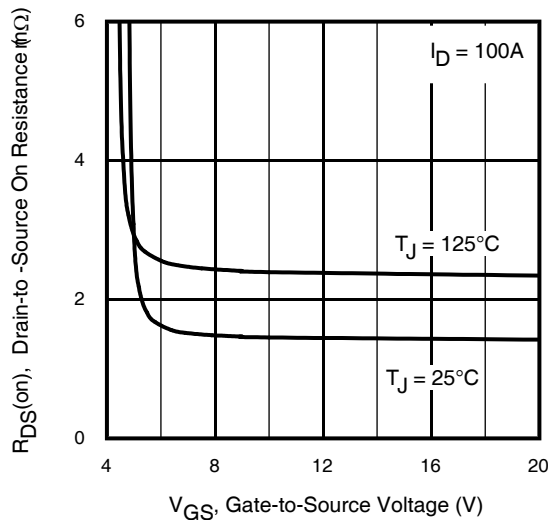


<b>V<sub>DSS</sub></b>	<b>75V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>1.45mΩ</b>
	<b>max</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>355A①</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>195A</b>

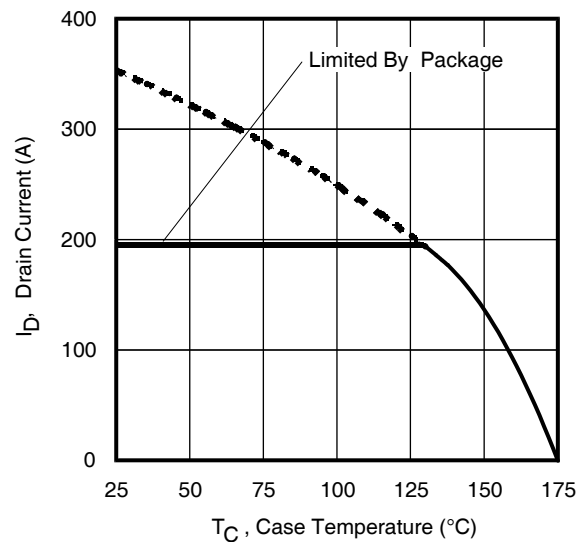


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP7718PbF	TO-247	Tube	25	IRFP7718PbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	355 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	250 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1590 <sup>②</sup>	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	517	W
	Linear Derating Factor	3.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	1160	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	2004	
$I_{AR}$	Avalanche Current <sup>⑤</sup>	See Fig 14, 15, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>⑥</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑦</sup>	—	0.29	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	42	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 2\text{mA}$ <sup>⑧</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.45	1.80	mΩ	$V_{GS} = 10\text{V}, I_D = 100\text{A}$
		—	1.60	—		$V_{GS} = 6\text{V}, I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	0.9	—	Ω	

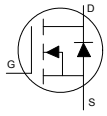
**Notes:**

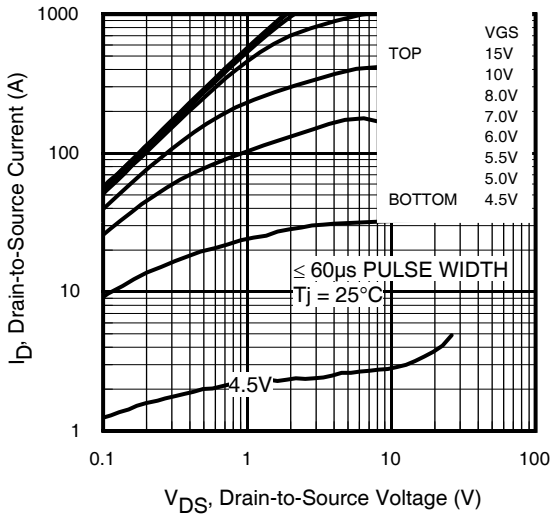
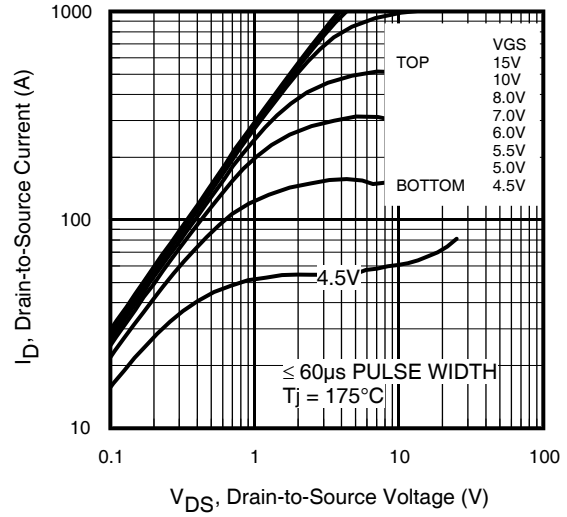
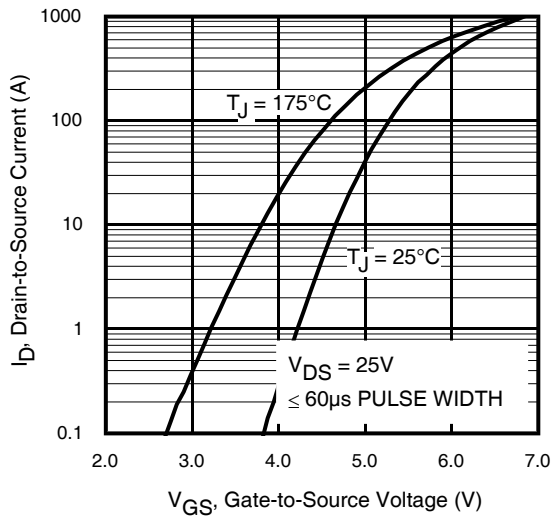
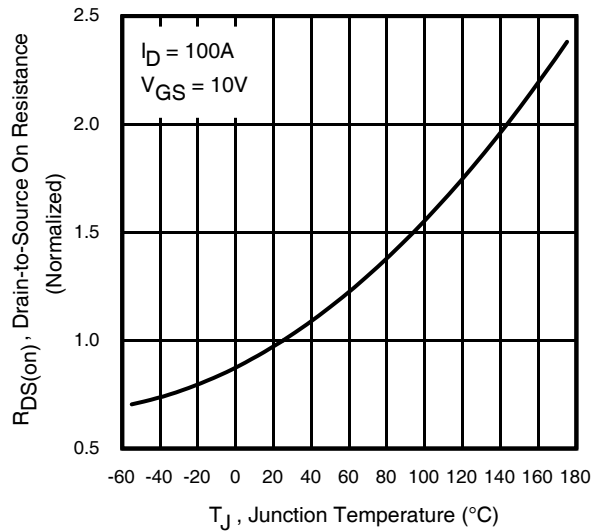
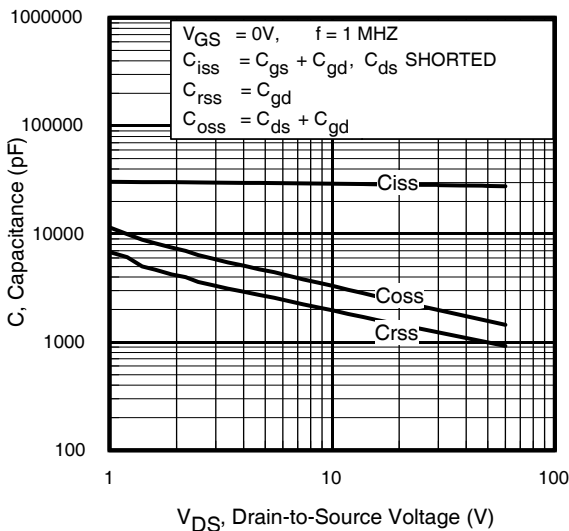
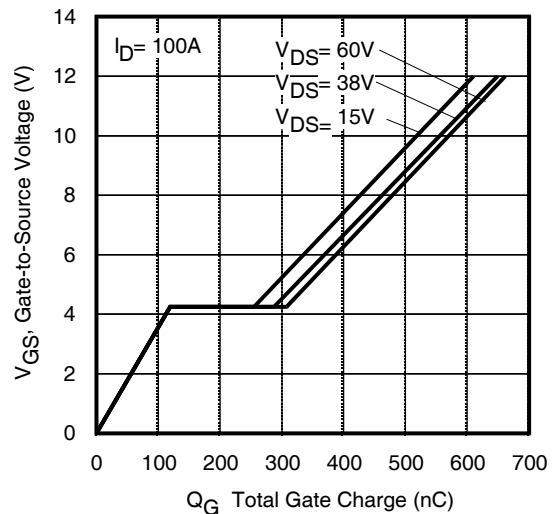
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 233\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 1279\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 63\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑩ Pulse drain current is limited at 780A by source bonding technology.

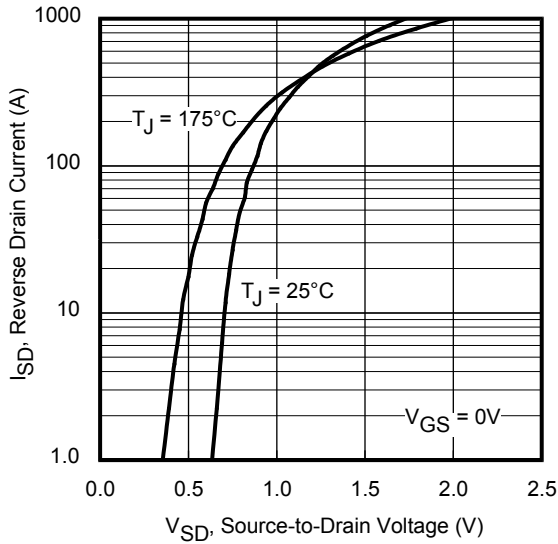
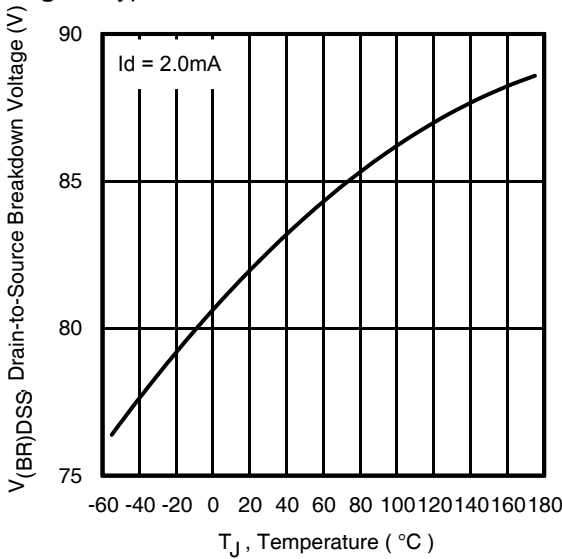
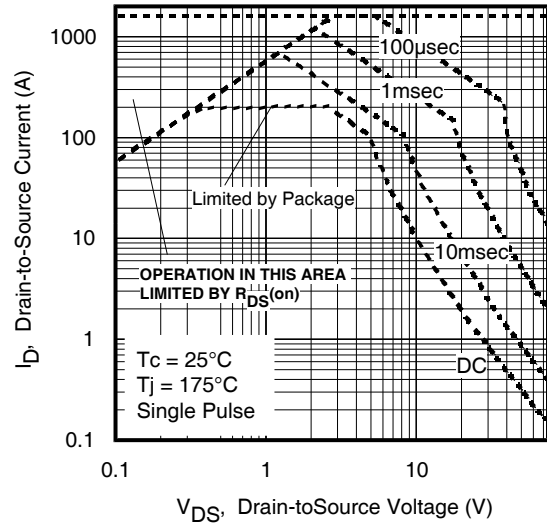
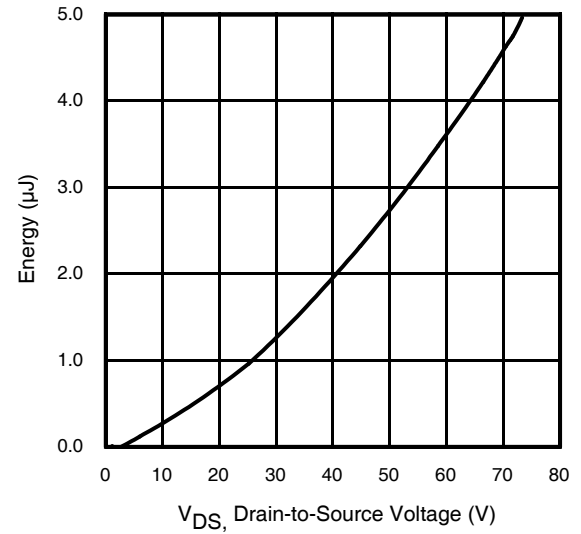
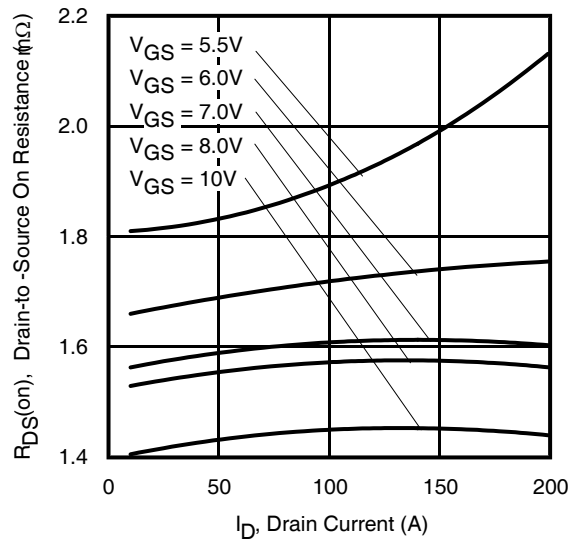
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

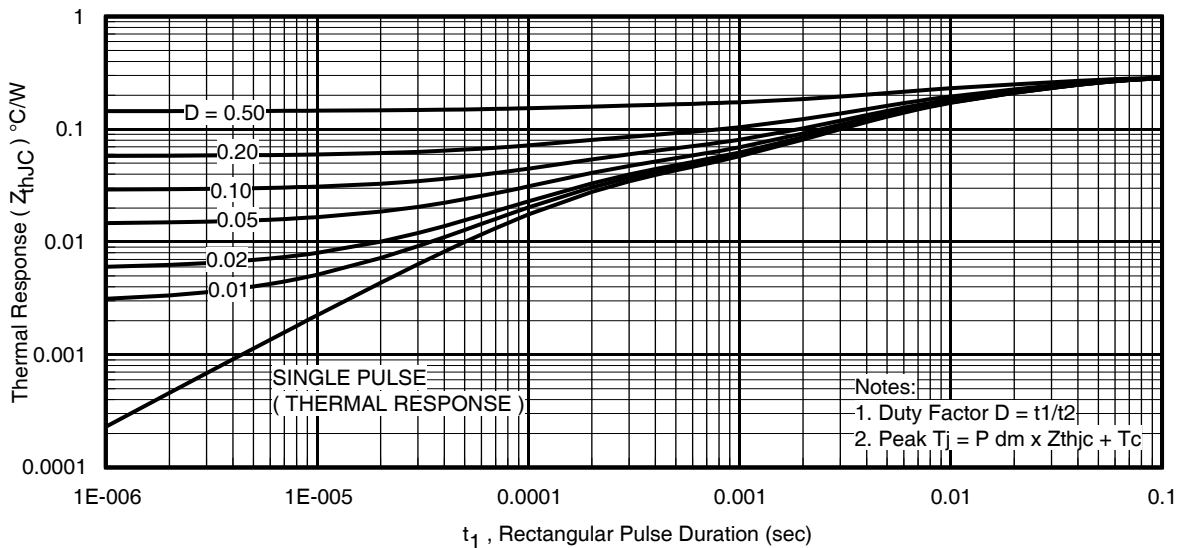
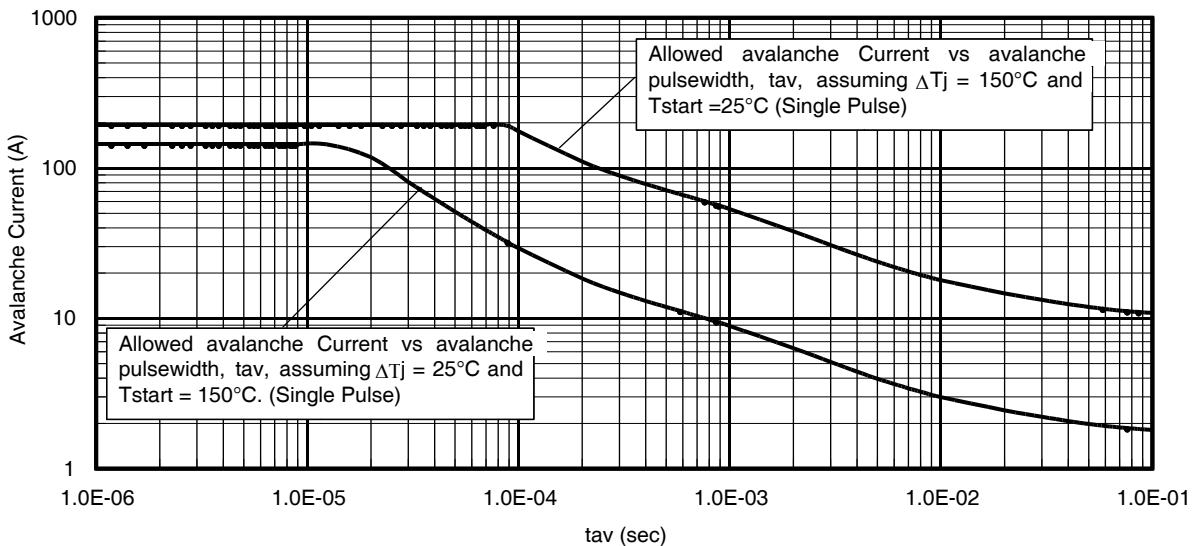
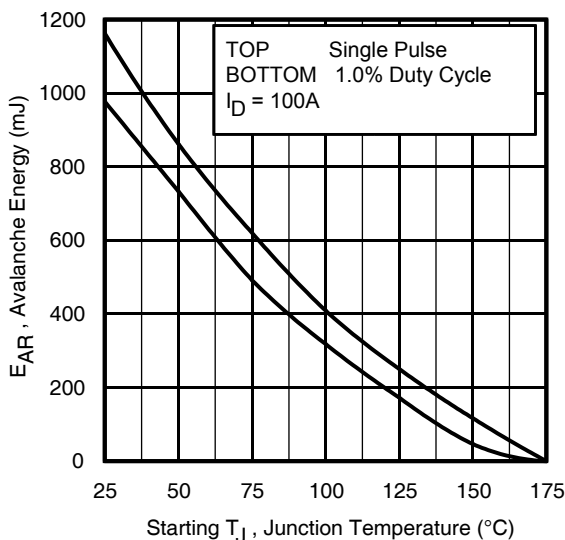
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	420	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 100A
Q <sub>g</sub>	Total Gate Charge	—	552	830	nC	I <sub>D</sub> = 100A V <sub>DS</sub> = 38V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	119	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	168	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	384	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	58	—	ns	V <sub>DD</sub> = 38V I <sub>D</sub> = 100A R <sub>G</sub> = 2.6Ω V <sub>GS</sub> = 10V <sup>⑤</sup>
t <sub>r</sub>	Rise Time	—	164	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	266	—		
t <sub>f</sub>	Fall Time	—	160	—		
C <sub>iss</sub>	Input Capacitance	—	29550	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 100KHz, See Fig.7 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑦</sup> V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑧</sup>
C <sub>oss</sub>	Output Capacitance	—	2270	—		
C <sub>riss</sub>	Reverse Transfer Capacitance	—	1395	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	2010	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	2560	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	355 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	1590 <sup>⑩</sup>		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 100A, V <sub>GS</sub> = 0V <sup>⑤</sup>
dv/dt	Peak Diode Recovery dv/dt <sup>④</sup>	—	8.6	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 100A, V <sub>DS</sub> = 75V
t <sub>rr</sub>	Reverse Recovery Time	—	75	—	ns	V <sub>DD</sub> = 64V I <sub>F</sub> = 100A, di/dt = 100A/μs <sup>⑤</sup>
		—	80	—		
Q <sub>rr</sub>	Reverse Recovery Charge	—	208	—	nC	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C
		—	251	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	4.8	—	A	T <sub>J</sub> = 25°C


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

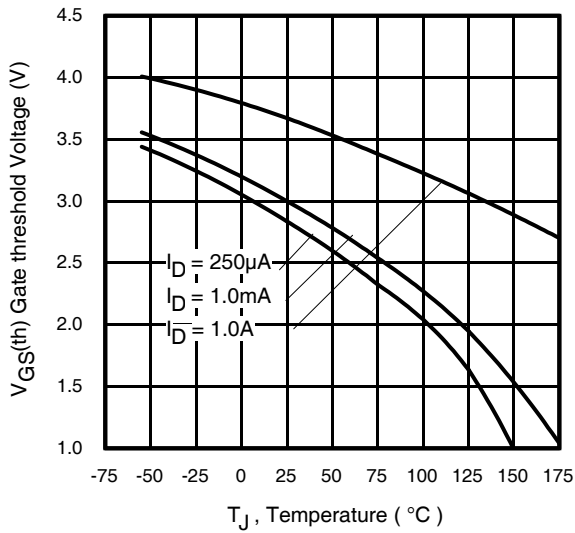


Fig 17. Threshold Voltage vs. Temperature

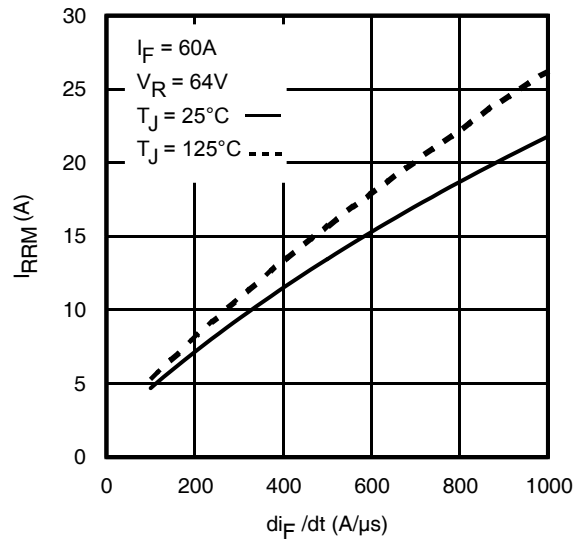


Fig 18. Typical Recovery Current vs. dif/dt

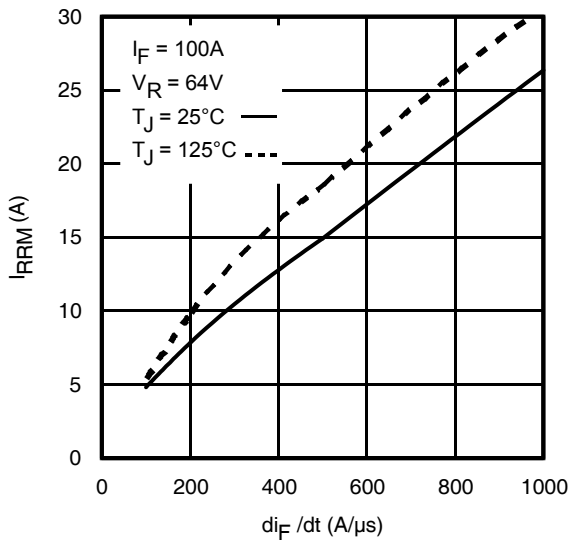


Fig 19. Typical Recovery Current vs. dif/dt

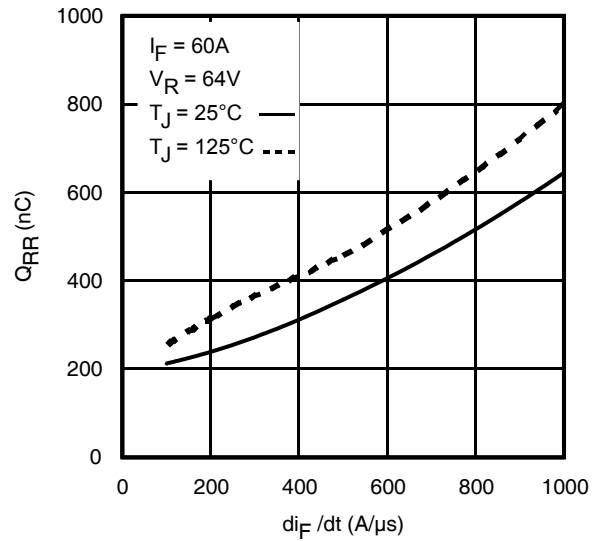


Fig 20. Typical Stored Charge vs. dif/dt

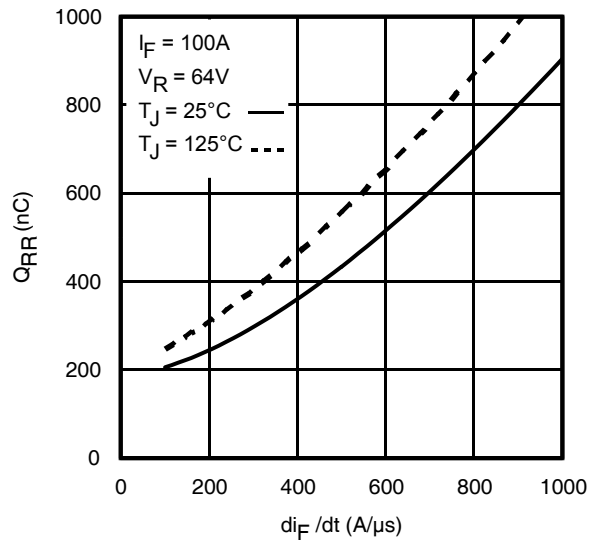
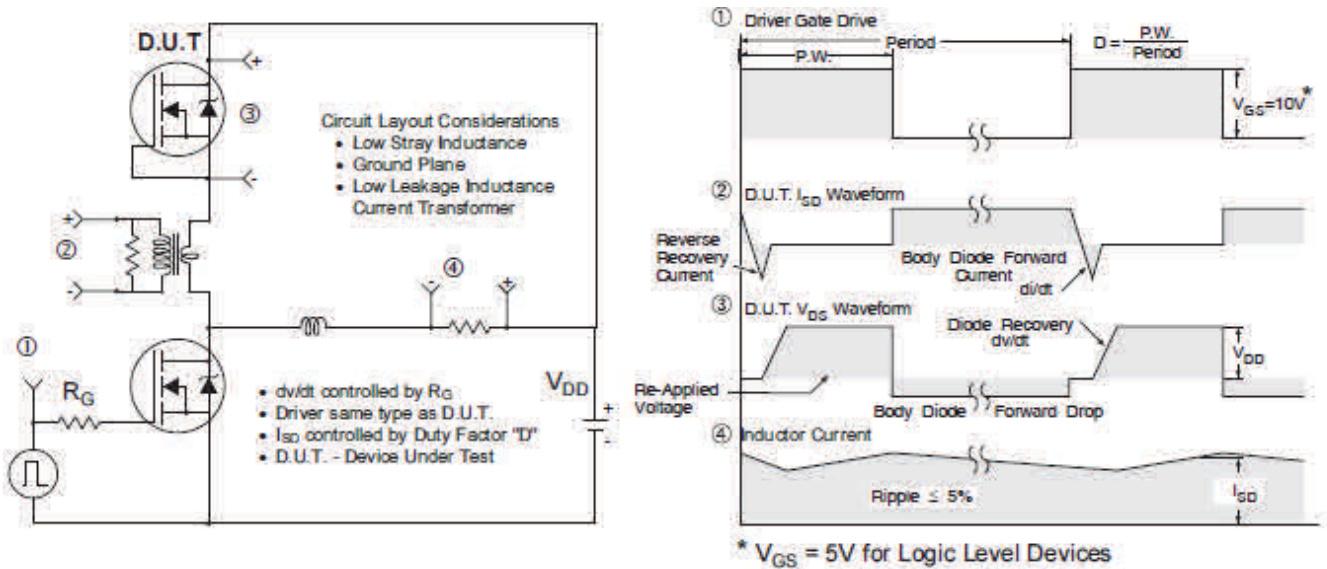
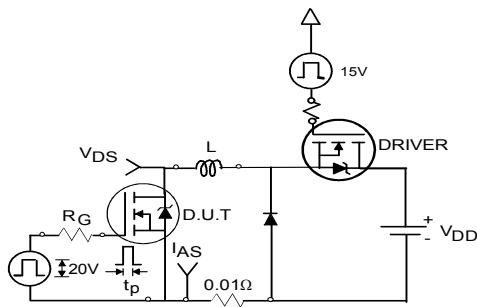


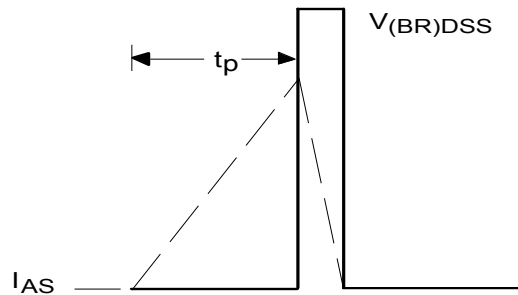
Fig 21. Typical Stored Charge vs. dif/dt



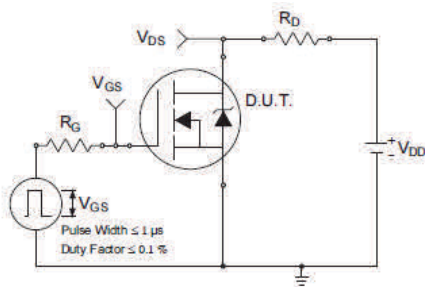
**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



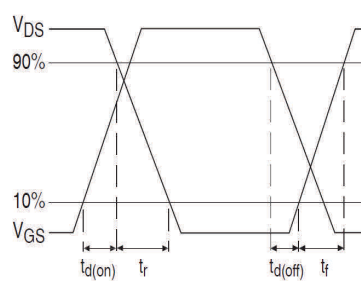
**Fig 23a.** Unclamped Inductive Test Circuit



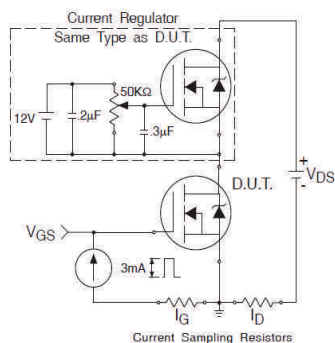
**Fig 23b.** Unclamped Inductive Waveforms



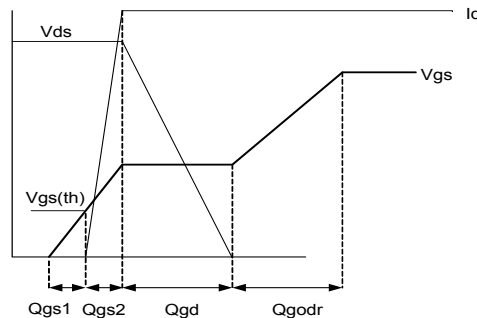
**Fig 24a.** Switching Time Test Circuit



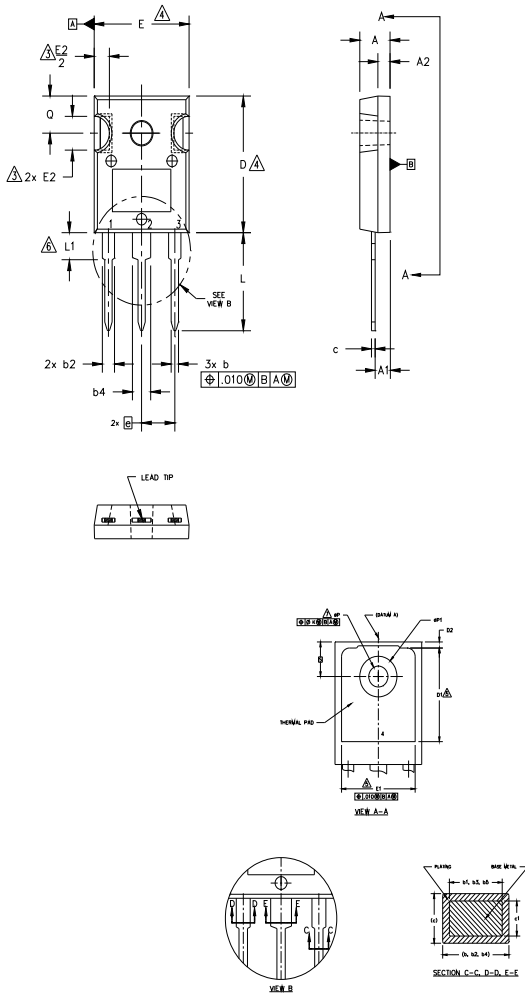
**Fig 24b.** Switching Time Waveforms



**Fig 25a.** Gate Charge Test Circuit



**Fig 25b.** Gate Charge Waveform

**TO-247AC Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
$\phi P1$	.140	.144	3.56	3.66	
Q	-	.291	-	7.39	
S	.209	.224	5.31	5.69	
	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**DIODES**

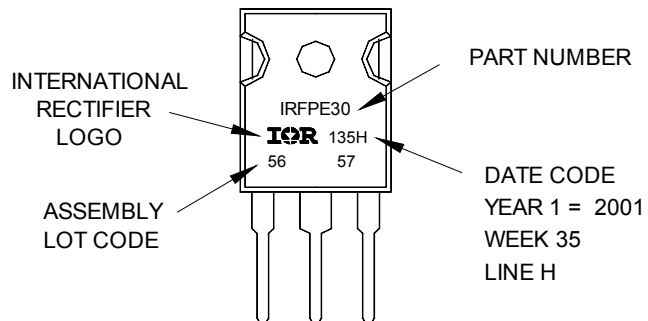
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

**TO-247AC Part Marking Information**

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information†**

<b>Qualification Level</b>	Industrial	
<b>Moisture Sensitivity Level</b>	TO-247AC	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

<b>Date</b>	<b>Comments</b>
02/19/2015	<ul style="list-style-type: none"> <li>Updated <math>E_{AS (L=1mH)} = 2004mJ</math> on page 2</li> <li>Updated note 9 "Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 63A</math>, <math>V_{GS} = 10V</math>" on page 2</li> </ul>
11/30/2015	<ul style="list-style-type: none"> <li>Corrected fig 4 label typo from "25°C" to "175°C" on page 4.</li> <li>Updated datasheet with corporate template</li> </ul>

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