PSB 21150, PEB 3086, PEB 3186 and PEB 3081

IPAC-X, ISAC-SX, ISAC-SX TE and SBCX-X

Migration to New Generation S-Transceivers

Wired Communications

Infineon technologies

Never stop thinking.

Preliminary

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Table of Contents

List of Figures

Preliminary

Abstract

This Application Note describes how to use the new generation S-Transceivers from Infineon Technologies. It describes mostly the differences between the previous 5V generation and the new 3,3 V generation. This application note does not cover all items. It is meant as help, but is not as a complete delta sheet.

The main feature of these new chips compared to the current S-Transceivers like ISAC-S and IPAC is that they operate from a single 3.3 V power supply. Nevertheless, lots of other features have been included which allow much more flexible solutions than before (e.g. an additional serial data strobe output (SDS) for simplified connection of a codec/ ASIC, buffered clock output, enhanced switching functionality etc).

This document will focus on the migration from existing IPAC designs (PSB 2115) to IPAC-X designs (PSB 21150). However, since all three transceivers are very similar, this document is also useable to transfer ISAC-S to ISAC-SX designs and describes the SBCX-X as well. The major differences between the four chips (SBCX-X, ISAC-SX, ISAC-SX TE and IPAC-X) lie in the number of HDLC controllers and the supported modes. For details, please refer to the data sheets.

All new S-Transceiver devices use the same register settings for operation and eases modular applications therefore (register compatible). The IPAC-X and ISAC-SX are pin-compatible and register compatible.

Table 1 All previous S-Transceivers have successors

Previous S-Transceivers (5V)		New SX-Transceivers (3,3V)	
IPAC	PSB 2115	IPAC-X	PSB 21150
ISAC-S	PEB 2086	ISAC-SX	PEB 3086
ISAC-S TE	PEB 2186	ISAC-SX TE	PEB 3186
SBCX	PEB 2081	SBCX-X	PEB 3081

Table 2 Packages Overview

Previous S-Transceivers (5V)		New SX-Transceivers (3,3V)	
IPAC	P-MQFP-64 P-TQFP-64	IPAC-X	P-MQFP-64 P-TQFP-64
ISAC-S	P-MQFP-64 P-LCC-44	ISAC-SX	P-MQFP-64 P-TQFP-64
ISAC-S TE	P-MQFP-64 P-LCC-44	ISAC-SX TE	P-MQFP-64 P-TQFP-64
SBCX	P-LCC 28 P-DIP 28	SBCX-X	P-MQFP-44 P-TQFP-48

1 Host Interface

If the parallel host interface of the IPAC-X is used, no special differences to the IPAC have to be taken care of. It should be pointed out that the interface is 5 V tolerant, i.e. it can be driven from a 5 V microcontroller or similar devices.

To select the type of the bus interface (Motorola or Siemens/Intel multiplexed or demultiplexed), the ALE pin is used as known from the IPAC (please refer to the IPAC-X PSB21150 Data Sheet). The interface is configured during hardware reset of the chip as described in the data sheet.

To select the serial interface, the $\overline{WR}$, $\overline{RD}$ and ALE pins have to be pulled to Vss during reset whereas $\overline{CS}$ has to be pulled to Vdd. Note that it is also possible to use the chip without any host interface (in that case it is fully controlled via the IOM-2 interface).

Table 3 Host Interfaces in Comparison (only the changes are shown)

Previous S-Transceivers		New SX-Transceivers	
IPAC	• No serial (SCI) interface • DMA interface	IPAC-X	• Additional serial (SCI) interface • No DMA interface
ISAC-S	• No serial (SCI) interface	ISAC-SX	• Additional serial (SCI) interface
ISAC-S TE	• No serial (SCI) interface	ISAC-SX TE	• Additional serial (SCI) interface
SBCX	• Controlled by monitor-channel/CI-Channel only • no microcontroller interface	SBCX-X	• Serial (SCI) interface • Controlled by monitor-channel/CI-Channel also.

Note, that the new SBCX-X provides a SCI microcontroller interface now, allowing direct access to all registers. The hardware designer is not forced to use the IOM-interface with monitor channel programming any more (but can still be used, if wanted).

1.1 IPAC - DMA Transfer

The DMA feature which has been a part of the old IPAC host interface (pins DRQx and $\overline{DACK}$x) is no longer available with the IPAC-X chip. If a design uses that DMA feature, it has to be changed to use non-DMA transfer.

2 Flexible IOM-Handler instead of PCM Interface

The PCM interface of the IPAC is no longer available with the IPAC-X. However, the IOM-2 interface of the IPAC-X can be configured to act as a pure PCM interface (the chip is then controlled via the host interface). To enable this feature, the monitor handler, the C/I handler and the TIC-bus handler can be disabled (i.e. they are not connected to the IOM-2 interface or at least not influenced, please refer also to **Chapter 4**). Please refer to the detailed register description of the MON_CR and IOM_CR registers in the IPAC-X PSB21150 Data Sheet.

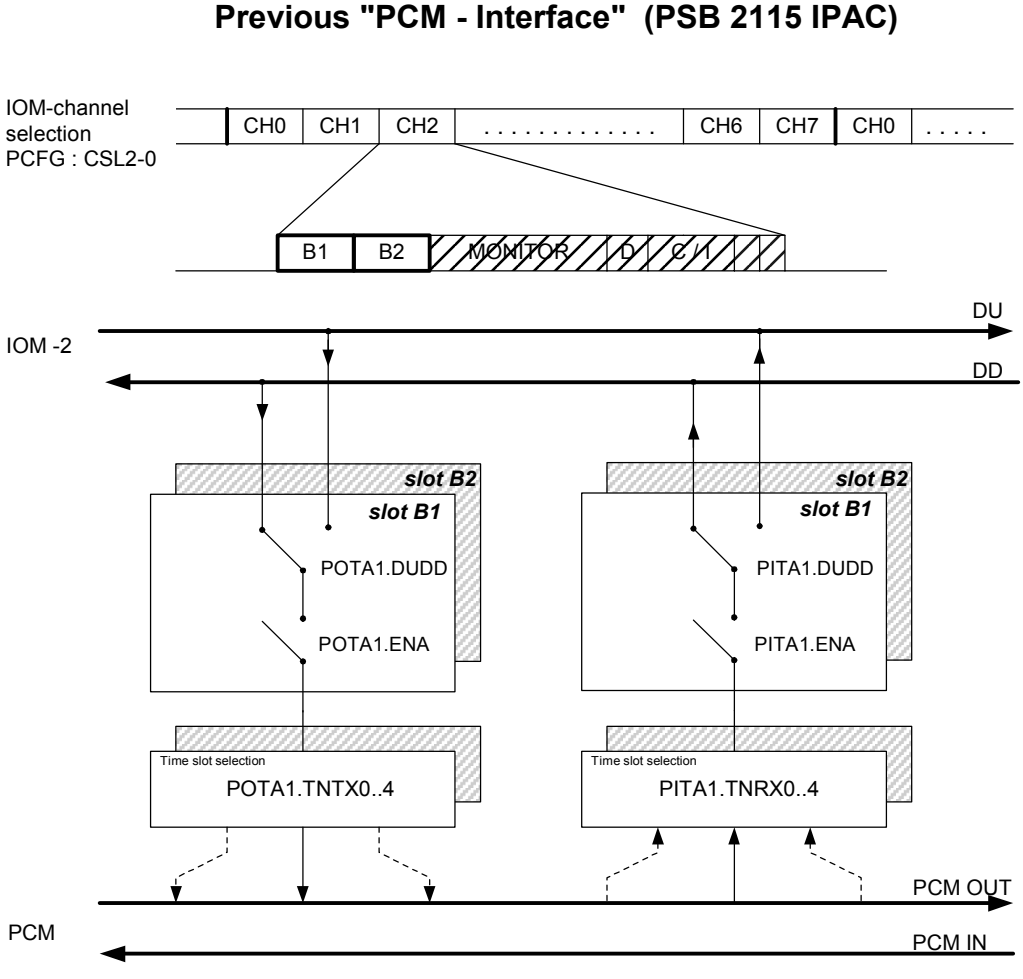

Figure 1 The previous PCM interface of IPAC can handle B-channels only

The new S-Transceivers are much more flexible compared to the previous generation. It is possible to assign every time slot (0...31) to the SX-Transceiver for each B-channel seperately. In front of the DU/DD pins a IOM-Handler with integrated CDA Handler

(Controller Data Access) can be used for shifting, looping, monitoring and even switching. The figure below shows some examples, only.

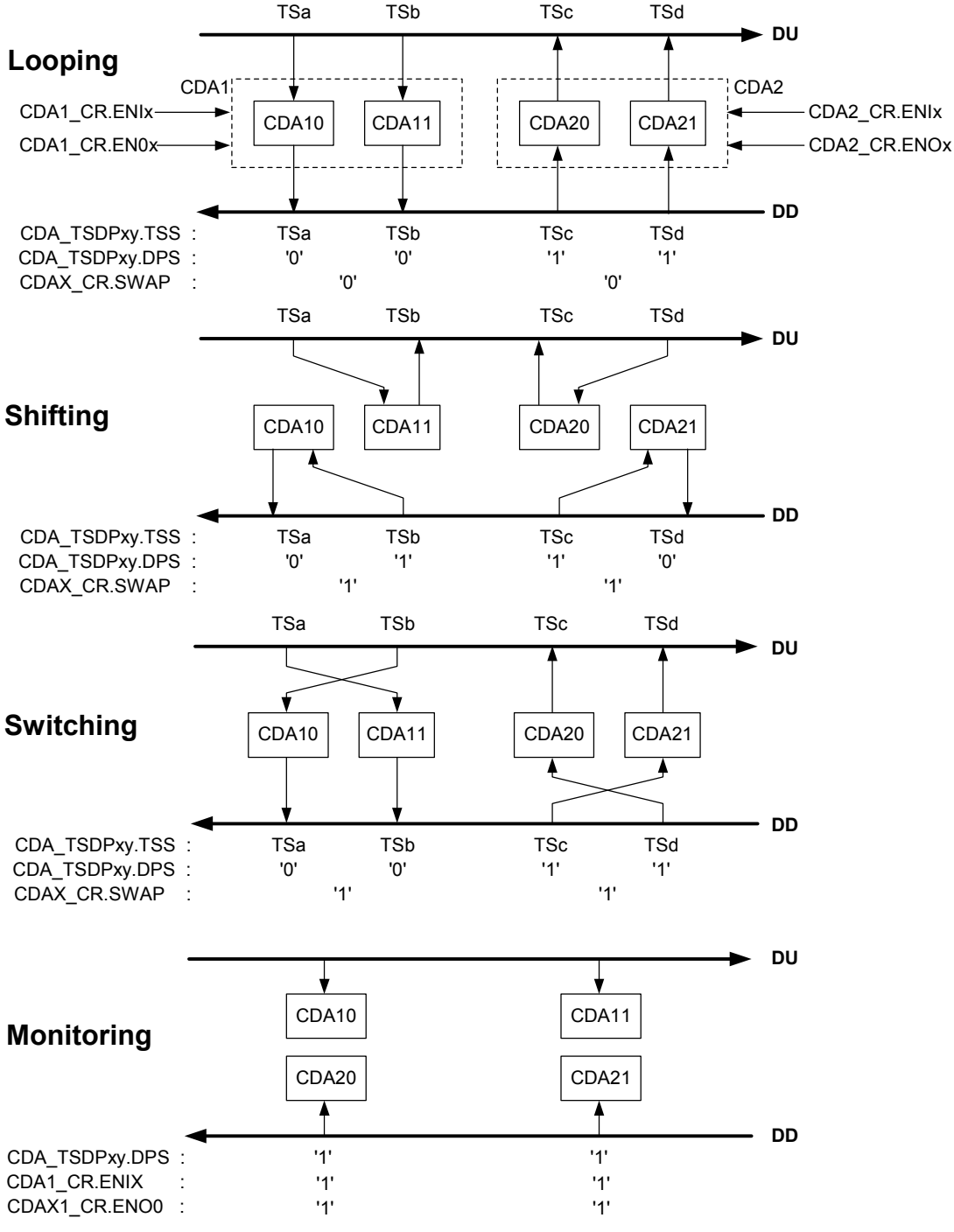

Figure 2 The CDA Handler of the new SX transceiver generation

This CDA handler is provided in all new S-transceivers as SBCX-X, ISAC-SX TE, ISAC-SX and IPAC-X.

2.1 Controller Data Access / Timeslot Assigner

The four CDA registers (CDA10..CDA21) can be seen as a "1-byte FIFO". They may be used to access data at a given timeslot.

The time slot selection is done in the CDA_TSDPxy registers (xy = [10, 11, 20, 21]). Bit7 of these registers allows to receive data on DU and send data on DD or vice versa.

Table 4 Data processing - Comparison

Chip	Related registers
IPAC PSB 2115, ISAC-S PEB 2086	SPCR, C1R, C2R, B1CR, B2CR
IPAC-X PSB 21150, ISAC-SX PEB 3086, SBCX-X PEB 3081	CDAx_CR, CDAx, CDA_TSDPxy

In the CDAx_CR registers the inputs and outputs of the CDAxy registers are enabled.

Examples:

Looping B1, B2 on IOM-2 bus (TE mode): Default register setting & CDA2_CR=0x1E

Looping B1, B2 on IOM-2 bus (NT mode): Default register setting & CDA1_CR=0x1E

Monitoring B1, B2 at DU and B1, B2 at DD: Default register setting & CDA1_CR=0x18 & CDA2_CR=0x18

Switch B1, B2 (DU->DD): Default register setting & CDA1_CR=0x1F

Note: Also a CDA handler configurator (CDA.EXE) is available together with the SMART-packages of the IPAC-X family. This program is implemented in WinEasy, but can run also in a stand alone configuration (without SMART board and without WinEasy). It runs on Win95, Win98, WinNT.

Special case: TIC-bus monitoring (TS11 on DU/DD)

Please note that the CDA registers can be used to access also the TIC-Bus (normally slot 11, i.e. the last octet of the third IOM channel). The time slot 11 CDA access needs to set the CDAx_CR.EN_TBM bit before. The TIC bus time slot can be read or written, if CDA_TSDPx0.TSS = 0x08/0x88.

The TIC bus arbitration can be switched off completely (IOM_CR.TIC_DIS). In this case the TS11 can be used for multi purposes.

3 Clocks, Data Strobes, Reset and Auxiliary Interface

3.1 Serial Data strobe interface (SDS)

An additional feature of the new S-Transceiver generation is a second serial strobe signal which is free programmable. This allows simple connection of external devices like codecs which need a strobe signal to access a certain timeslot of the serial highway. Please refer to the description of the SDS1 and SDS2 pins.

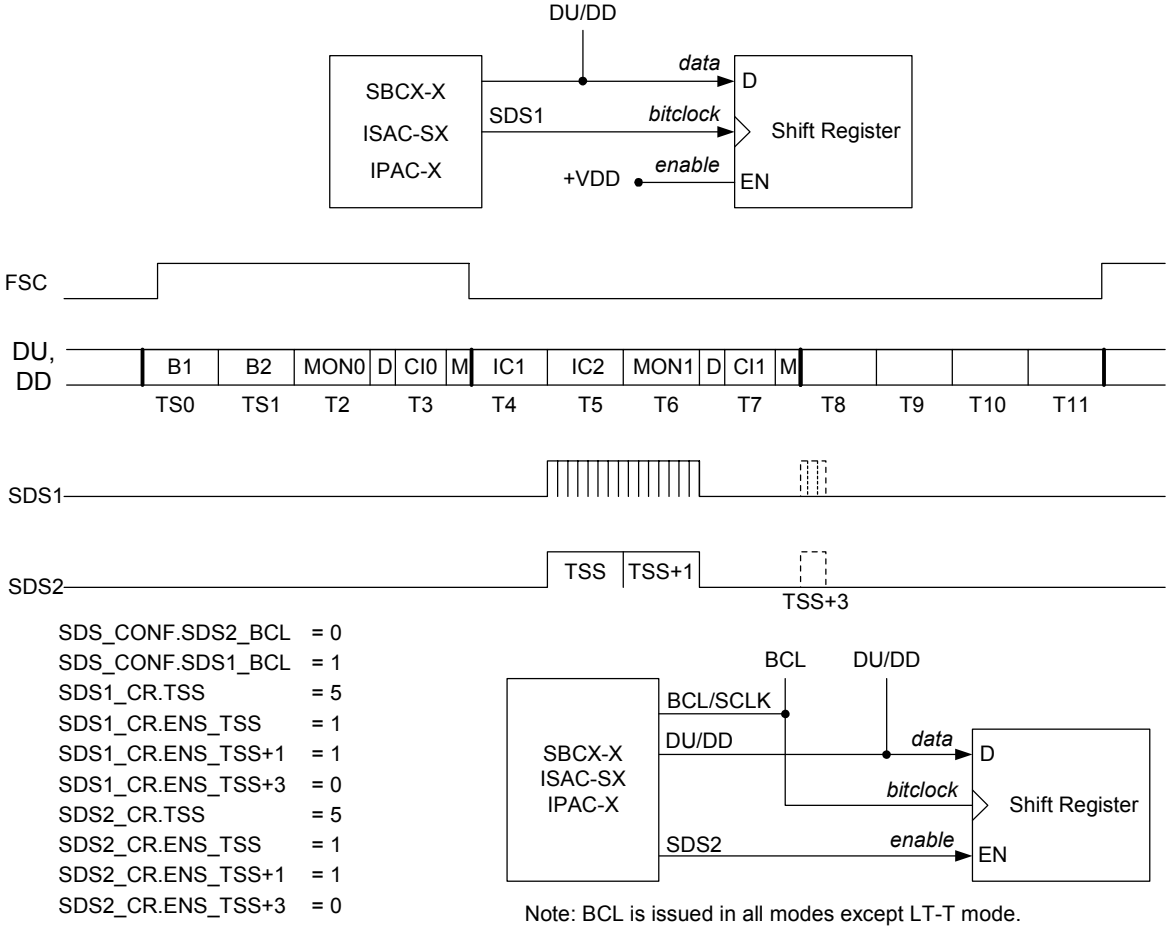

Figure 3 Using one or both SDS outputs for simple adaptations

Both pins, SDS1 and SDS2, can handle strobed bit BCL or active high signal.

Chip	Related register
IPAC PSB 2115, ISAC-S PEB2086	ADF2.D1C0..D1C2
IPAC-X PSB 21150 (family)	SDS_CONF, SDSx_CR

Note: The ISAC-SX TE version provides only one SDS pin.

3.2 New: SDS1 strobe signal on DU/DD line

A new feature is also the SDS1 strobe signal, which can affect the IOM-2 interface. It controls the IOM-2 interface in the way, that data on the internal IOM-Bus can be filtered out, as the IOM-2 interace is switched in high-impedance mode for the appropriated time slots, only. The filtered out data on this timeslots are internally still valid, but on the external IOM-2 interface this data is not available.

It can be programed as descripted above and additionally SDS_CONF.DIOM_SDS has to be set.

For example, the transceiver output data on B1 and B2 at the DD-line is not wanted on the external IOM-2 interface (DD-line). Therefore the DIOM_SDS is set and the SDS1_CR register is programmed to the B1 and B2 location.

Note: The filter-out mechanism can be inverted (is always active, but not at the programmed SDS1 timeslots) with the DIOM_INV bit.

3.3 Buffered crystal clock (C768)

Together with the new S-transceivers also the C768 pin is available. This pin is the buffered quartz crystal output clock. It allows to save crystals in multline applications as shown below:

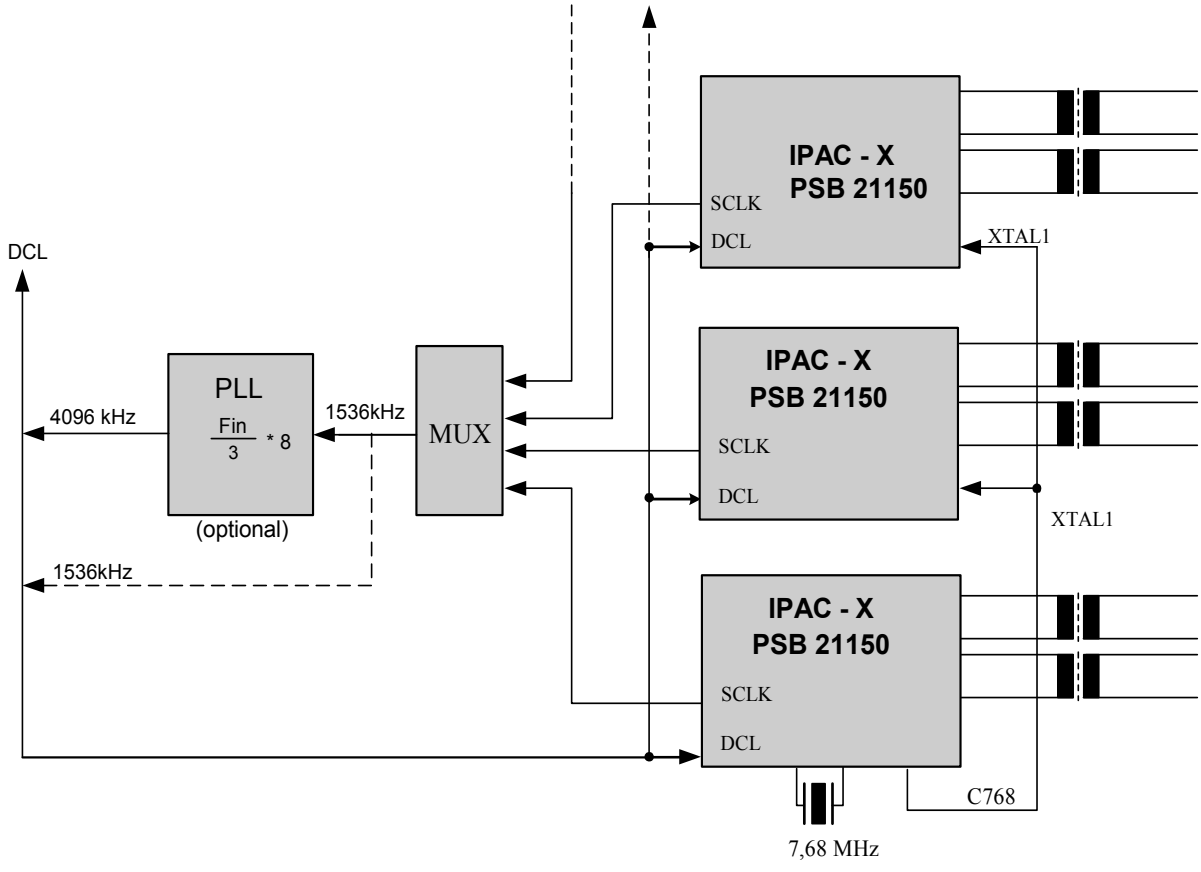

Figure 4 Saving crystals by using the C768 pin (e.g. PBX application)

It is recommend to use the C768 in star configuration, to avoid accumulating propagation delay times. The C768 output driver is strong enough to drive the input capacitances very fast.

It is also possible to use a daisy chain configuration, but please take care that the duty cycle of the last (far end) XTAL input is according to the data sheet for XTAL1 input. This is also the criterium for the star configuration.

3.4 Using clock generators instead of a crystal

In many applications it is possible to save crystals. Often U-Transceiver with 15.360 MHz crystal is used together with the S-Transceivers, that would need an additional 7,68 MHz XTAL input frequency. Therefore it is often decided to use one crystal based clock generator and deriving the needed clocks from it.

The new S-Transceiver family allows you to connect a permanent clocking generator to the XTAL1 input. This is possible even if the 'G1/F3 Deactivated' state is reached and the MODE1.CFS-bit is set. Usually the S-Transceiver switches off the XTAL oscillator in order to save power in this state.

The new S-Transceivers switch off the XTAL input path to the internal clock tree additionally (refer to the figure below).

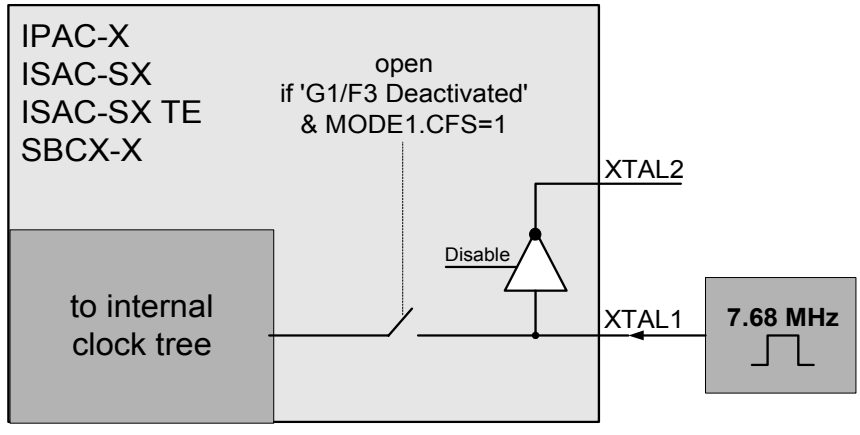

Figure 5 Block diagram of the principle

3.5 Auxiliary Interface

The auxiliary interface is similar to the one of the IPAC, please refer to the IPAC-X PSB21150 Data Sheet for details. Note that the AUX0..AUX2 pins are used to select timeslots in certain modes (same mechanism as used with the old IPAC).

The LED outputs are available with the IPAC-X as well. Interrupts (from external devices) can be routed via $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ pins (they have to be configured as inputs).

3.6 Reset ($\overline{\text{RES}}$ and $\overline{\text{RSTO}}$)

3.6.1 Reset input

The reset pin has been changed compared to most of the previous S-transceivers. Additionally a seperate $\overline{\text{RSTO}}$ pin is available now. Via register setting (SRES) different reset sources can be selected and the $\overline{\text{RSTO}}$ pin can be activated. All members of the new S-transceiver generation provide the $\overline{\text{RSTO}}$ pin.

Table 5 Reset input pin behaviour

Previous S-Transceivers		**New SX-Transceivers**	
IPAC	active HIGH	IPAC-X	**active LOW**
ISAC-S	active HIGH	ISAC-SX	**active LOW**
ISAC-S TE	active HIGH	ISAC-SX TE	**active LOW**
SBCX	active LOW	SBCX-X	active LOW

Furthermore, if the AUX7 pin is used to output the state of the Stop/Go bit, the polarity and pulse length of this output can be defined with two bits.

3.6.2 Reset Source Selection

With previous S-Transceivers the reset source selection was done with the CIX0.RSS bit. It was possible to select between two possibilities:

a) EAW interrupt or C/I Code change

b) Watchdog timer

The new S-Transceiver generation provides two bits RSS0 and RSS1 for selection.

Chip	**Related register**
IPAC PSB 2115, ISAC-S PEB 2086	CIX0.RSS
IPAC-X PSB 21150 (family)	MODE1.RSS0/1

It is possible to disable the reset sources now in order to avoid reset generation.

4 IOM-2 Interface & Internal Structure

All internal units, like D-Channel HDLC controller, B-channel HDLC controller, CI-Handler and the S-Transceiver are connected to the internal IOM-Bus.

New are the CDA1-and CDA2 handler - two autonomous units also connected to the internal IOM-bus.

In some applications it is necessary to disable some units temporarily. Refer to the figure below:

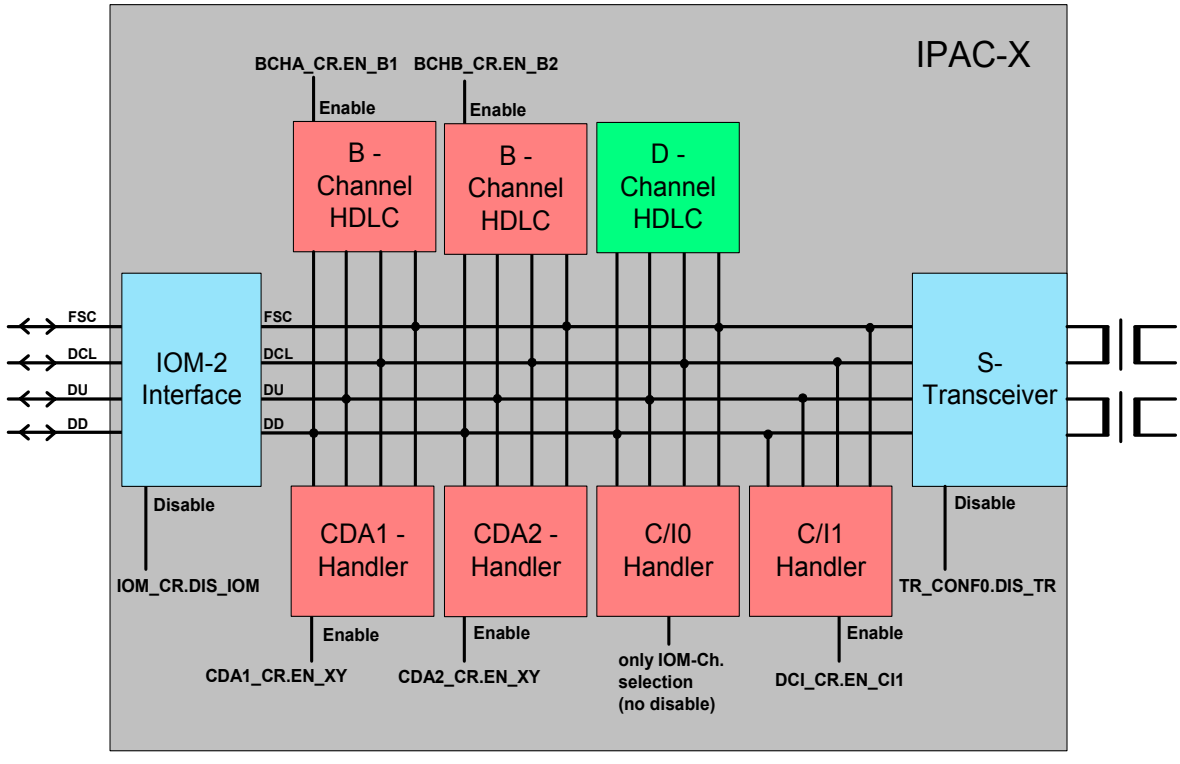

Figure 6 Internal units are connected to the internal IOM-bus

Internal units can be disabled. Both B-HDLC controllers can be disabled (has no more any effect on the IOM-bus).

Also the CI1-Handler can be disabled, the CI0-Handler can not be disabled, but can be programmed to a different timeslot. If the CI0-Handler is programmed to a timeslot TS>11 in TE mode, it is quasi-disabled, because this timeslot cannot be reached.

4.1 Disabling the IOM-Interface

The IOM-2 interface is handled by the IOM-Handler. This allows to seperate the external IOM-2 bus from the internal bus (IOM_CR.DIS_IOM bit).

Table 6 Disable IOM-Interface

Chip	Related bits
IPAC PSB 2115, ISAC-S PEB 2086	ADF1.IOF
IPAC-X PSB 21150, ISAC-SX PEB 3086, SBCX-X PEB 3081	IOM_CR.DIS_IOM

If the IOM-Interface is disabled, the DU/DD lines are switched to high impedant mode and the DCL and FSC clock pins are switched to input.

Note: There is one restriction: If the MODE1.CFS bit is set in order to switch off the XTAL in 'F3 Deactivated' or 'G4 Pending Deactivation' mode, the DU line would float, because the DU/DD lines are switched into input mode automatically. The DU line is also used to wake up the transceiver (refer to the SPU bit). If the DU line is tied to low the XTAL is switched on. In this case it is necessary to use a pullup resistor at the DU line at least (the DU-induced wakeup bypasses the multiplexer in the IOM-handler).

4.2 Special case: Disabling the S-Transceiver

In rare cases it is necessary to switch off the transceiver completely or only temporarily. This is possible with the TR_CONF0.DIS_TR bit.

If the transceiver was in TE mode before, the internal FSC-and DCL clock generation is switched off and automatically the FSC-pin and DCL-pin is switched to a high impedant input. The internal HDLC controllers and CI-Handler can work if they are supplied with DCL and FSC clocks from external.

Once disabled a software reset (SRES.RES_TR) is necessary to reactivate the S-Transceiver. The whole transceiver related registers are also reset herewith.

Table 7 Disable S-Transceiver

Chip	Related bits
IPAC PSB 2115	CONF.TEM
IPAC-X PSB 21150	TR_CONF0.DIS_TR
ISAC-SX PEB 3086	TR_CONF0.DIS_TR
SBCX-X PEB 3081	TR_CONF0.DIS_TR

Note: If the S-Transceiver is switched off, the whole transceiver unit is without clocks. This means, the XTAL is not running and also the level detector does not work. Commands to the transceiver related registers have no effect.

4.3 Push/Pull IOM-2 output driver

The IOM-interface use open drain outputs by default. Therefore two external pullup resistors at DU and DD are necessary. In some applications (single chip application, like PC cards) the IOM-2 bus isn't used.

It is possible to save these two pullup resistors because the IOM-Interface can be switched to push pull output driver mode. This means, always if an internal unit writes to the IOM-bus (DU or DD line) the output driver goes active. During all other time slots the

IOM-interface is dynamical switched to input. This allows to input data in time slots that are not allocated by internal units.

Table 8 Push/Pull output driver mode

Chip	Related bits
IPAC PSB 2115, ISAC-S PEB 2086	ADF2.ODS
IPAC-X PSB 21150, ISAC-SX PEB 3086, SBCX-X PEB 3081	IOM_CR.DIS_OD

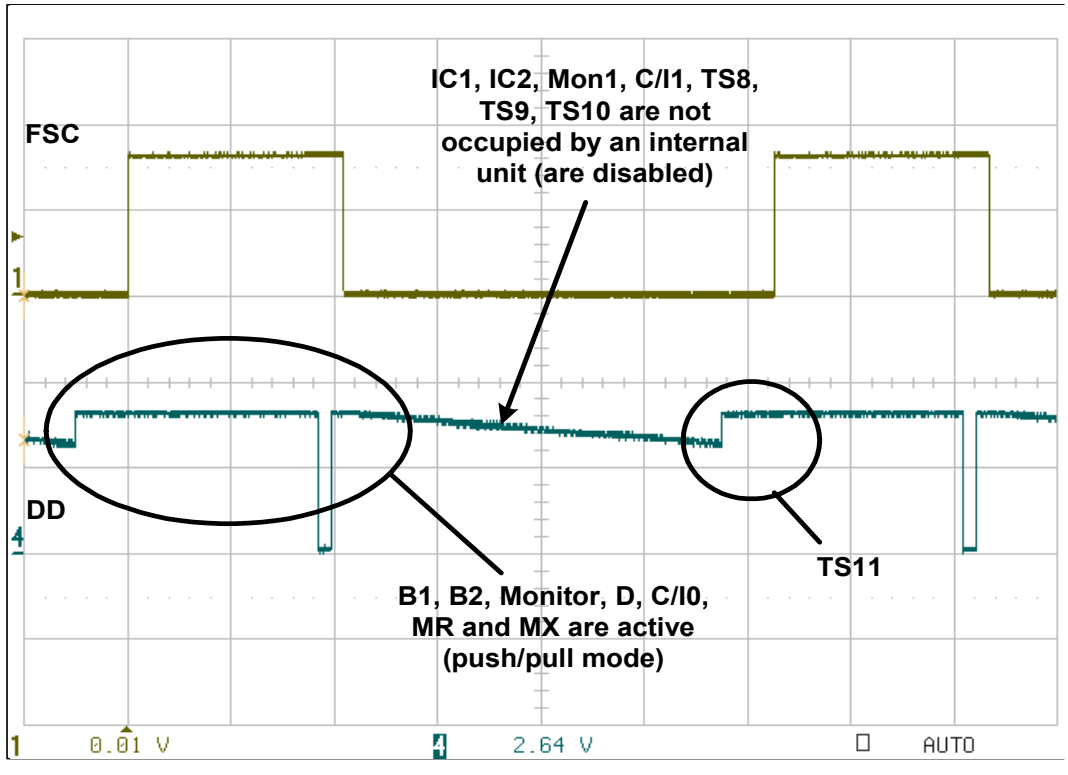

Figure 7 IOM-2 bus in TE mode (push/pull mode without ext. resistors)

The time between two active driving units (e.g. C/I0-time slot and TS11 on IOM-2 bus) the IOM-2 interface (DU and DD pin) is high impedant. This non-occupied time slots could be monitored with the CDA registers for example.

4.4 IDP0, IDP1 and DU, DD

All new S-transceivers use the DU/DD pins, not the IDP0/IDP1 declaration. DU means data upstream (transceiver transport direction) and says nothing about the input/output behaviour of this pins. Both DU and DD are bidirectional lines !

Table 9 Transceiver Data Flow

	TE / LT-T		NT/ LT-S	
Transceiver data on IOM-2..	**goes to Transceiver**	**comes from Transceiver**	**goes to Transceiver**	**comes from Transceiver**
IPAC PSB 2115	DU	DD	DD	DU
IPAC-X PSB 21150	DU	DD	DD	DU
ISAC-SX PEB 3086	DU	DD	DD	DU
SBCX-X PEB 3081	DU	DD	DD	DU

	LT-T		TE / NT / LT-S	
Transceiver data on IOM-2..	**goes to Transceiver**	**comes from Transceiver**	**goes to Transceiver**	**comes from Transceiver**
ISAC-S PEB 2086	IDP0	IDP1	IDP1	IDP0
SBCX PEB 2081	IDP0	IDP1	IDP1	IDP0

Note: The new S-Transceiver allows to select the DD or DU line for data output for almost all internal units seperately.

5 HDLC Controller

5.1 HDLC buffer sizes

The HDLC controllers are similar to the old IPAC, though more flexible. They are organized as cyclic buffers with a size of 64 bytes for the D channel controller and 128 bytes for the B channel controllers. The threshold of these buffers can be programmed using the RFBS bits in the EXMB and EXMD1 registers. To be fully compatible to the old IPAC, these bits can be programmed to a threshold of 64 bytes for the B channels (i.e. EXMB.RFBS = 00) and to a threshold of 32 bytes for the D channel controller (i.e. EXMD1.RFBS = 00). Note that these bits only define the threshold in receive direction. For the transmit direction, the XFBS bits in both registers define the blocksize of the FIFO, they can also be programmed to 0 to be compatible to the old IPAC. All these values are default settings, so in most applications, no reprogramming of these bits should be necessary.

5.2 HDLC Receive and transmit mechanism

The receive mechanism is the same as with the old IPAC. When the FIFO has been filled to the threshold, an RPF (Receive Pool Full) interrupt or an RME (Receive Message End) interrupt is generated. The host then reads the data and acknowledges via the RMC command.

The transmit mechanism is also identical to the old IPAC, using XPR/XMR interrupts and XTF/XME/XRES commands. Please refer to the IPAC-X PSB21150 Data Sheet.

Special care should be taken with the XDU interrupt.

Note: If XDU occurs, the transmit FIFO is locked until this interrupt has been read by the host. The interrupt cannot be read if it has been masked in MASKD/MASKB.

Note: It is necessary to enable the MASKB.RPF and MASKB.RFO interrupts! If these two bits are masked, the internal HDLC controller functionality may be affected (hangs in extended transparent mode, if only XTF is used to send).

If an application has to react very fast to incoming data, the receive FIFO threshold may be lowered to a minimum of 8 bytes. Note that the receive threshold can be adapted dynamically since it is re-set with every RMC command based on the current value of the RFBS bits.

It should be noted that the B channel controller FIFOs occupy only **one** byte in the address space. IPAC-X B-channel controller makes an autoincrement internally to fill the buffer. This must be checked carefully when existing software uses a loop to write blocks into the B channel FIFOs (writing 16 bytes to consecutive locations in the IPAC-X would overwrite 15 registers).

The D channel controller still uses 32 bytes address room (as known from the old IPAC). What ever address inside the 32 byte block is selected an internal pointer is selected auto incrementing the D channel buffer (no random access prossbile).

The TR_TSDP_BC1 and TR_TSDP_BC2, allows to connect the B1 and B2 channels **of the S_0-interface** to an arbitrary timeslot of the IOM-2 interface.

*Note: These register names refer to the "physical" B1 and B2 channels, however, they **do not necessarily** map the B1- and B2-channels to the so-called B1 and B2 channels of the IOM-interface !*

5.3 Swap the HDLC input/outputs

Also the HDLC controller (D and B channel) can swap the input/output directions. By default all HDLC controller outputs data to the DU line and takes data from the DD line.

Please refer to the table below for the related bits.

Table 10 Swap the HDLC inputs/outputs

Chip	D-HDLC	B-HDLC
IPAC PSB 2115	SPCR.SDL	CCR2.SOC
IPAC-X PSB 21150	Depends on ISDN mode	BCHx_TSDP_BC1.DPS
ISAC-SX PEB 3086	Depends on ISDN mode	BCHx_TSDP_BC1.DPS
SBCX-X PEB 3081	Depends on ISDN mode	BCHx_TSDP_BC1.DPS

IPAC-X, ISAC-SX and SBCX-X : D-HDLC input/output

Chip	LT-S / NT	TE / LT-T / iNT
IPAC-X PSB 21150	Output on DD, Input on DU	Output on DU, Input on DD
ISAC-SX PEB 3086	Output on DD, Input on DU	Output on DU, Input on DD
SBCX-X PEB 3081	Output on DD, Input on DU	Output on DU, Input on DD

5.4 New: IDSL Support

If the HDLC controller is used to access an 8-bit timeslot only, the second 8-bit timeslot and the 2-bit timeslot must be disabled (default value). This is done via the BCHA_CR register by setting the bits EN_D and EN_BC2 to 0. Consequently, to access 16-bit data, EN_BC2 is set to 1. In the case of IDSL, 18-bit wide data access is done by setting all three bits to 1. However, the default values are set to 8-bit access of the B-channel HDLC controller.

The next group, BCHA_TSDP_xx (xx = [BC1, BC2]) allows to connect the HDLC controllers to certain timeslots. Each HDLC controller can access any combination of two 8-bit timeslots and one 2-bit timeslot, i.e. operate on 2, 8, 10, 16 or 18 bits. These three timeslots do not have to be consecutive. The BCHA_TSDP_BC1 register defines the location of the first 8-bit timeslot, BCHA_TSDP_BC2 defines the second 8-bit timeslot. The 2-bit timeslot uses always the D-channel timeslot location, but the IOM-Channel (0..7) can be selected in the BCHA_CR register (bits CS0..2).

The same mechanism is used for the second B-channel controller. The same register set exists, only the names are changed from BCHA_... to BCHB_...

Please refer also to the IPAC-X PSB21150 Data Sheet which includes some figures to help understanding the timeslot assigner, especially chapter ’3.7.1.2 IDSL Support’.

To support IDSL, the D channel controller can be programmed to access the B1, B2 and D-channel as an 18-bit wide time slot. This is done by setting the D_EN_D, D_EN_B1 and D_EN_B2 bits in the DCI_CR register.

*Note: The B1 and B2 channels refer to the B1 and B2 channel timeslots on the IOM-2 interface, i.e. the **first two consecutive 8-bit time slots** in a IOM-2 channel, whereas the IOM-channel (0..7) can be selected. If you reprogram the transceiver timeslots via the TR_TDSP_BCx registers to other locations, they are not accessed via the D-channel controller.*

6 Transceiver

By default, the transceiver is enabled, but the transmitter (the output driver, TR_CONF2.DIS_TX) is disabled. No S-activation is possible, of course, while this bit has not been reset during initialization of the chip.

6.1 Adaptive and fixed timing (Receive PLL)

In TE mode and in point-to-point configuration (long distances) in NT and LT-S mode usually the adaptive timing is used (default value, BUS = 0). In NT/LT-S mode the bus configuration (NT short passive bus) is usual, therefore the bit TR_CONF0.BUS has to be set. The TR_CONF1 register can be used to enable the generation of short FSC signals synchronous to the S multiframes (Multiframe marker).

Table 11 Adaptive / fixed timing

Chip	Related bits
IPAC PSB 2115	MON-8 Configuration (C/W/P)
ISAC-S PEB 2086	SQXR.CFS
SBCX PEB 2081	MON-8 Configuration (C/W/P)
IPAC-X PSB 21150	TR_CONF0.BUS
ISAC-SX PEB 3086	TR_CONF0.BUS
SBCX-X PEB 3081	TR_CONF0.BUS

6.2 New: Fully software controlled state machine (Layer 1 Software State machine)

If the layer-1 statemachine shall be implemented in software, the TR_CONF0.L1SW bit can be set. In this configuration, the registers TR_STA and TR_CMD are used to control the transceiver (i.e. to send the various INFOx signals and get indications on what INFOx signals have been detected by the transceiver). The CIX0 and CIR0 registers has no meaning any more.

Note: It is not necessary to use the software controlled state machine, because by default the hardware state machine is enabled and can be used. Especially applications (proprietary adaptions) could be realized herewith.

The registers TR_STA and TR_CMD are used to program that part of the chip.

6.3 Transceiver operation mode

The transceiver (ISDN) operation mode of the new SX-Transceiver family can be set via pinstrapping. The necessary pins are MODE0, MODE1 selecting the operating mode of the transceiver (TE, LT-T or LT-S). This setting can be overwritten in the TR_MODE register to enable TE, LT-S, LT-T, NT or two different intelligent NT settings.

E.g. for a NT application the LT-S mode is pinstrapped first, the microcontroller overwrites the TR_MODE register afterwards with the bit setting for NT mode.

Table 12 ISDN mode / State machine selection

Chip	Related bits
IPAC PSB 2115	MON-8 Configuration (FSMM) & Pinstrapping only
ISAC-S PEB 2086	Pinstrapping only
SBCX PEB 2081	MON-8 Configuration (FSMM) & Pinstrapping only
IPAC-X PSB 21150	TR_MODE.MODE0..2
ISAC-SX PEB 3086	TR_MODE.MODE0..2
SBCX-X PEB 3081	TR_MODE.MODE0..2

6.4 External Circuitry for S-Interface

The only major difference is the transformer. The old IPAC uses a transformer with a winding ratio of 2:1, the new transceivers need a 1:1 ratio. This is due to the fact that the levels necessary to fulfill the I.430 pulse shape can not be achieved with the old transformers since the chip only has a 3.3 V power supply.

The protection circuitry has to be changed only on the transmit side, the receiver protection circuitry stays the same compared to the IPAC. For details, please refer to the IPAC-X PSB21150 Data Sheet.

In the current data sheet (July 2000), two 8..10 ohms resistors are shown for the transmit side. This might be too high, as this value is transformer related. 5.6 ohms resistors can be used in TE mode to achieve the 750 mV amplitude at the S-bus side. Values below 5R6 ohms should not be used, because the transmitter output impedance would drop below 20 ohms (ETS 300 012 requiry) then.

TR_CONF2 includes also a PDS bit to adjust the phase deviation of the transceiver.

7 C/I Channel Handler (C/I0 & C/I1)

It should be noted that the CIR and CIX registers which are used to receive and transmit C/I codes have been changed. With the previous IPAC, the 4-bit C/I code was at bit positions 2..5, with the new IPAC-X the C/I code is in position 4..7 (i.e. the higher nibble of the respective register). This should be checked if using existing software.

The C/I1 channel can be switched between 4-bit C/I codes and 6-bit C/I codes. The old IPAC always used 6-bit C/I codes. This can be programmed via the CIX1.CICW bit.

If the C/I1 handler is not used it is possible to switch off the C/I1 channel (DCI_CR.EN_CI1 = 0). For the C/I0 channel, this can only be done via a trick. Select in the DCI_CR register an IOM-2 channel that is not used or can never occur (in TE mode e.g. CH3 and following).

7.1 Intelligent NT Support

All new S-Transceivers supports the intelligent NT feature (except ISAC-SX TE).

The intelligent NT mode can only be selected via software (i.e. not via pin-strapping). Either the NT statemachine or the LT-S statemachine may be used (together with an U-transceiver only iNT mode makes sense). This mode is identical to the basic modes with the addition of the D channel arbitration logic.

The S-Transceiver works in the IOM channel 1 (the second) in that mode (C/I1), i.e. uses bits 2..5 of time slot 7 (the U-Transceiver uses the bits 2..7 of time slot 3 in the iNT application as C/I channel). This implies that the C/I channel must also be programmed in the second IOM channel (C/I1). Since the U-transceiver C/I channel cannot be relocated (always CH0 is used, therefore C/I0 is used for the U-transceiver), the C/I1 registers have to be used to control the S-Transceiver in that mode. To enable this handler, the DPS_CI1 bit has to be reset and the EN_CI1 bit has to be set. Both bits are located in the DCI_CI register.

The C/I0-Handler should be used without setting the BAC-bit (CIX0 = ’CCCC.1110’), because it would block the downstream S-transceiver immediatly.

If more than one D-channel controller should have local access, the priority is selected with the TIC bus address.

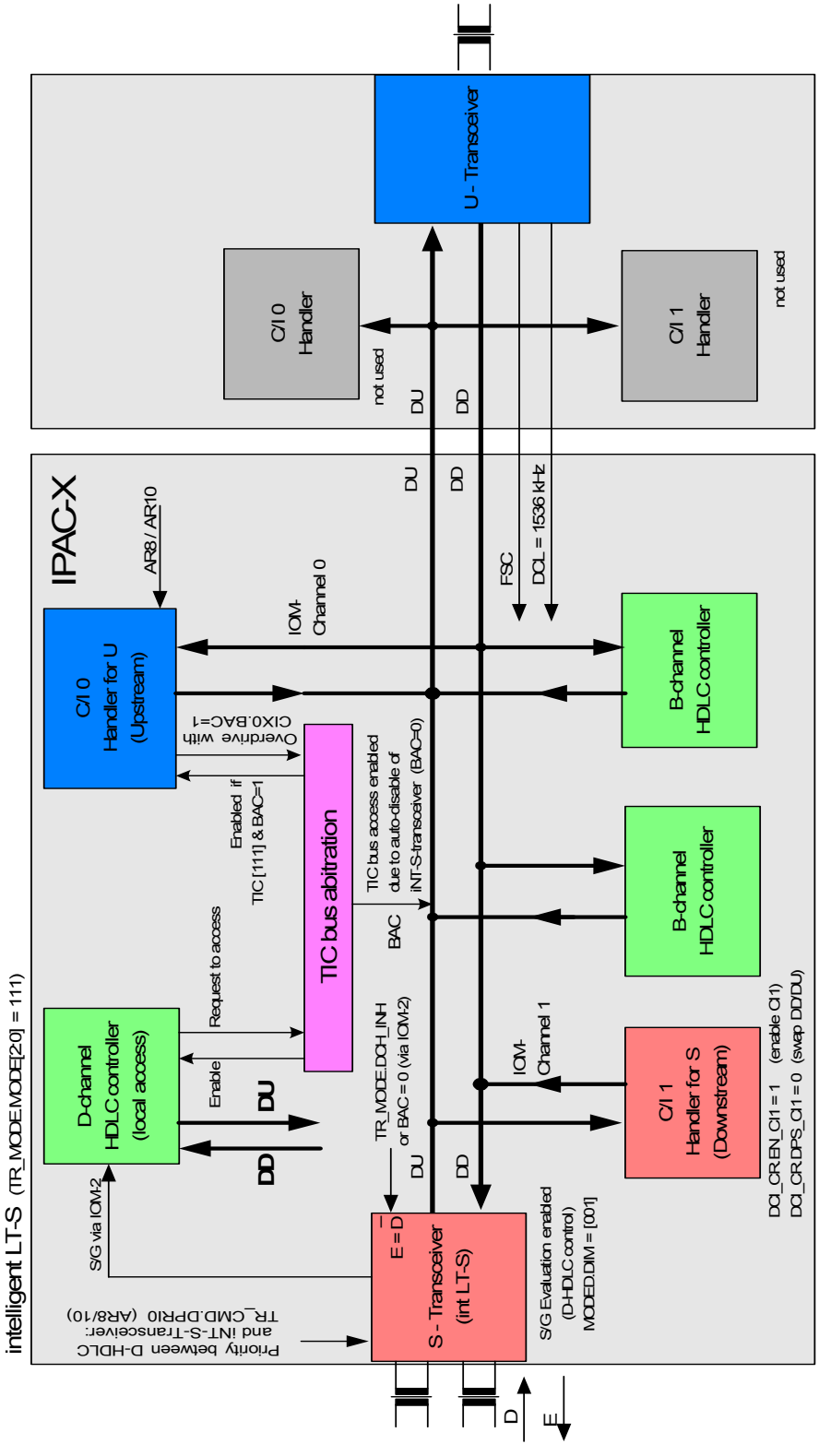

Figure 8 Intelligent NT mode

Table 13 Intelligent NT/LT-S mode

Chip	Related bits
IPAC PSB 2115	STCR.TBA0..2, SCFG.PRI, CONF.IDH, SPCR.SPM, MON-8-Configuration (FSMM)
ISAC-S PEB 2086	not supported
SBCX PEB 2081	MON-8-Configuration (FSMM)
IPAC-X PSB 21150	CIX0.TBA0..2, TR_CMD.DPRIO, DCI_CR.EN_CI1, DCI_CR.DPS_CI1
ISAC-SX PEB 3086	CIX0.TBA0..2, TR_CMD.DPRIO, DCI_CR.EN_CI1, DCI_CR.DPS_CI1
SBCX-X PEB 3081	CIX0.TBA0..2, TR_CMD.DPRIO, DCI_CR.EN_CI1, DCI_CR.DPS_CI1