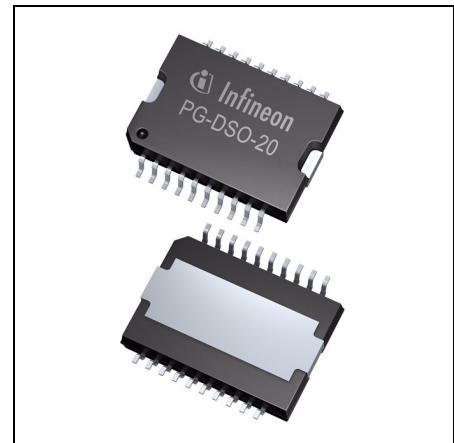




Features

- Triple Voltage Regulator
- Output Voltage 5 V with 450 mA Current Capability
- Two tracked Outputs for 50 mA and 100 mA
- Enable Function for main and tracked Output(s)
- Reset with adjustable Threshold
- Undervoltage- and Power On-Reset
- Watchdog
- Independent Watchdog- and Reset delay
- Wide Temperature Range
- Overtemperature Protection
- Overvoltage Protection
- Reverse Polarity Proof
- Green Product (RoHS compliant)
- AEC Qualified



Functional Description

The TLE 4471 is a monolithic integrated very low-drop triple voltage regulator. The main output supplies loads up to 450 mA and the additional tracked outputs can provide up to 50 mA and 100 mA. In addition the device includes a watchdog for microcontroller-supervision, an undervoltage reset, a power on reset and extended enabling features. The watchdog and reset timing can be chosen independently of each other. The TLE 4471 is available in a Power PG-DSO-20 package. It is designed to supply microprocessor systems under the severe condition of automotive applications and therefore it is equipped with additional protection against overload, short circuit and overtemperature. Of course the TLE 4471 can be used in other applications as well.

The TLE 4471 operates in the temperature range of $T_j = -40$ to 150 °C.

| Type | Package |
|------------|-----------------|
| TLE 4471 G | Power PG-DSO-20 |

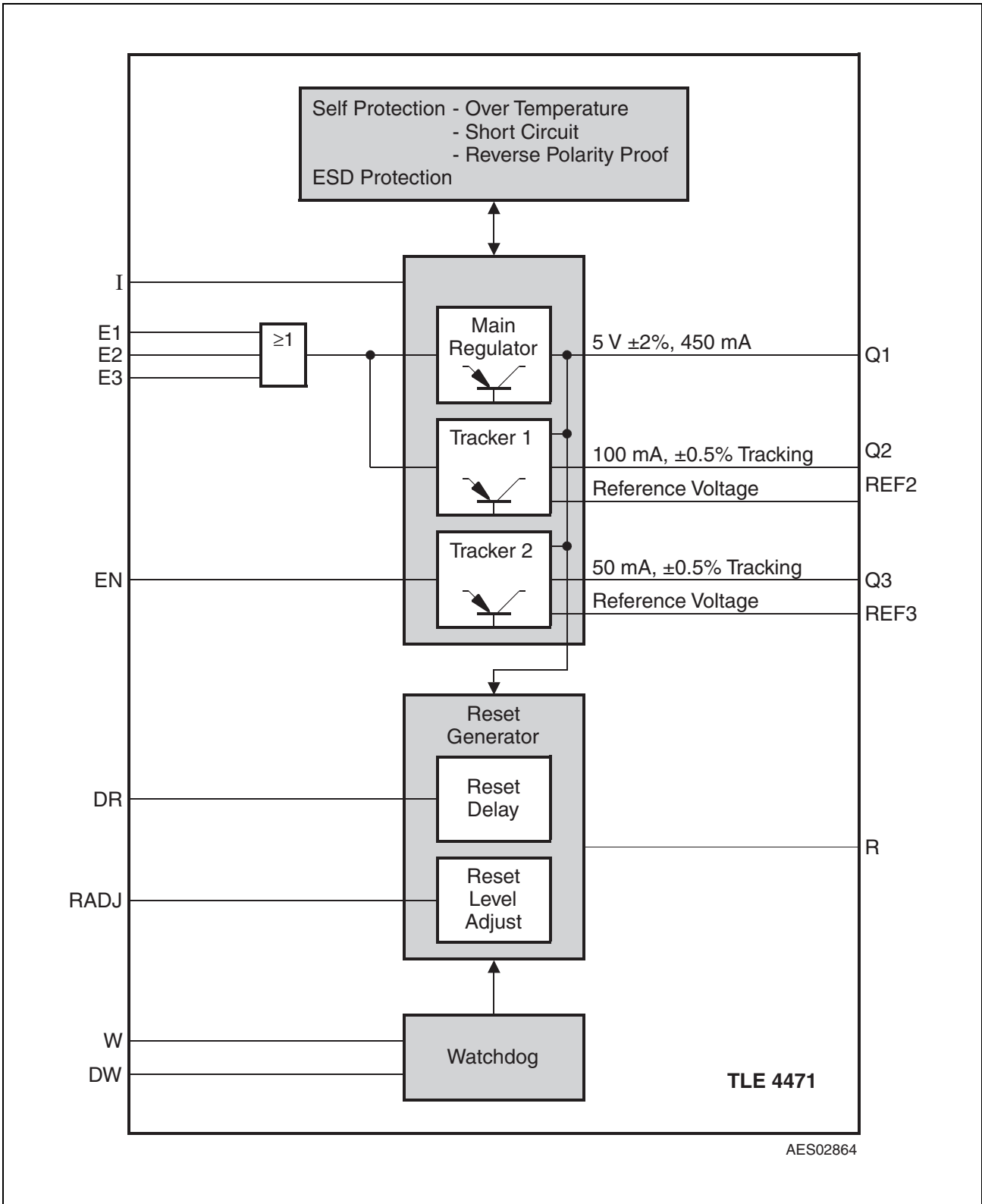


Figure 1 Block Diagram

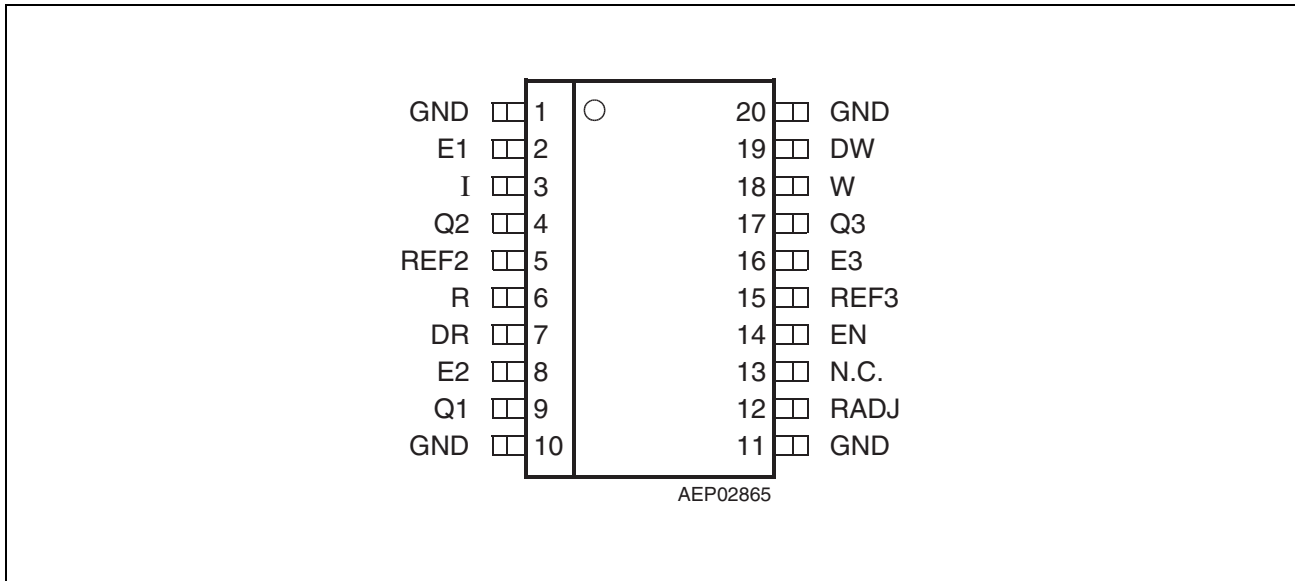


Figure 2 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

| Pin No. | Symbol | Function |
|---------------|--------|--|
| 1, 10, 11, 20 | GND | GROUND ; all four pins connected to the heat sink |
| 2 | E1 | Enable 1 ; Enable for Main Output Q1 and Q2; E1, E2 and E3 are ored together; connect to GND, if not needed. |
| 3 | I | Input ; block to ground directly at the IC for line compensation. |
| 4 | Q2 | Tracking Output Q2 ; block to GND with min. 10 μ F with ESR < 3 Ω . |
| 5 | REF2 | Reference Output ; Reference Voltage related to Q2. |
| 6 | R | Reset Output ; the open collector Output is connected to Q1 via an integrated resistor. |
| 7 | DR | Reset Delay ; connect a capacitor to GND for reset delay time adjustment. |
| 8 | E2 | Enable 2 ; Enable for Main Output Q1 and Q2; E1, E2 and E3 are ored together; connect to GND, if not needed. |
| 9 | Q1 | Main Output Q1 ; block to GND with min. 22 μ F, ESR < 3 Ω . |
| 12 | RADJ | Reset Switching Threshold Adjust ; The reset threshold can be set individually with an external voltage divider at the pin. If it is connected straight to GND the reset threshold remains at 4.65 V. |
| 13 | NC | Not Connected |

Table 1 Pin Definitions and Functions (cont'd)

| Pin No. | Symbol | Function |
|---------|--------|--|
| 14 | EN | Enable Input ; enables Q3 |
| 15 | REF3 | Reference Output ; Reference Voltage related to Q3. |
| 16 | E3 | Enable 3 ; Enable for Main Output Q1 and Q2; E1, E2 and E3 are orred together; connect to GND, if not needed. |
| 17 | Q3 | Tracker Output Q3 ; block to GND with min. 10 μ F with ESR < 3 Ω . |
| 18 | W | Watchdog Trigger Input ; positive edge triggered input for monitoring a microcontroller. |
| 19 | DW | Watchdog Delay ; connect a capacitor to GND for watchdog trigger time adjustment. |

Table 2 Absolute Maximum Ratings
 $T_j = -40$ to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|------------------------------|------------|--------------|------|------|--------------------|
| | | Min. | Max. | | |
| Input I | | | | | |
| Input voltage | V_I | -45 | 42 | V | – $t < 400$ ms |
| | | – | 60 | V | |
| Main Output Q1 | | | | | |
| Output voltage | V_{Q1} | -0.3 | 7 | V | – |
| Output current | I_{Q1} | – | – | mA | internally limited |
| Tracking Output Q2 | | | | | |
| Output voltage | V_{Q2} | -2 | 27 | V | – |
| Output current | I_{Q2} | – | – | mA | internally limited |
| Tracking Output Q3 | | | | | |
| Output voltage | V_{Q3} | -2 | 27 | V | – |
| Output current | I_{Q3} | -5 | – | mA | internally limited |
| Enable Input E1 | | | | | |
| Input voltage | V_{E1} | -0.3 | 16 | V | – |
| Input current | I_{E1} | -20 | 20 | mA | – |
| Enable Input E2 | | | | | |
| Input voltage | V_{E2} | -0.3 | 6.5 | V | – |
| Input current | I_{E2} | – | – | mA | internally limited |
| Enable Input E3 | | | | | |
| Input voltage | V_{E3} | -0.3 | 16 | V | – |
| Input current | I_{E3} | -20 | 20 | mA | – |
| Enable Input EN | | | | | |
| Input voltage | V_{EN} | -0.3 | 7 | V | – |
| Input current | I_{EN} | – | – | mA | internally limited |
| Reference Output REF2 | | | | | |
| Output voltage | V_{REF2} | -0.3 | 4.5 | V | – |
| Output current | I_{REF2} | – | – | mA | – |

Table 2 Absolute Maximum Ratings (cont'd)
 $T_j = -40$ to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--------------------------------|------------|--------------|------|------|--------------------|
| | | Min. | Max. | | |
| Reference Output REF3 | | | | | |
| Output voltage | V_{REF3} | -0.3 | 4.5 | V | – |
| Output current | I_{REF3} | – | – | mA | – |
| Reset Adjust Input RADJ | | | | | |
| Input Voltage | V_{RADJ} | -0.3 | 7 | V | – |
| Input Current | I_{RADJ} | – | – | mA | internally limited |
| Reset Delay DR | | | | | |
| Voltage | V_{DR} | -0.3 | 7 | V | – |
| Reset Output R | | | | | |
| Voltage | V_R | -0.3 | 7 | V | – |
| Watchdog Delay DW | | | | | |
| Voltage | V_{DW} | -0.3 | 7 | V | – |
| Watchdog Input W | | | | | |
| Input voltage | V_W | -0.3 | 7 | V | – |
| Input current | I_W | – | – | mA | – |
| Temperature | | | | | |
| Junction temperature | T_j | -50 | 150 | °C | – |
| Storage temperature | T_{Stg} | -65 | 150 | °C | – |
| Thermal Data | | | | | |
| Junction-ambient | R_{thja} | – | – | K/W | – |
| | R_{thjp} | – | 4 | K/W | – |
| ESD | | | | | |
| Human Body Model | – | -2 | 2 | kV | – |

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Notes |
|----------------------------|------------|--------------|------|------|-------|
| | | Min. | Max. | | |
| Input voltage | V_I | 5.5 | 40 | V | – |
| Junction temperature | T_j | -40 | 150 | °C | – |
| Shutdown voltage threshold | V_{shut} | – | 44 | V | – |

Note: In the operating range, the functions given in the circuit description are fulfilled.

Table 4 Characteristics
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|----------------------------------|-----------------------------------|--------------|------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Main Output Q1 | | | | | | |
| Output voltage | V_{Q1} | 4.9 | 5.0 | 5.1 | V | $10 \text{ mA} < I_{Q1} < 450 \text{ mA};$ $5.5 \text{ V} < V_I < 19 \text{ V}$ |
| Output voltage | V_{Q1} | 4.8 | 5.0 | 5.2 | V | $10 \text{ mA} < I_{Q1} < 300 \text{ mA};$ $5.5 \text{ V} < V_I < 28 \text{ V}$ |
| Output voltage | V_{Q1} | 4.8 | 5.0 | 5.2 | V | $10 \text{ mA} < I_{Q1} < 200 \text{ mA};$ $5.5 \text{ V} < V_I < 40 \text{ V}$ |
| Output current limit | I_{Q1} | 550 | – | 1500 | mA | $V_{Q1} = 0.1 \text{ V}$ |
| Output voltage drop | V_{DR} | – | 0.25 | 0.55 | V | $I_{Q1} = 450 \text{ mA}^{1)}$ |
| Line regulation | ΔV_{Q1} | -25 | – | 25 | mV | $8 \text{ V} \leq V_I \leq 16 \text{ V};$ $I_{Q1} = 10 \text{ mA}$ |
| Load regulation | ΔV_{Q1} | -25 | – | 25 | mV | $10 \text{ mA} < I_{Q1} < 450 \text{ mA};$ $V_I = 7 \text{ V}$ |
| Power Supply Ripple Rejection | $PSRR$ | – | 30 | – | dB | $C_{Q1} = 22 \text{ } \mu\text{F};$ $20 \text{ Hz} < f_r < 20 \text{ kHz};$ $V_{PP} = 0.5 \text{ V}^{2)}$ |
| Output capacitor | C_{Q1} | 22 | – | – | μF | ²⁾ |
| ESR of output capacitor | ESR | – | – | 3 | Ω | at $10 \text{ kHz}^{2)}$ |
| Tracked Output Q2 | | | | | | |
| Output voltage tracking accuracy | $\Delta V_{Q2} = V_{Q2} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 19 \text{ V};$ $1 \text{ mA} < I_{Q2} < 100 \text{ mA}$ |
| Output voltage tracking accuracy | $\Delta V_{Q2} = V_{Q2} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 28 \text{ V};$ $1 \text{ mA} < I_{Q2} < 80 \text{ mA}$ |
| Output voltage tracking accuracy | $\Delta V_{Q2} = V_{Q2} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 40 \text{ V};$ $1 \text{ mA} < I_{Q2} < 50 \text{ mA}$ |
| Output current limit | I_{Q2} | 110 | – | – | mA | $V_{Q2} = 0.1 \text{ V}$ |
| Output voltage drop | V_{DR2} | – | – | 0.6 | V | $I_{Q2} = 100 \text{ mA}$ |
| Power Supply Ripple Rejection | $PSRR$ | – | 30 | – | dB | $20 \text{ Hz} < f_r < 20 \text{ kHz};$ $V_{PP} = 0.5 \text{ V};$ $C_{Q2} = 10 \text{ } \mu\text{F}^{2)}$ |

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|-------------------------|----------|--------------|------|------|---------------|-------------------------|
| | | Min. | Typ. | Max. | | |
| Output capacitor | C_{Q2} | 10 | – | – | μF | ²⁾ |
| ESR of output capacitor | ESR | – | – | 3 | Ω | at 10 kHz ²⁾ |

Tracked Output Q3

| | | | | | | |
|--|-------------------------------------|-----|----|-----|---------------|--|
| Output voltage tracking accuracy | $\Delta V_{Q3} = V_{Q3} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 19 \text{ V};$ $1 \text{ mA} < I_{Q3} < 50 \text{ mA}$ |
| Output voltage tracking accuracy | $\Delta V_{Q3} = V_{Q3} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 28 \text{ V};$ $1 \text{ mA} < I_{Q3} < 40 \text{ mA}$ |
| Output voltage tracking accuracy | $\Delta V_{Q3} = V_{Q3} - V_{Q1}$ | -25 | – | 25 | mV | $5.7 \text{ V} < V_I < 40 \text{ V};$ $1 \text{ mA} < I_{Q3} < 25 \text{ mA}$ |
| Output current limit | I_{Q3} | 55 | – | 150 | mA | $V_{Q3} = 0.1 \text{ V}$ |
| Output voltage drop | V_{DR3} | – | – | 0.6 | V | $1 \text{ mA} \leq I_{Q3} \leq 50 \text{ mA}$ |
| Power Supply Ripple Rejection | $PSRR$ | – | 30 | – | dB | $20 \text{ Hz} < f_r < 20 \text{ kHz};$ $V_{PP} = 0.5 \text{ V};$ $C_{Q3} = 10 \mu\text{F}^2)$ |
| Output capacitor | C_{Q3} | 10 | – | – | μF | ²⁾ |
| ESR of output capacitor | ESR | – | – | 3 | Ω | at 10 kHz ²⁾ |
| Matching error between V_{Q2} and V_{Q3} | $\Delta V_{Q2,3} = V_{Q3} - V_{Q2}$ | -25 | – | 25 | mV | – |

Current Consumption

| | | | | | | |
|---|-------|---|------|----|---------------|--|
| Quiescent current (standby) | I_q | – | – | 20 | μA | Q1 OFF, Q2 OFF; Q3 OFF |
| Current consumption; $I_q = I_I - I_Q$ | I_q | – | 1100 | – | μA | Q3 OFF, $I_{Q1} < 1 \text{ mA};$ $I_{Q2} < 1 \text{ mA}$ |
| Current consumption; $I_q = I_I - I_Q$ | I_q | – | 1800 | – | μA | $I_{Q1} < 10 \text{ mA};$ $I_{Q2} < 1 \text{ mA};$ $I_{Q3} < 1 \text{ mA}$ |

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|---------------------------------------|---------------|--------------|------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Enable Function E1, E2, E3, EN | | | | | | |
| E1 On threshold | $V_{E1, on}$ | 3.5 | 4.1 | 4.5 | V | $V_{Q1} > 4.8 \text{ V}; V_{Q2} > 4.8 \text{ V}$ |
| E1 Off threshold | $V_{E1, off}$ | 1.5 | – | 2.5 | V | – |
| E1 High input current | $I_{E1, on}$ | – | 50 | – | μA | $V_{E1} = 16 \text{ V}$ |
| E1 Low input current | $I_{E1, off}$ | -1 | – | 5 | μA | $V_{E1} = 0 \text{ V}$ |
| E2 On threshold | $V_{E2, on}$ | 1.3 | 1.7 | 2.0 | V | $V_{Q1} > 4.8 \text{ V}; V_{Q2} > 4.8 \text{ V}$ |
| E2 Off threshold | $V_{E2, off}$ | 0.8 | 1.2 | 1.7 | V | – |
| E2 resistance to GND | R_{E2} | 5 | 15 | 40 | $\text{k}\Omega$ | – |
| E3 On threshold | $V_{E3, on}$ | 3.5 | – | 4.5 | V | $V_{Q1} > 4.8 \text{ V}; V_{Q2} > 4.8 \text{ V}$ |
| E3 Off threshold | $V_{E3, off}$ | 1.5 | – | 2.5 | V | – |
| E3 High input current | $I_{E3, on}$ | – | 50 | – | μA | $V_{E3} = 16 \text{ V}$ |
| E3 Low input current | $I_{E3, off}$ | -1 | – | 5 | μA | $V_{E3} = 0 \text{ V}$ |
| EN On threshold | $V_{EN, on}$ | 1.0 | 1.7 | 2.3 | V | $V_{Q3} > 4.8 \text{ V}; Q1 \text{ ON}$ |
| EN Off threshold | $V_{EN, off}$ | 0.8 | 1.2 | 1.7 | V | $V_{Q3} < 0.1 \text{ V}$ |
| Enable resistance to GND | R_{EN} | 5 | 15 | 40 | $\text{k}\Omega$ | – |
| Reset Generator | | | | | | |
| Switching threshold | $V_{Q, rth}$ | 4.5 | 4.65 | 4.8 | V | RADJ connected to GND |
| Reset headroom | V_{head} | 250 | 350 | 500 | mV | $10 \text{ mA} < I_{Q1} < 450 \text{ mA}$ |
| Reset pull-up | R_R | 2.4 | – | 6 | $\text{k}\Omega$ | – |
| Reset output low voltage | $V_{R, low}$ | – | – | 0.4 | V | $1 \text{ V} < V_{Q1} < V_{Q, rth}$ |
| Reset output Low voltage | $V_{R, low}$ | – | – | 0.4 | V | $V_{Q1} = 1 \text{ V}, I_R = 50 \mu\text{A}$ |
| Reset output High voltage | $V_{R, high}$ | 4.5 | – | – | V | – |
| Reset adjust threshold | V_{RADJ} | 1.25 | 1.35 | 1.45 | V | $V_{Q1} > 3.5 \text{ V}$ |

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|-------------------------------|---------------|--------------|------|------|---------------|------------------------|
| | | Min. | Typ. | Max. | | |
| Reset delay charging current | $I_{DR, ch}$ | 2 | 4 | 6 | μA | $V_{DR} = 1 \text{ V}$ |
| Reset delay discharge current | $I_{DR, dis}$ | 60 | 120 | 160 | mA | $V_{DR} = 1 \text{ V}$ |
| Upper reset timing threshold | $V_{DR, dt}$ | 0.9 | 1.8 | 2.7 | V | – |
| Lower timing threshold | $V_{DR, st}$ | 0.25 | 0.4 | 0.65 | V | – |
| Reset delay time | t_{dr} | 35 | 50 | 70 | ms | $C_R = 100 \text{ nF}$ |
| Reset reaction time | t_{rr} | 0.5 | – | 3 | μs | $C_R = 100 \text{ nF}$ |

Watchdog

| | | | | | | |
|-----------------------------------|--------------|-----|-----|-----|------------------|--|
| Watchdog input pull-down resistor | R_W | 5 | 15 | 40 | $\text{k}\Omega$ | – |
| Watchdog delay charging current | $I_{DW, ch}$ | 2 | 4 | 6 | μA | $V_{DW} = 1 \text{ V}; V_{DR} = 2.7 \text{ V}$ |
| Watchdog upper timing threshold | $V_{DW, dt}$ | 1.5 | 1.9 | 2.5 | V | – |
| Watchdog lower timing threshold | $V_{DW, st}$ | 0 | 30 | 200 | mV | – |
| Watchdog trigger pulse interval | t_{wp} | 35 | 50 | 70 | ms | $C_{DW} = 100 \text{ nF}$ |

Reference Output REF2

| | | | | | | |
|-----------------------|------------|------|----|------|------------------|---|
| Voltage divider ratio | V_{REF2} | 49.5 | 50 | 50.5 | % of V_{Q2} | – |
| Output impedance | R_{REF2} | 10 | – | 20 | $\text{k}\Omega$ | – |
| Output clamp voltage | – | – | – | 4.5 | V | – |

Table 4 Characteristics (cont'd)

$V_I = 13.5\text{ V}; T_j = -40\text{ °C} < T_j < 125\text{ °C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|------------------------------|------------|--------------|------|------|---------------|---------------------|
| | | Min. | Typ. | Max. | | |
| Reference Output REF3 | | | | | | |
| Voltage divider ratio | V_{REF3} | 49.5 | 50 | 50.5 | % of V_{Q3} | – |
| Output impedance | R_{REF3} | 10 | – | 20 | k Ω | – |
| Output clamp voltage | – | – | – | 4.5 | V | – |

1) Measured when the output voltage V_Q dropped 100 mV from the nominal value.

2) Not subject to production test, specified by design.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\text{ °C}$ and the given supply voltage.

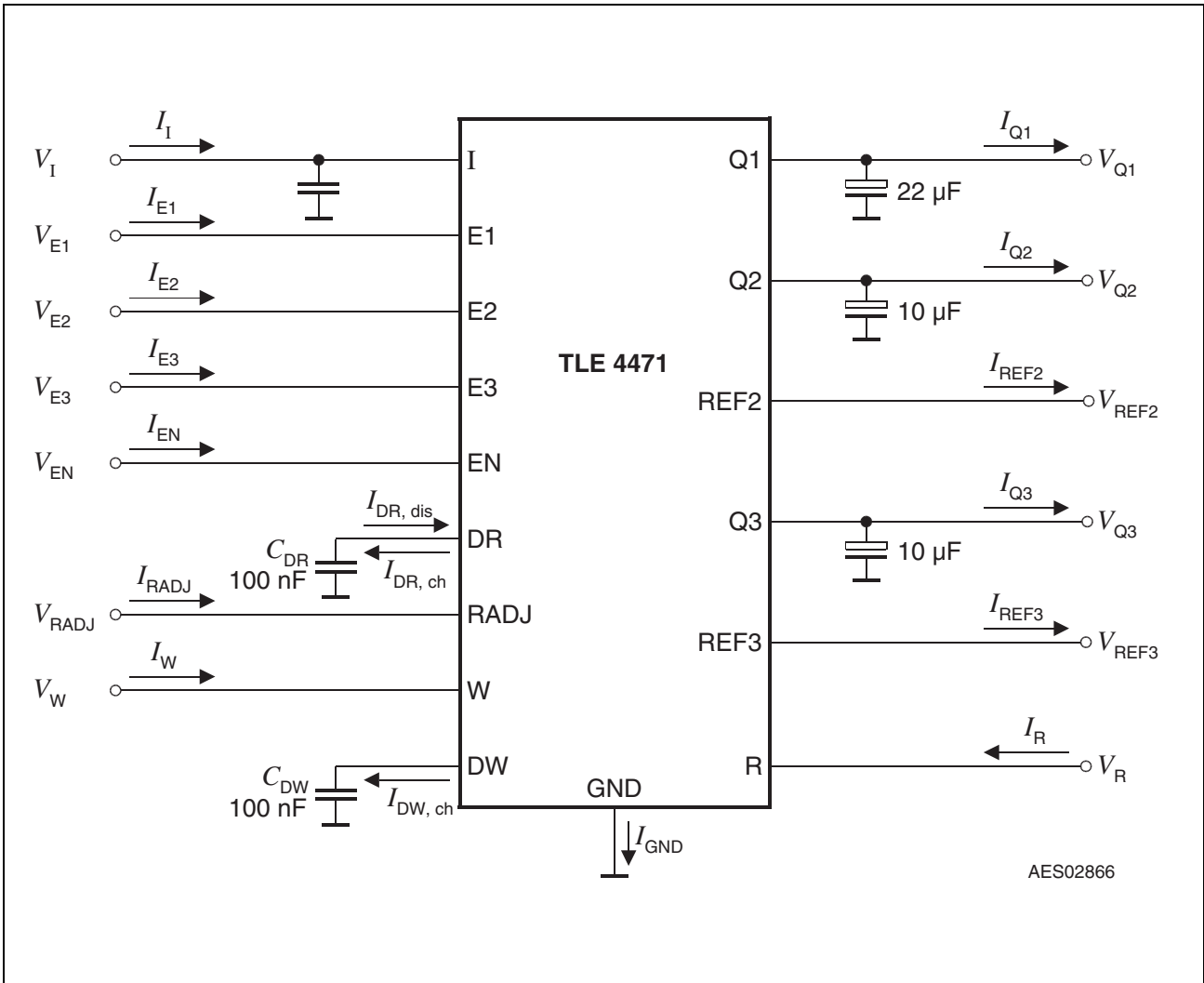


Figure 3 Measurement Circuit

Output Voltage

To obtain an output voltage of $V_{Q1} = 5\text{ V}$ with an accuracy of 2% at the main output Q1 an input voltage in the range of $5.5\text{ V} < V_1 < 40\text{ V}$ is needed. The main output Q1 supplies 5 V with 450 mA current capability. For stability it requires an output capacitor of at least 22 μF and a maximum ESR of 3 Ω . The two outputs Q2 and Q3 are tracked to Q1 and can supply currents of 100 mA and 50 mA. So any undervoltage condition or shutdown of Q1 will cause the same effect to Q2 and Q3. For Stability both outputs require an output capacitor of at least 10 μF with $\text{ESR} < 3\ \Omega$ each. Q2 is switched on and off simultaneously with Q1, while the tracked output Q3 can be enabled or disabled individually.

Two reference outputs REF2, REF3 with voltages of $V_{\text{REF2}} = V_{Q2}/2$ and $V_{\text{REF3}} = V_{Q3}/2$ are also available. In case of an overvoltage at the tracker outputs, the voltage references are limited internally to 4.5 V.

Output Current

The output current is a function of the input voltage. For high input voltages above 22 V, the output current is reduced linear. This is designed into the regulator for protection. Above 42 V the regulator is switched off. The thermal shutdown switches the regulator off, if it exceeds the thermal threshold of 160 °C typical. It is switched on again, as soon as the regulator is cooled down by typical 10 K (thermal hysteresis). Please note the device should not be operated above a junction temperature of 150 °C for long term reliability.

Enable Function

The TLE 4471 includes the possibility of enabling the main and tracked outputs.

Three ORed enable inputs E1, E2, E3 are used to control the main output Q1 and the tracked output Q2. E1 and E3 can be supplied from the battery line or ignition key with input voltages up to 16 V. The enable inputs should be protected by a series resistor and a capacitor, e.g. $R_{E1} = R_{E3} = 22\text{ k}\Omega$, $C_{E1} = C_{E3} = 2.2\text{ nF}$. E2 is intended for connection to the microcontroller. A logic HIGH at any enable input will switch on the related regulator and/or tracker.

A separate enabling pin EN is available to switch on and off the second tracked output Q3 separately by the microcontroller.

Reset

The power on reset feature is necessary for a defined start of the microprocessor during power up. When the output voltage of the main regulator has reached the reset threshold voltage the reset delay capacitor C_{DR} is charged. After a certain time, the reset delay time t_{dr} , the voltage at the capacitor equals the upper reset timing threshold and the reset output goes HIGH.

The reset delay time t_{dr} is defined by the reset delay capacitor C_{DR} at pin DR and can be calculated as follows:

$$t_{rd} = C_{DR} \times \frac{V_{DR,dt}}{I_{DR,ch}} \quad (1)$$

Definitions:

- C_{DR} = reset delay capacitor
- t_{dr} = reset delay time required by the application
- $V_{DR,dt}$ = typical 1.8 V for power up reset
- $I_{DR,ch}$ = charge current typical 4 μ A

For a delay capacitor $C_{DR} = 100$ nF the typical power up reset delay time is 45 ms.

The undervoltage reset circuitry supervises the output voltage. In case V_{Q1} falls below the reset threshold the reset output is set LOW after the reset reaction time t_{rr} (discharge of the reset delay capacitor). The reset LOW signal is held down to an output voltage V_{Q1} of 1 V. Both, the reset reaction time and the reset delay time are defined by the capacitor value.

The reset reaction time t_{rr} is the time it takes the voltage regulator to set its reset output LOW after the output voltage has dropped below the reset threshold. The reset reaction time can be calculated using the following equation:

$$t_{rr} = C_{DR} \times \frac{V_{DR,dt} - V_{DR,st}}{I_{DR,dis}} \quad (2)$$

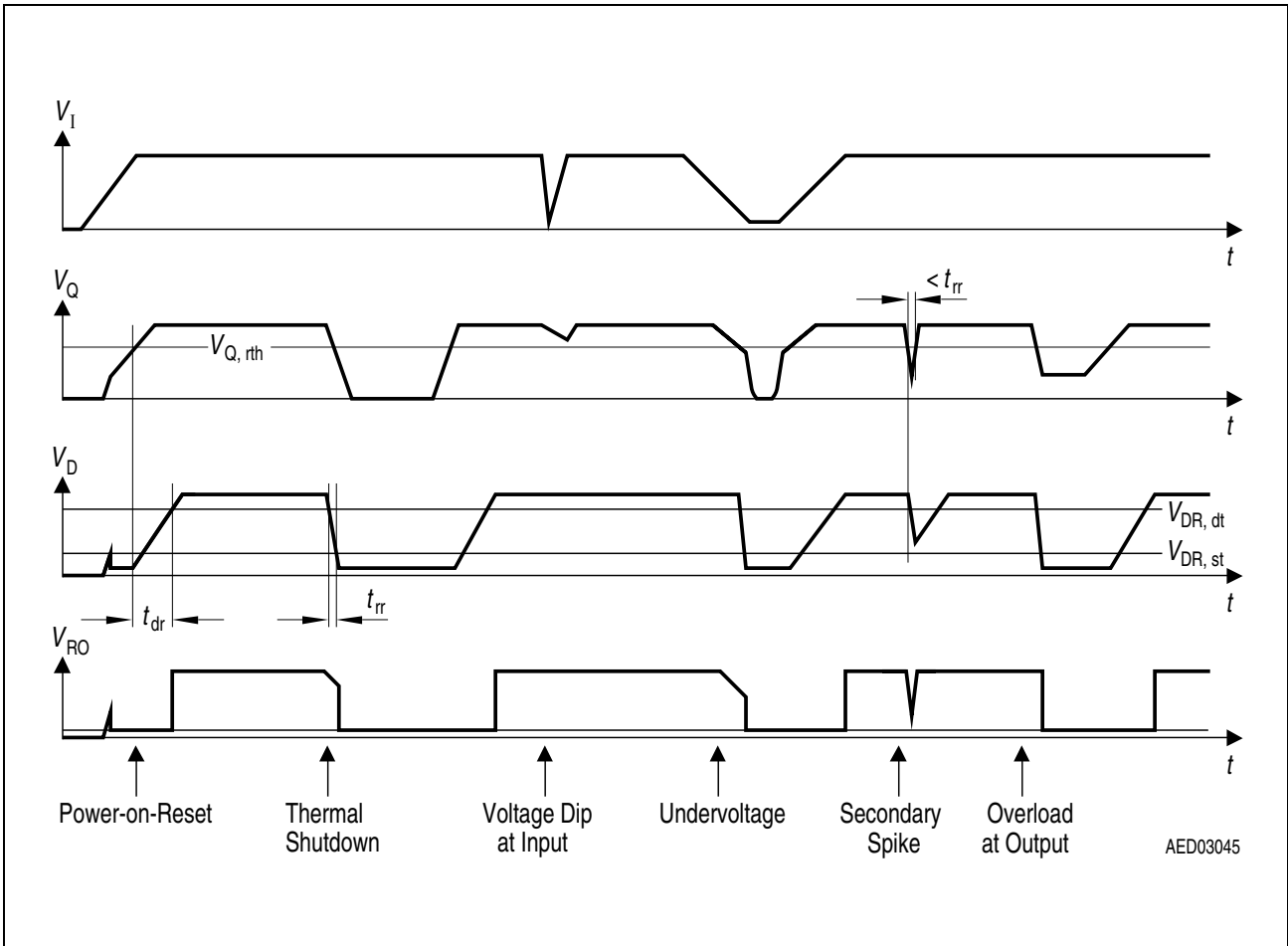


Figure 5 Reset Timing

The reset output is an open collector output with a pull-up-resistor of typical 4 k Ω to Q1. An external pull-up can be added with a resistor value of at least 20 k Ω .

In addition the reset switching threshold can be adjusted by an external voltage divider. The feature is useful with microprocessors which guarantee safe operation down to voltages below the internally set reset threshold of 4.65 typical.

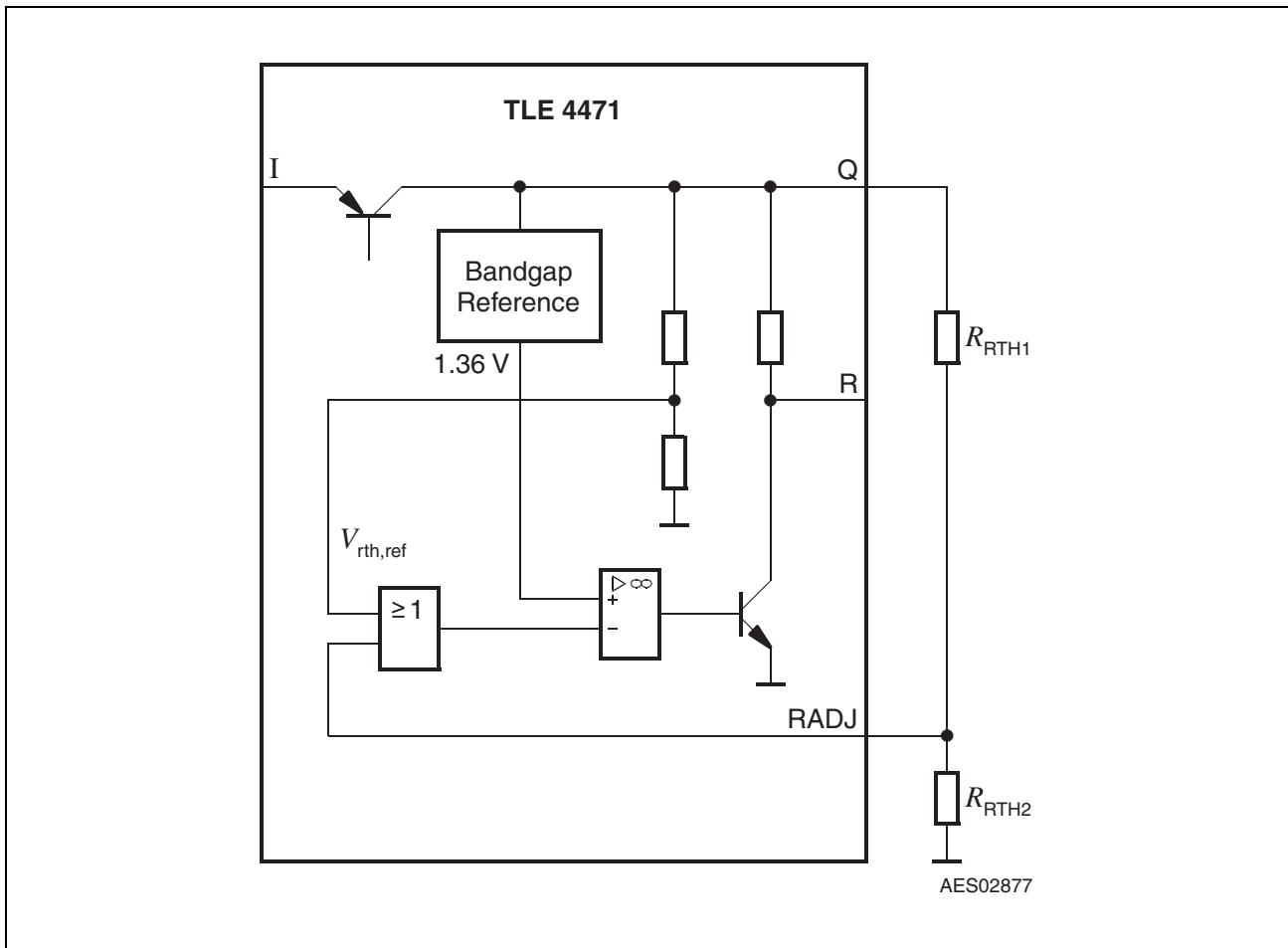


Figure 6 Adjusting the Reset Threshold

For using the preadjusted reset threshold voltage of typical $V_{Q, rth} = 4.65 \text{ V}$, the pin RADJ has to be connected to GND.

If a lower reset threshold is required by the system, a voltage divider defines the reset threshold $V_{Q, rthext}$ between 3.5 V and 4.65 V:

$$V_{Q, rthext} = V_{rth,ref} \times \left(1 + \frac{R_{RTH1}}{R_{RTH2}} \right) \quad (3)$$

$V_{rth,ref}$ is typical 1.35 V.

Watchdog

The reset and watchdog timing can be defined independently of each other by two delay capacitors C_{DR} and C_{DW} at pins DR and DW.

The watchdog function supervises the microcontroller including time base failures. If there is no positive edge within a certain pulse repetition time t_{wp} or the trigger pulse is too short a reset is generated. Programming of the max. repetition time is done by a delay capacitor C_{DW} at pin DW.

The frequency of the watchdog pulses generated by the microcontroller has to be higher than the minimum pulse sequence t_{wp} set by the external reset delay capacitor C_{DW} . The pulse repetition time can be calculated as follows:

$$t_{wp} = C_{DW} \times \frac{V_{DW,dt} - V_{DW,st}}{I_{DW,ch}} \tag{4}$$

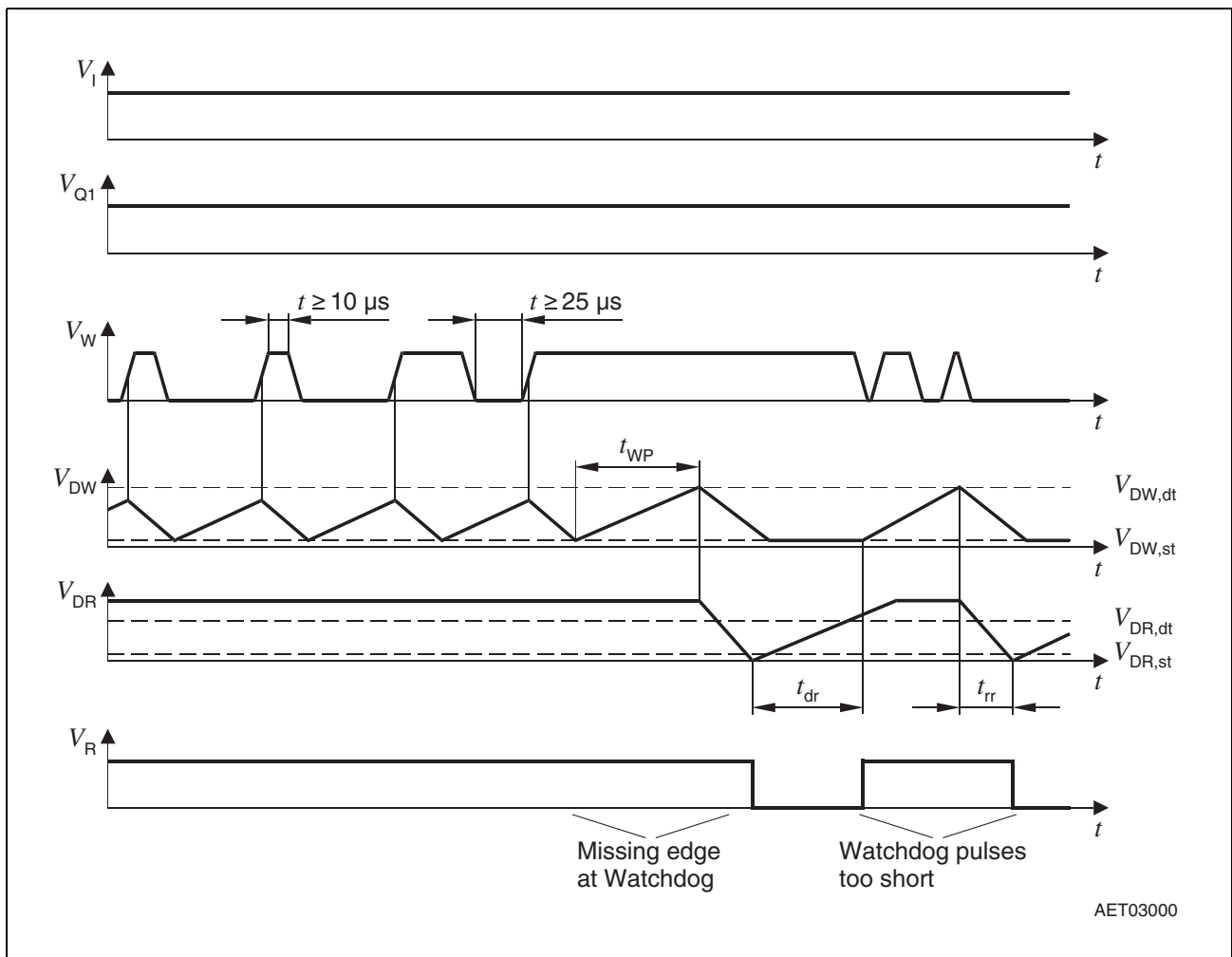
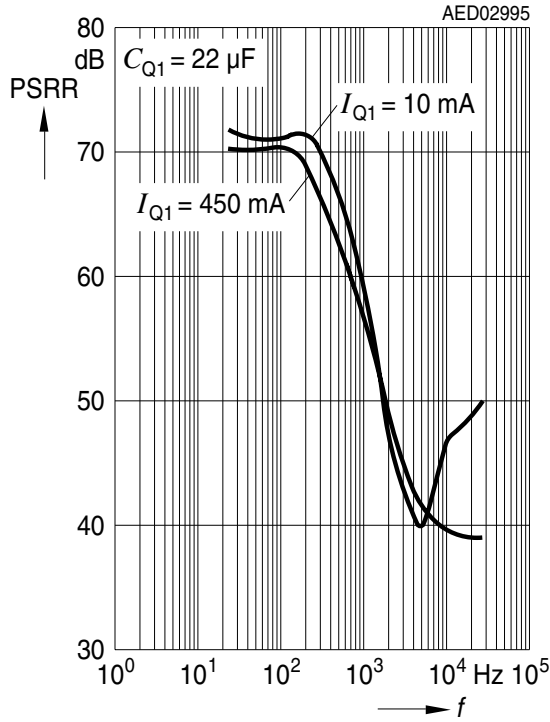


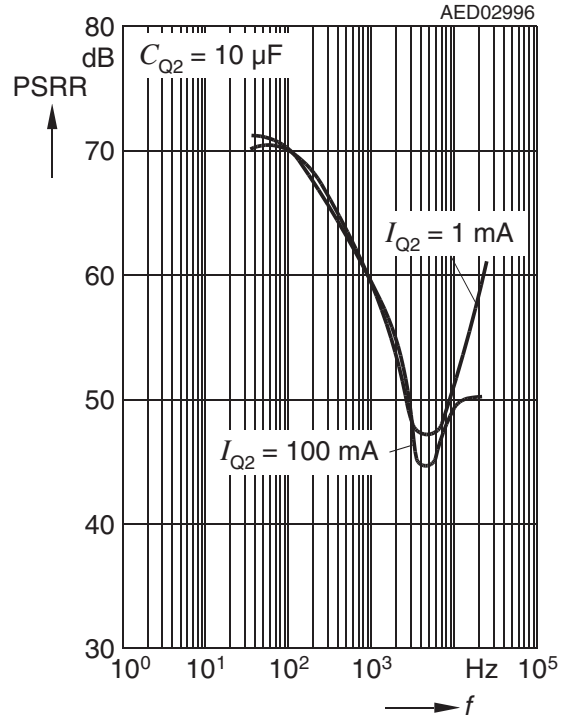
Figure 7 Watchdog Timing

If the watchdog is not used in an application the pin WD has to be connected to GND.

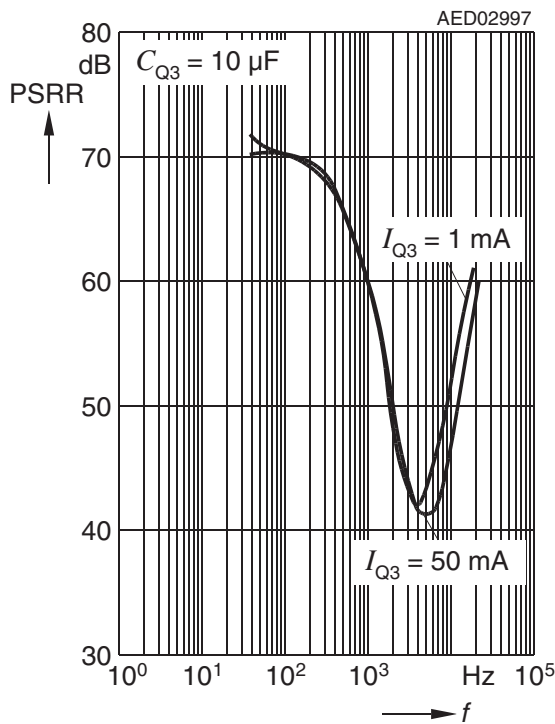
Power Supply Ripple Rejection *PSRR* of Main Output Q1 versus Frequency *f*



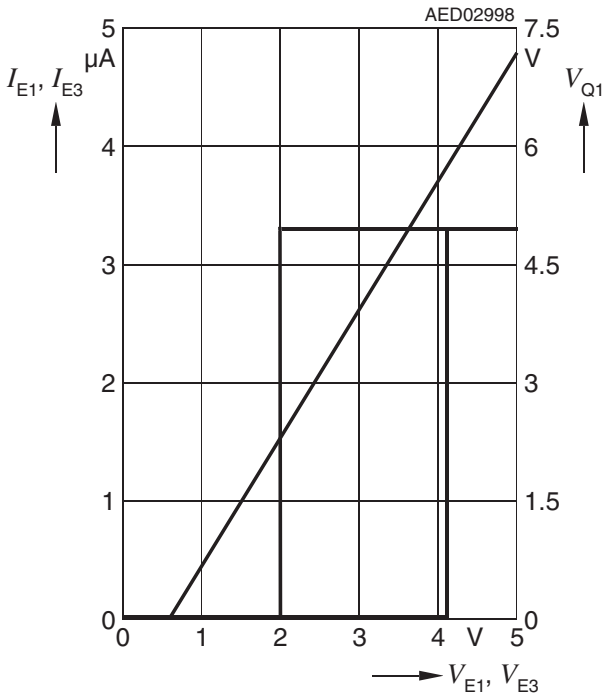
Power Supply Ripple Rejection *PSRR* of Output Q2 versus Frequency *f*



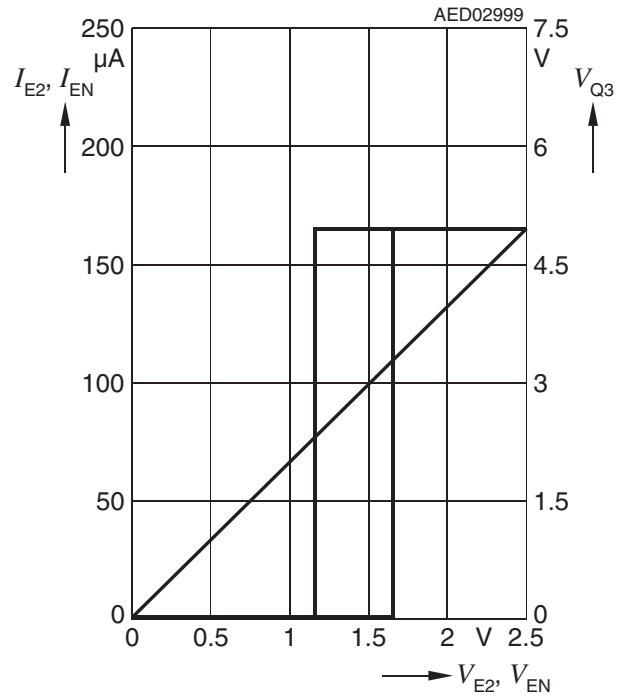
Power Supply Ripple Rejection *PSRR* of Output Q3 versus Frequency *f*



Enable Currents I_{E1} , I_{E3} and Output Voltage V_{Q1} versus Enable Voltages V_{E1} , V_{E3}



Enable Currents I_{E2} , I_{EN} and Output Voltage V_{Q3} versus Enable Voltages V_{E2} , V_{EN}



Package Outlines

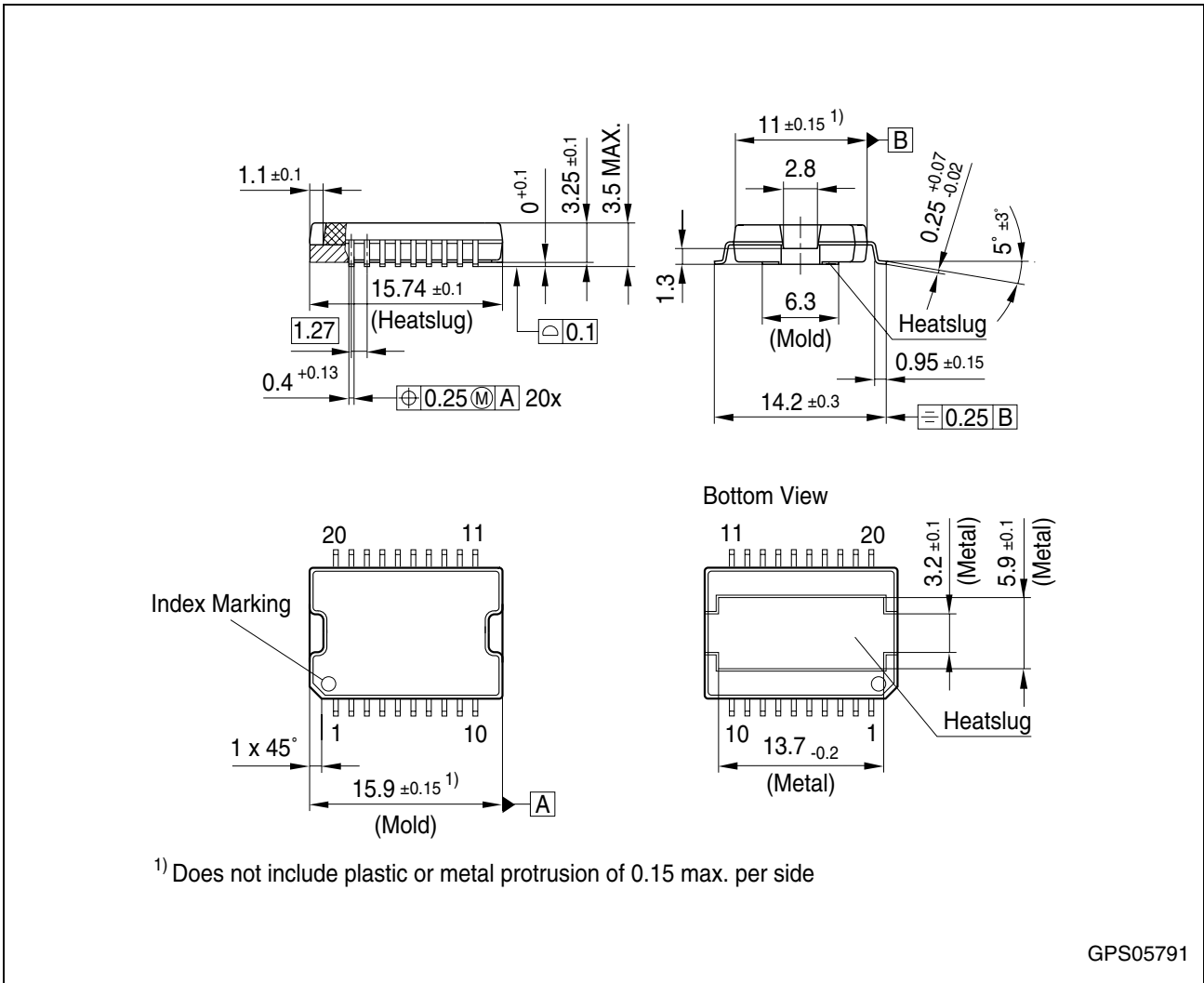


Figure 8 Power PG-DSO-20 (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Find all of our packages, sorts of packing and others in our Infineon Internet Page "Packages": <http://www.infineon.com/packages>.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

| Version | Date | Changes |
|----------|------------|---|
| Rev. 1.6 | 2009-02-03 | Package bond wire modification according to PCN No. 2007-090. Change of package name in datasheet to "Power PG-DSO-20". No change of package outline. |
| Rev. 1.5 | 2007-03-20 | Initial version of RoHS-compliant derivate of TLE 4471 Page 1 : AEC certified statement added Page 1 and Page 22 : RoHS compliance statement and Green product feature added Page 1 and Page 22 : Package changed to RoHS compliant version Legal Disclaimer updated |
| Rev. 1.4 | 2005-01-28 | Parameter "Output Clamp Voltage" REF2 and REF3: Max. value changed from 4V to 4.5V in order to align with the Maximum Ratings |

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