

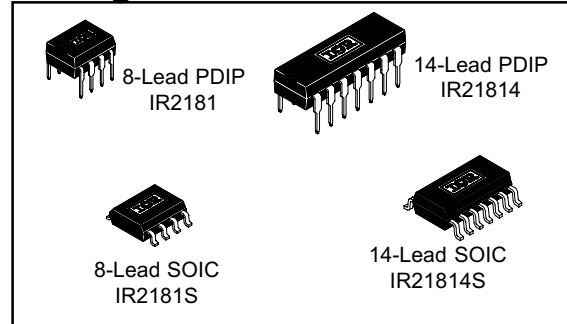
IR2181(4)(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A
- Also available LEAD-FREE (PbF)

Packages



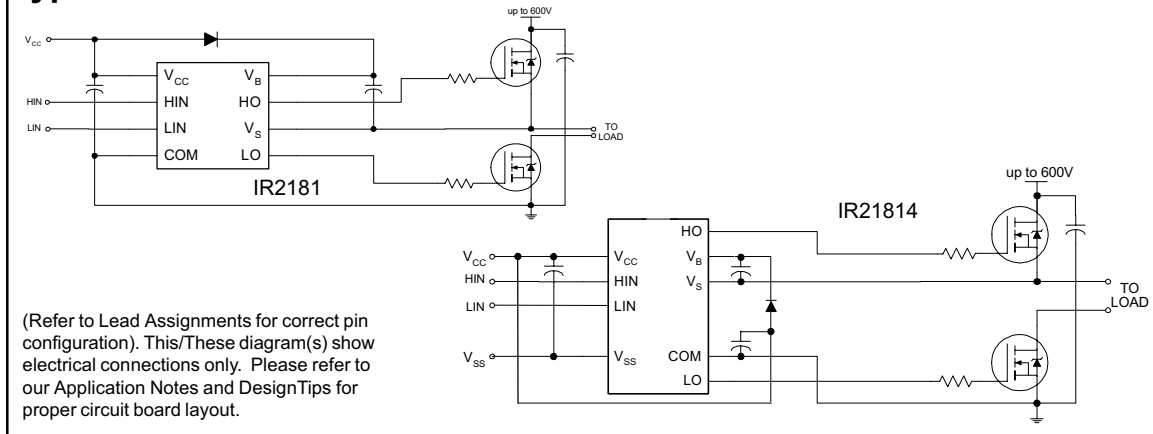
IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181 21814	HIN/LIN	no	none	COM VSS/COM	180/220 ns
2183 21834	HIN/LIN	yes	Internal 500ns Program 0.4 ~ 5 us	COM VSS/COM	180/220 ns
2184 21844	IN/SD	yes	Internal 500ns Program 0.4 ~ 5 us	COM VSS/COM	680/270 ns

Description

The IR2181(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



IR2181(4) (S) & (PbF)

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	V _{SS} - 0.3	V _{SS} + 10		
V _{SS}	Logic ground (IR21814 only)	V _{CC} - 25	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	V _{SS}	V _{SS} + 5	
V _{SS}	Logic ground (IR21814/IR21824 only)	-5	5	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: HIN and LIN pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	220	330		$V_S = 0V$ or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	35		
t_r	Turn-on rise time	—	40	60		$V_S = 0V$
t_f	Turn-off fall time	—	20	35		$V_S = 0V$

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads HIN and LIN. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2181/IR21814)	2.7	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage (IR2181/IR21814)	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" input bias current	—	25	60		$V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current	—	—	1.0		$V_{IN} = 0V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	$V_O = 0V$, $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		$V_O = 15V$, $PW \leq 10 \mu s$

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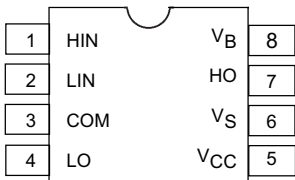
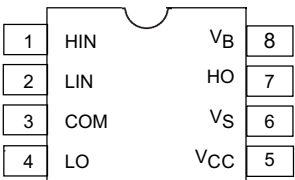
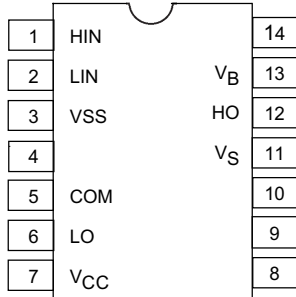
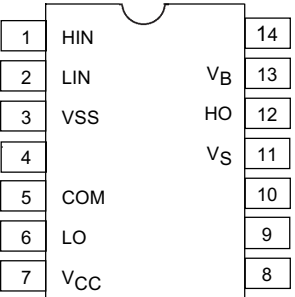
21814

The schematic diagram for the 21814 circuit is similar to the 2181 circuit but includes an additional input, VSS, which is connected to ground. The HIN and LIN inputs are each connected to a resistor and an inverter. The HIN signal path includes a VSS/COM Level Shift block before the Pulse Generator. The LIN signal path includes a VSS/COM Level Shift block and a Delay block before an AND gate. The AND gate's output is connected to the UV Detect block. The UV Detect block's output is connected to the LO output. The Pulse Generator's output is connected to the HV Level Shifter, which then connects to the Pulse Filter. The Pulse Filter's output is connected to the Q output of the SR flip-flop. The SR flip-flop's R and S inputs are connected to the UV Detect block. The Q output of the SR flip-flop is connected to the HO output. The VS output is connected to the VSS input. The VCC output is connected to the VCC input. The COM output is connected to the COM input.

Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2181/IR21814)
LIN	Logic input for low side gate driver output (LO), in phase (IR2181/IR21814)
VSS	Logic Ground (IR21814 only)
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

 8-Lead PDIP IR2181	 8-Lead SOIC IR2181S
 14-Lead PDIP IR21814	 14-Lead SOIC IR21814S

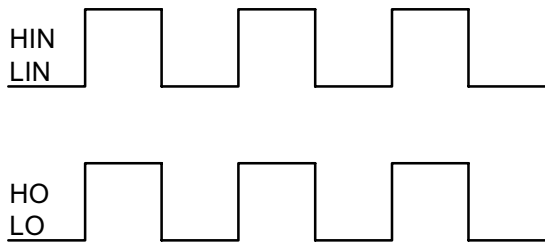


Figure 1. Input/Output Timing Diagram

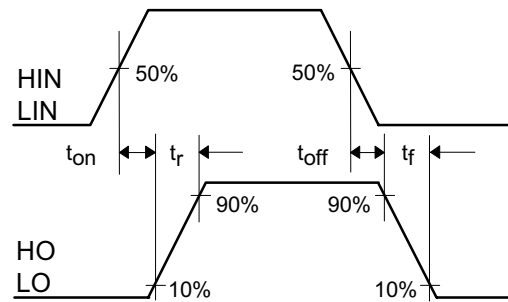


Figure 2. Switching Time Waveform Definitions

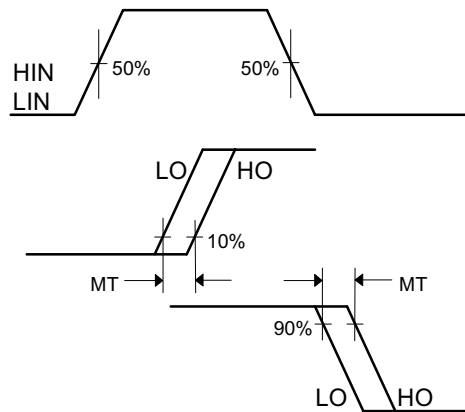


Figure 3. Delay Matching Waveform Definitions

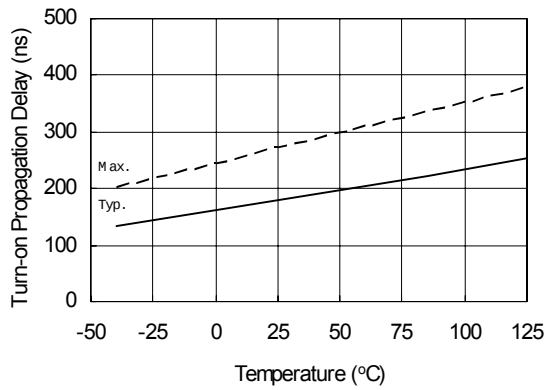


Figure 4A. Turn-on Propagation Delay vs. Temperature

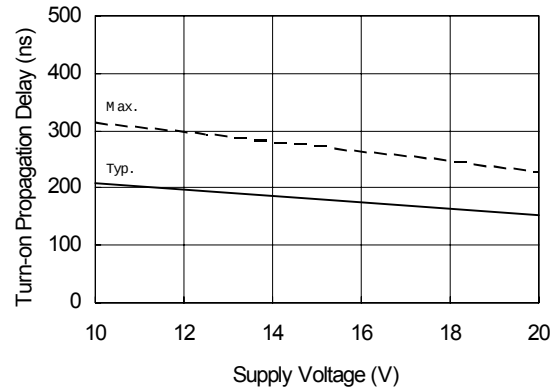


Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

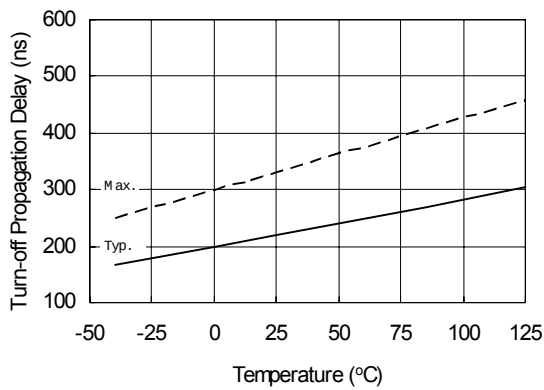


Figure 5A. Turn-off Propagation Delay vs. Temperature

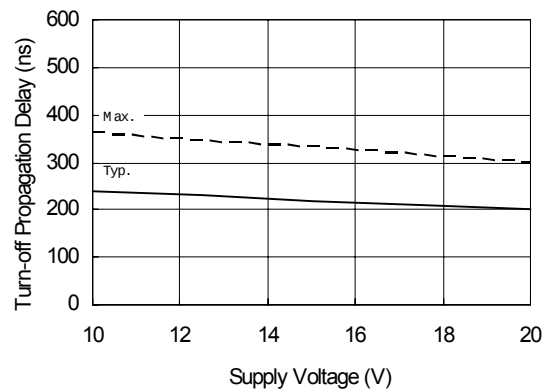


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

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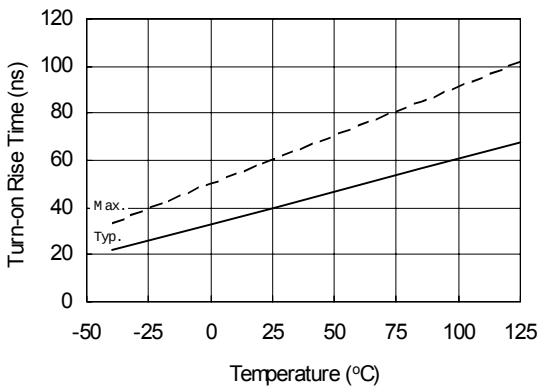


Figure 6A. Turn-on Rise Time vs. Temperature

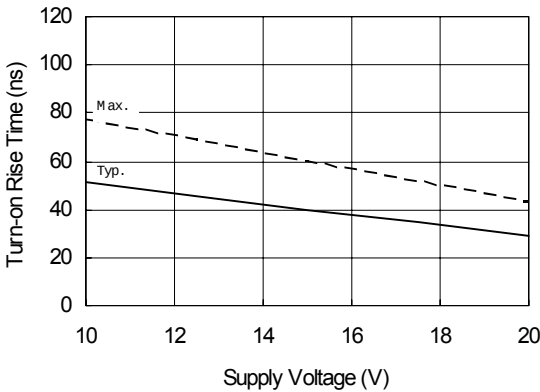


Figure 6B. Turn-on Rise Time vs. Supply Voltage

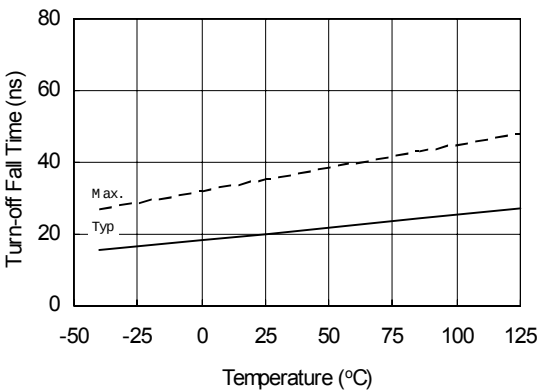


Figure 7A. Turn-off Fall Time vs. Temperature

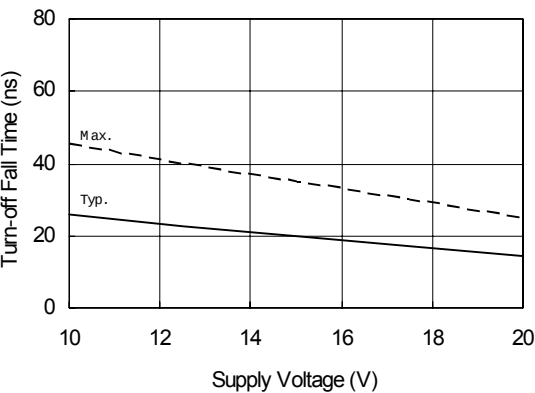


Figure 7B. Turn-off Fall Time vs. Supply Voltage

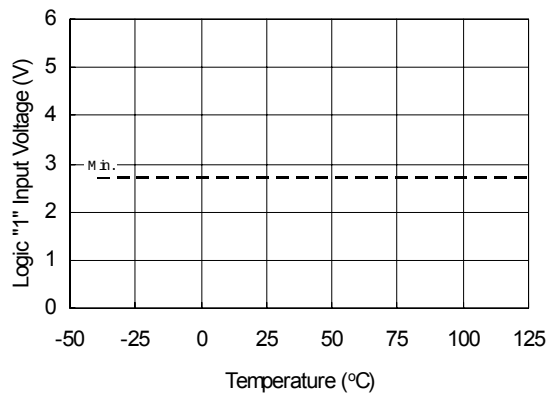


Figure 8A. Logic "1" Input Voltage vs. Temperature

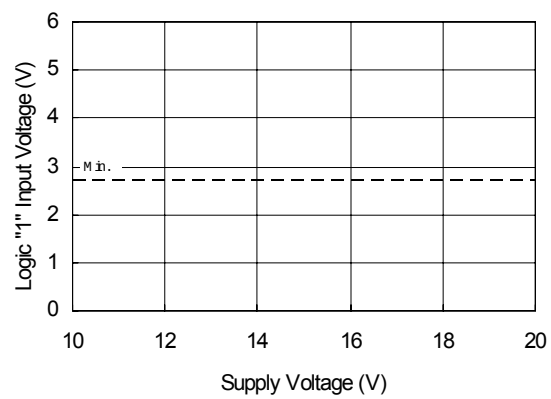


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

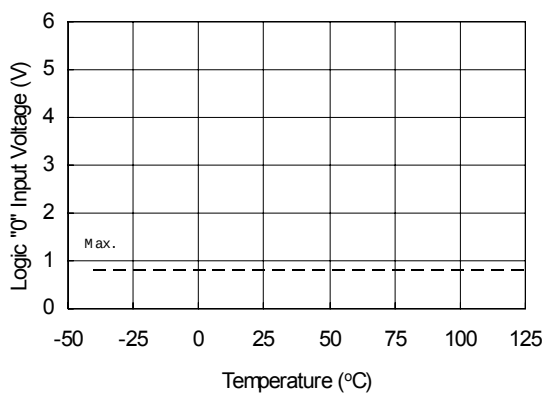


Figure 9A. Logic "0" Input Voltage vs. Temperature

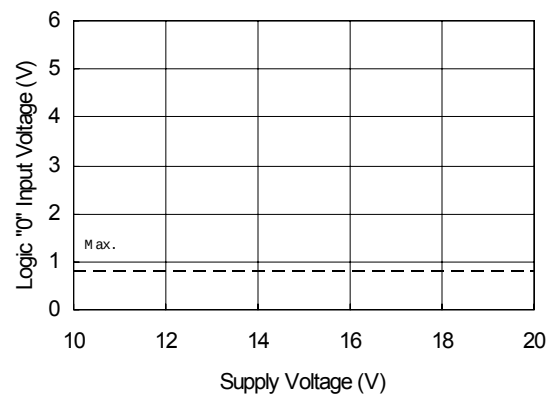


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

IR2181(4) (S) & (PbF)

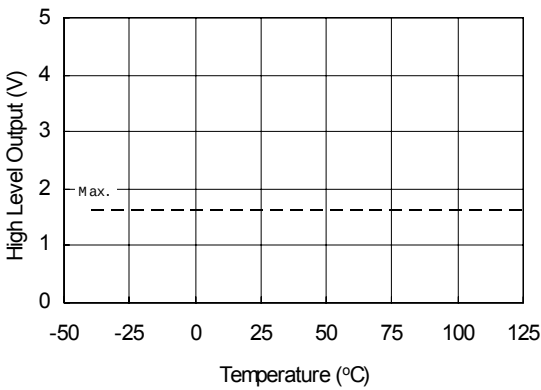


Figure 10A. High Level Output vs. Temperature

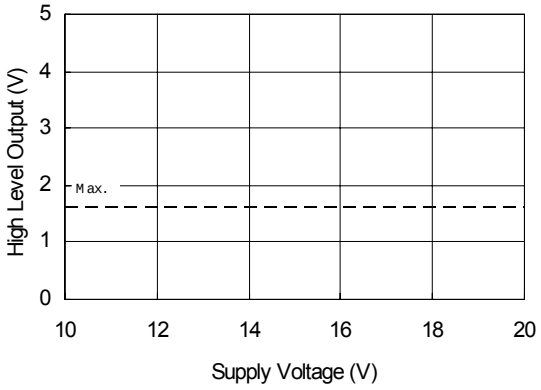


Figure 10B. High Level Output vs. Supply Voltage

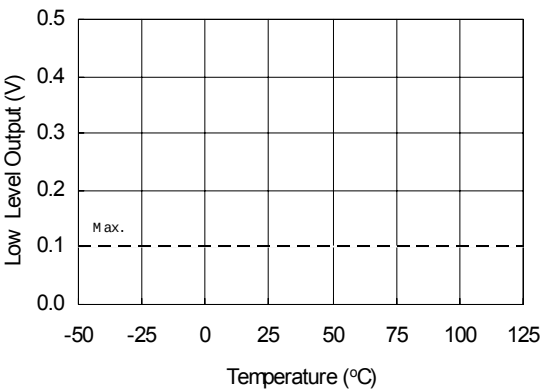


Figure 11A. Low Level Output vs. Temperature

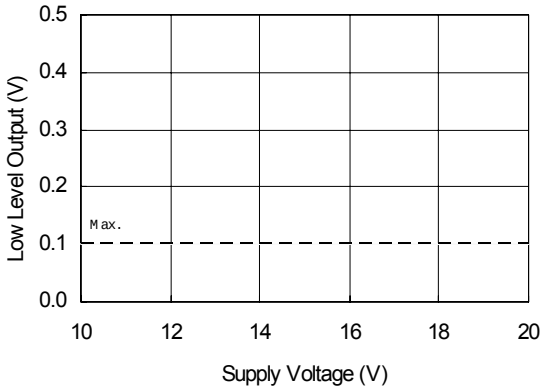


Figure 11B. Low Level Output vs. Supply Voltage

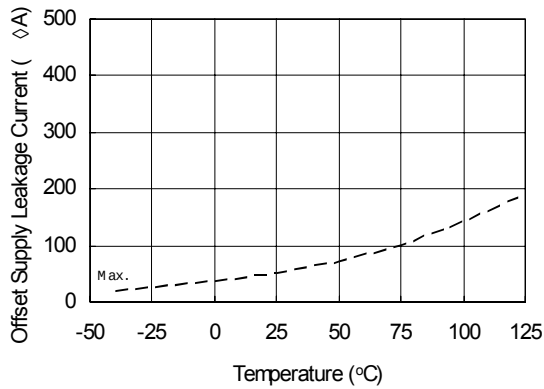


Figure 12A. Offset Supply Leakage Current vs. Temperature

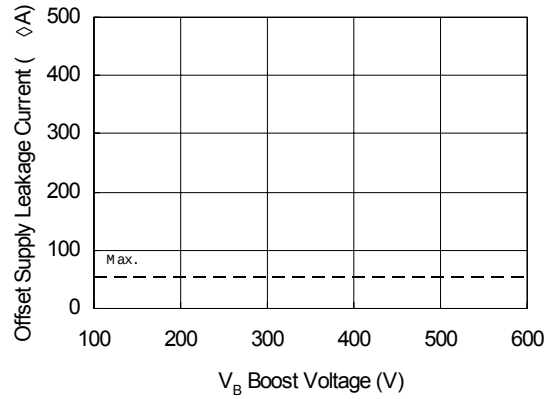


Figure 12B. Offset Supply Leakage Current vs. V_B Boost Voltage

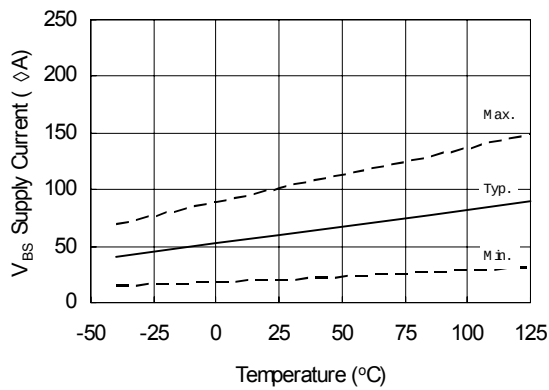


Figure 13A. V_{BS} Supply Current vs. Temperature

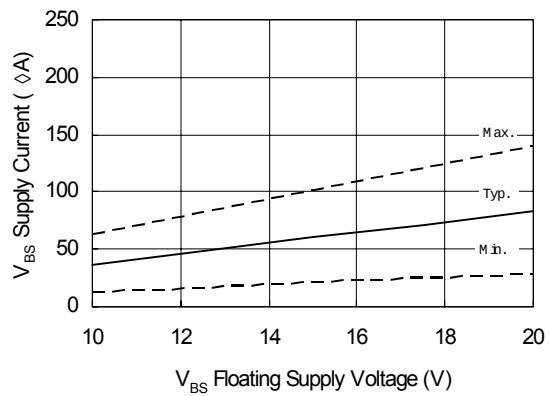


Figure 13B. V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

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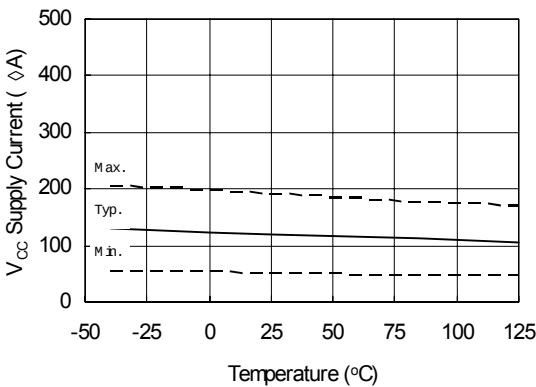


Figure 14A. V_{CC} Supply Current vs. V_{CC} Temperature

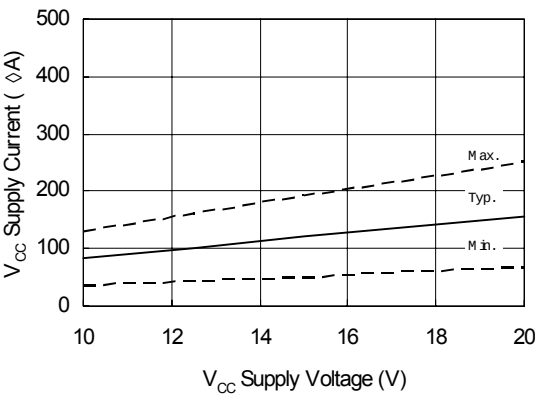


Figure 14B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

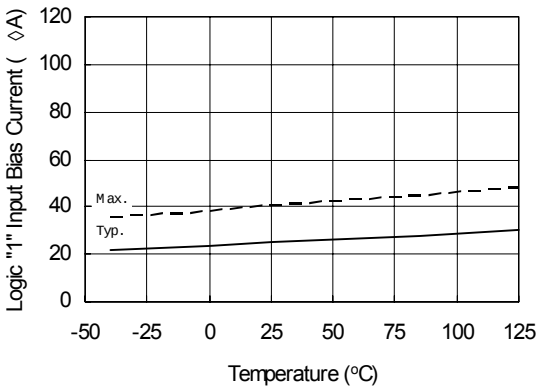


Figure 15A. Logic "1" Input Bias Current vs. Temperature

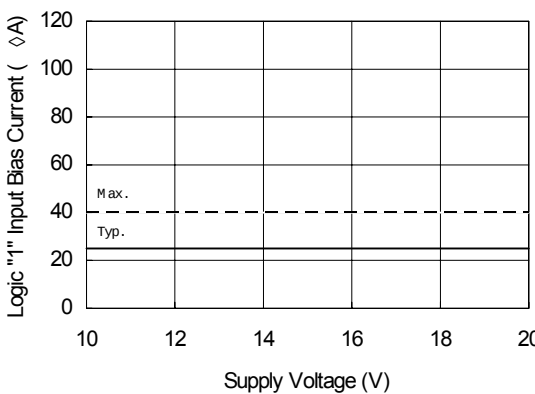


Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage

IR2181(4) (S) & (PbF)

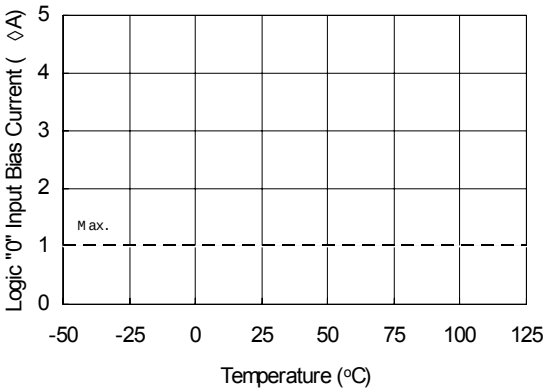


Figure 16A. Logic "0" Input Bias Current vs. Temperature

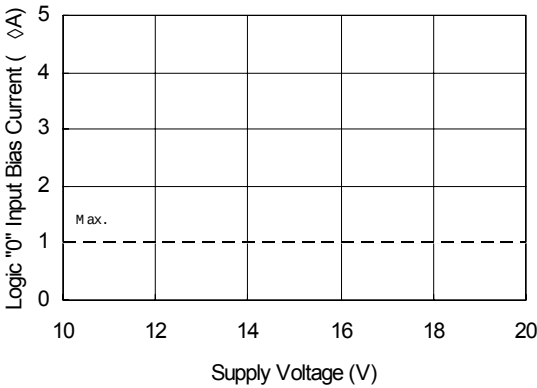


Figure 16B. Logic "0" Input Bias Current vs. Supply Voltage

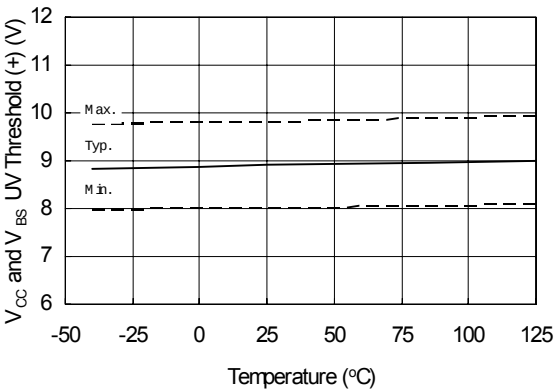


Figure 17. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

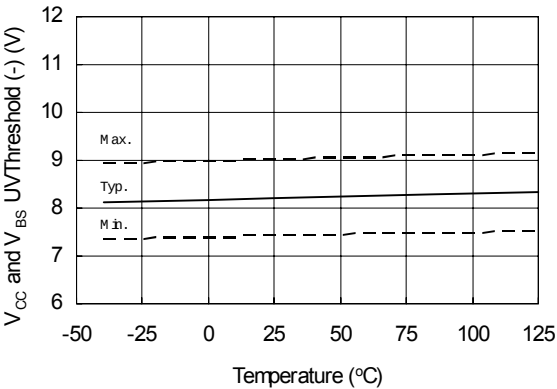


Figure 18. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

IR2181(4) (S) & (PbF)

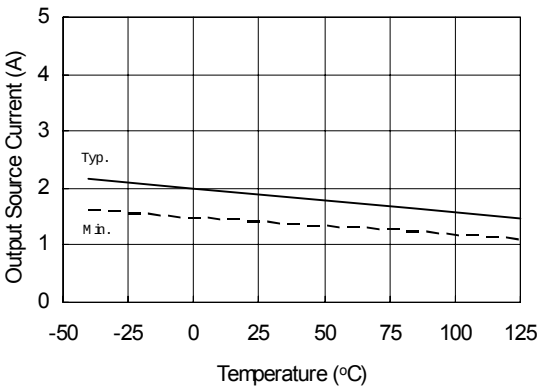


Figure 19A. Output Source Current vs. Temperature

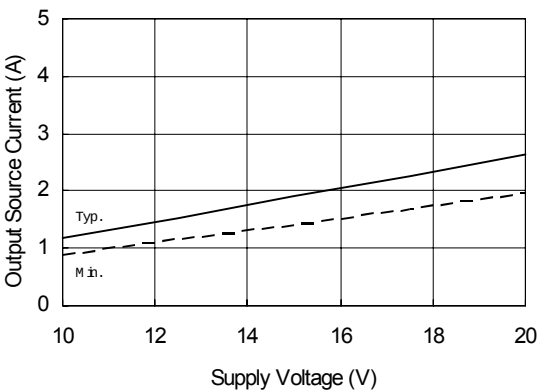


Figure 19B. Output Source Current vs. Supply Voltage

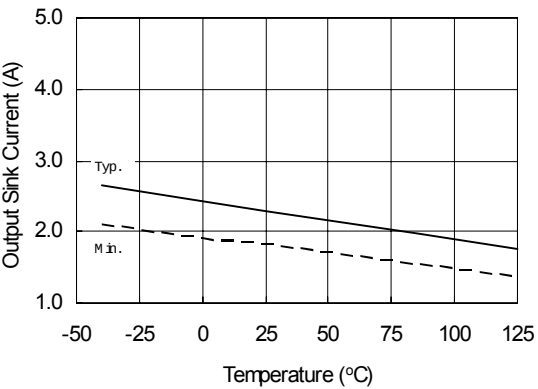


Figure 20A. Output Sink Current vs. Temperature

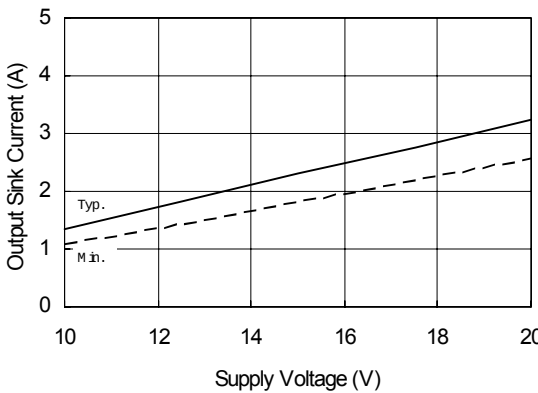


Figure 20B. Output Sink Current vs. Supply Voltage

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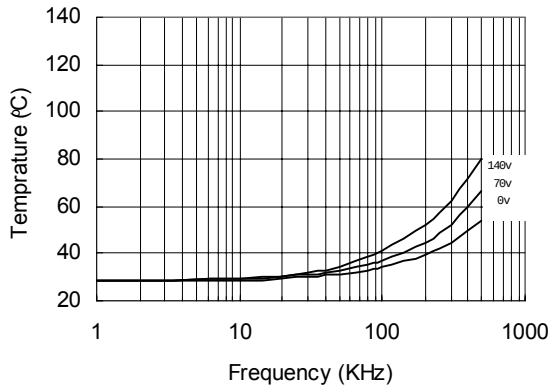


Figure 21. IR2181 vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega, V_{CC}=15V$

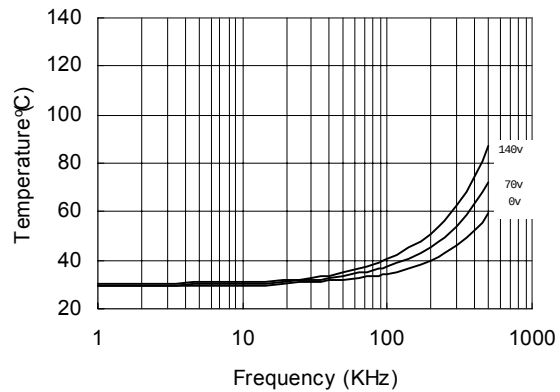


Figure 22. IR2181 vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega, V_{CC}=15V$

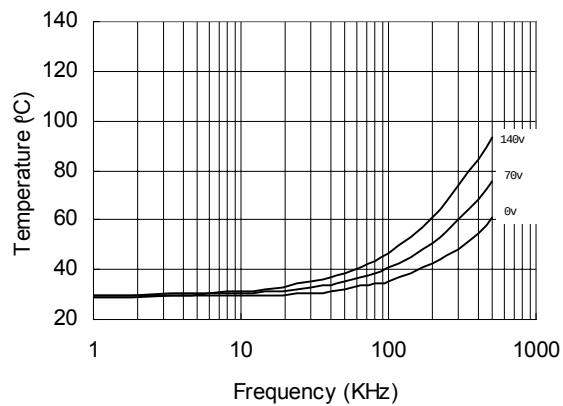


Figure 23. IR2181 vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega, V_{CC}=15V$

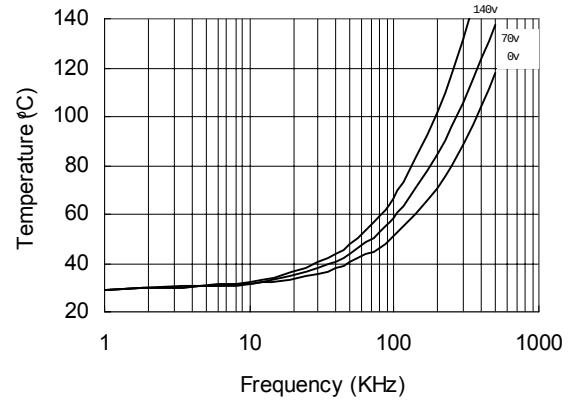


Figure 24. IR2181 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega, V_{CC}=15V$

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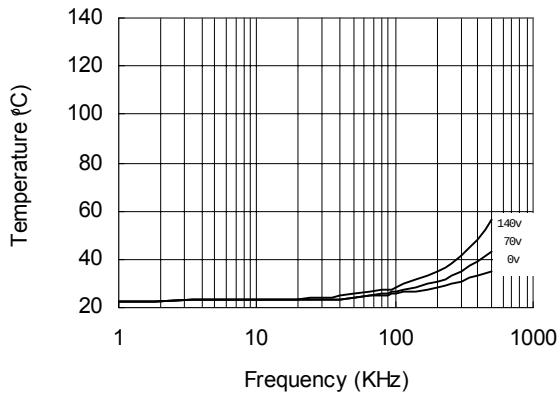


Figure 25. IR21814 vs. Frequency (IRFBC 20),
 $R_{gate}=33\Omega, V_{cc}=15V$

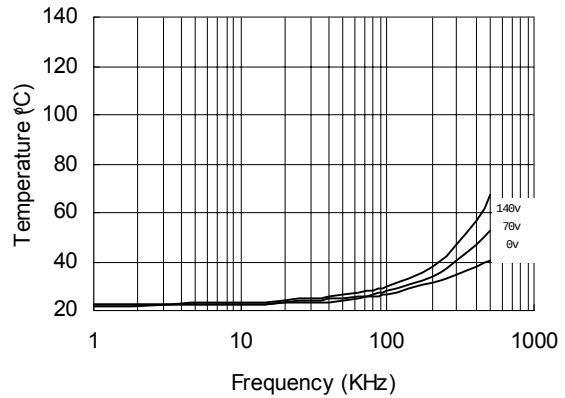


Figure 26. IR21814 vs. Frequency (IRFBC 30),
 $R_{gate}=22\Omega, V_{cc}=15V$

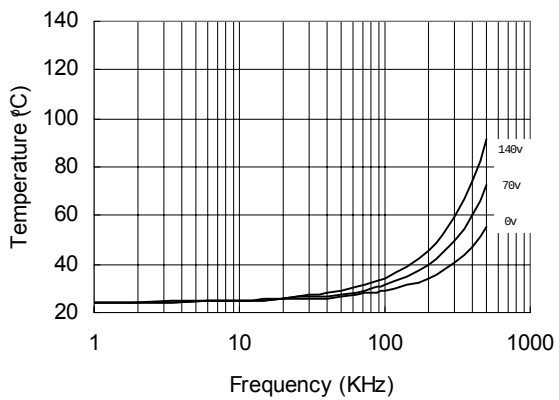


Figure 27. IR21814 vs. Frequency (IRFBC 40),
 $R_{gate}=15\Omega, V_{cc}=15V$

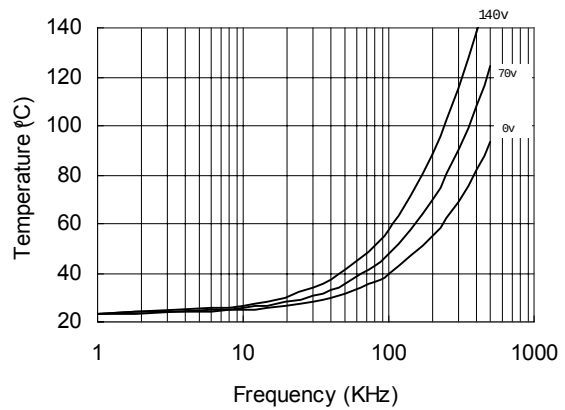


Figure 28. IR21814 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega, V_{cc}=15V$

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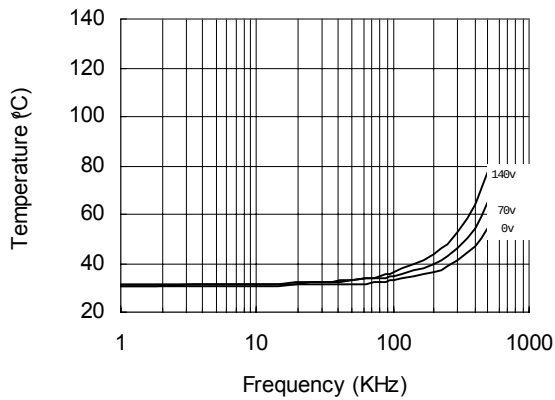


Figure 29. IR2181s vs. Frequency (IRFBC 20),
 $R_{gate}=33\Omega, V_{cc}=15V$

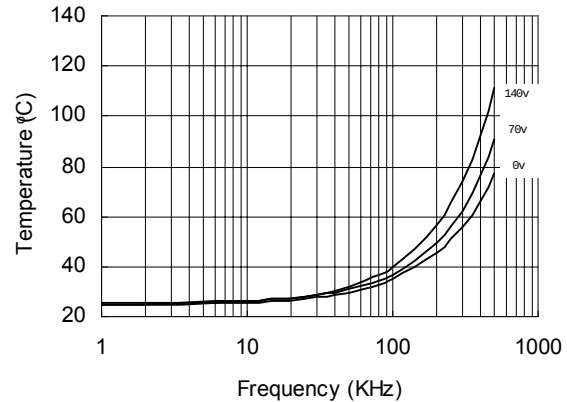


Figure 30. IR2181s vs. Frequency (IRFBC 30),
 $R_{gate}=22\Omega, V_{cc}=15V$

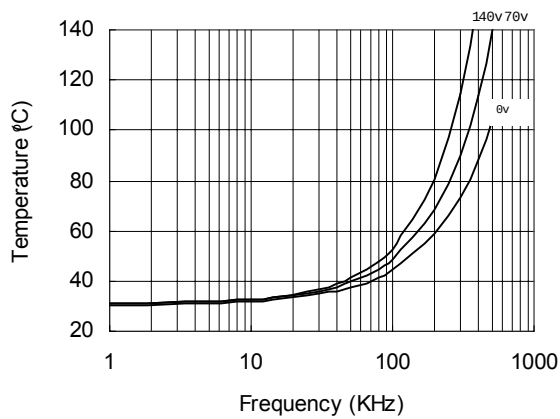


Figure 31. IR2181s vs. Frequency (IRFBC 40),
 $R_{gate}=15\Omega, V_{cc}=15V$

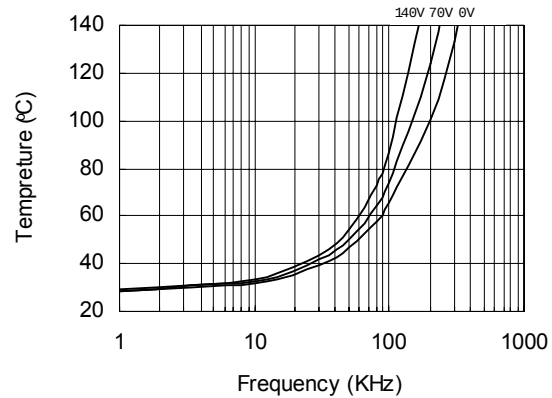


Figure 32. IR2181s vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega, V_{cc}=15V$

IR2181(4) (S) & (PbF)

International
IR Rectifier

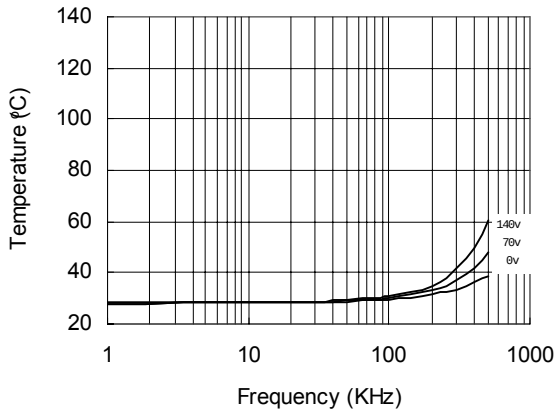


Figure 33. IR21814s vs. Frequency (RFBC 20),
 $R_{gate}=33\Omega, V_{cc}=15V$

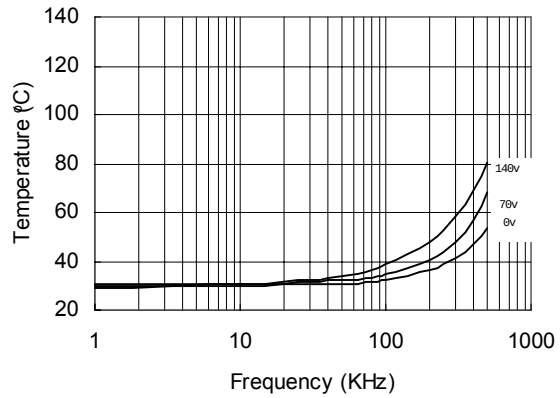


Figure 34. IR21814s vs. Frequency (RFBC 30),
 $R_{gate}=22\Omega, V_{cc}=15V$

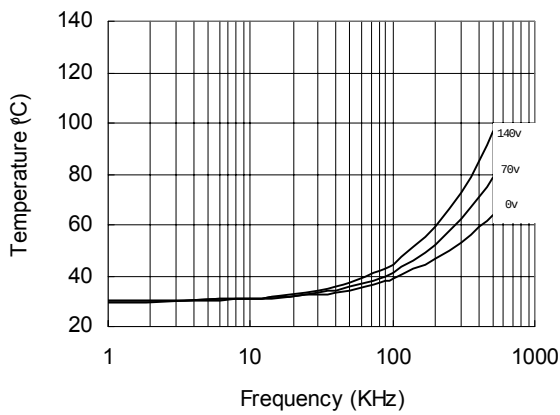


Figure 35. IR21814s vs. Frequency (RFBC 40),
 $R_{gate}=15\Omega, V_{cc}=15V$

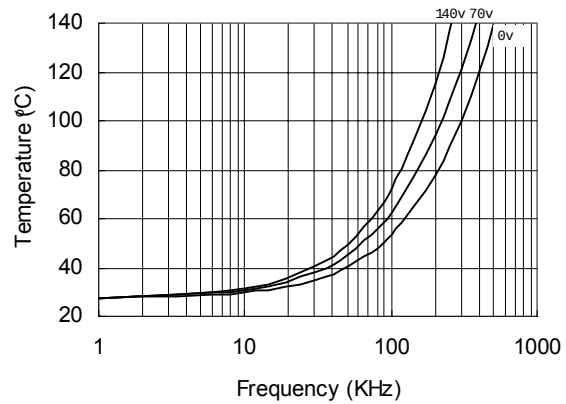
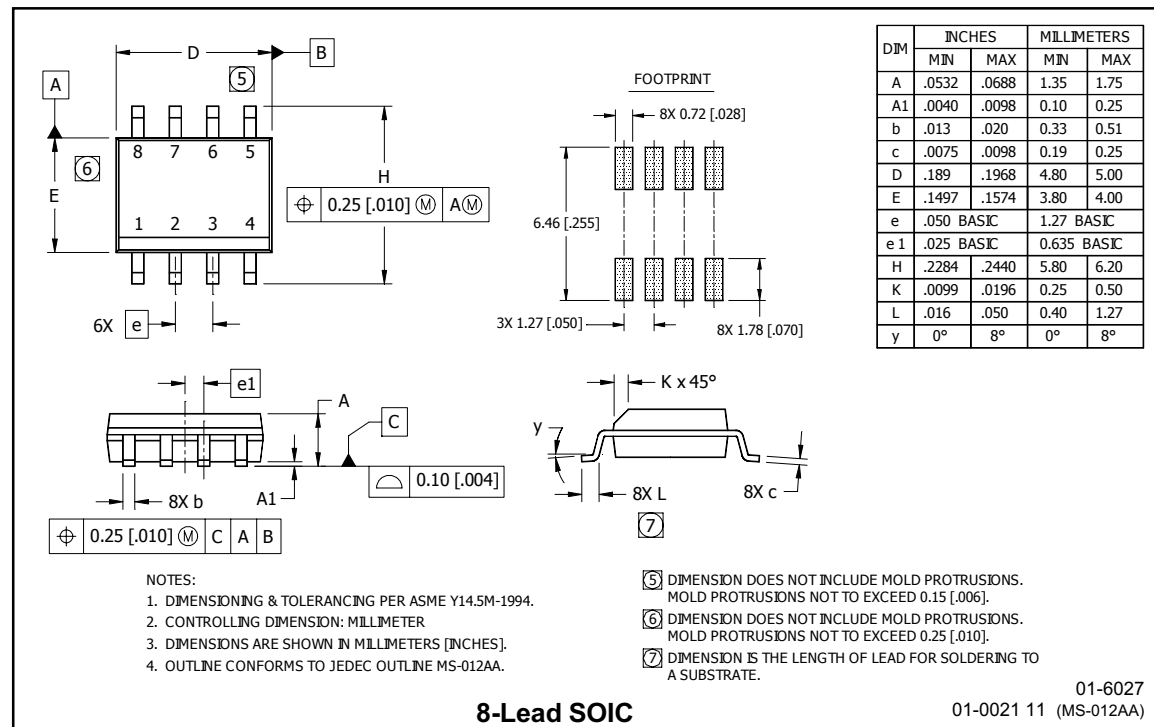
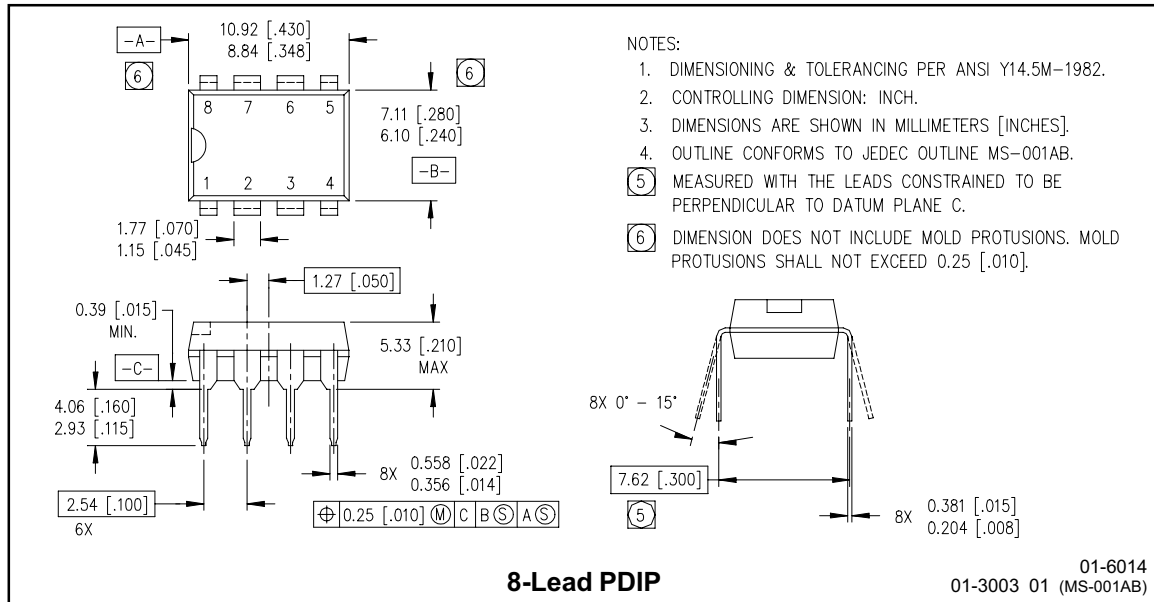


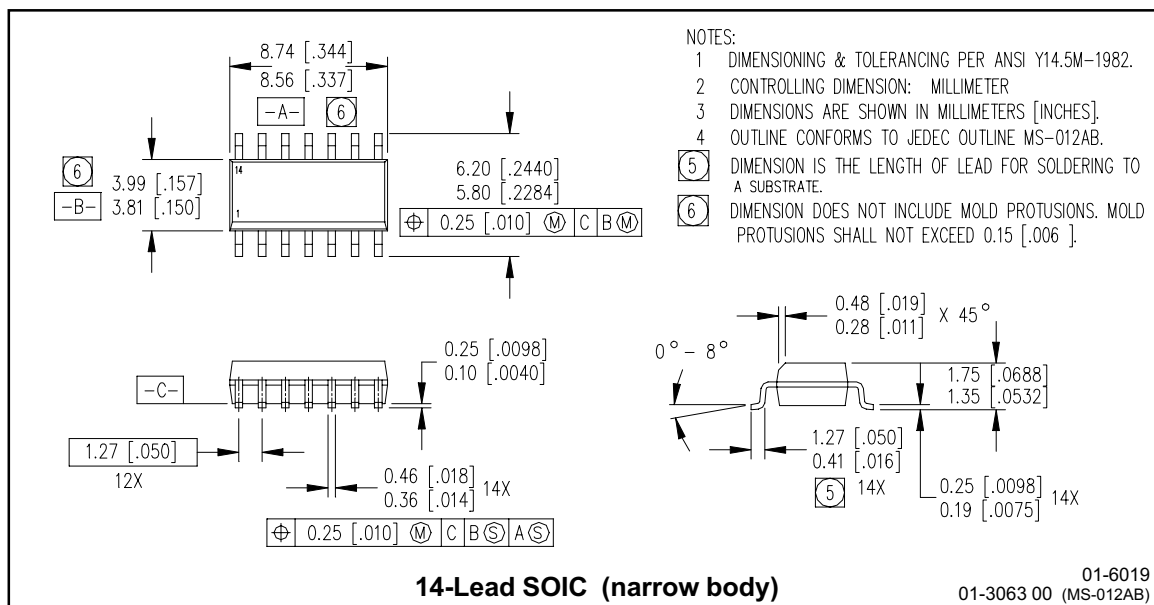
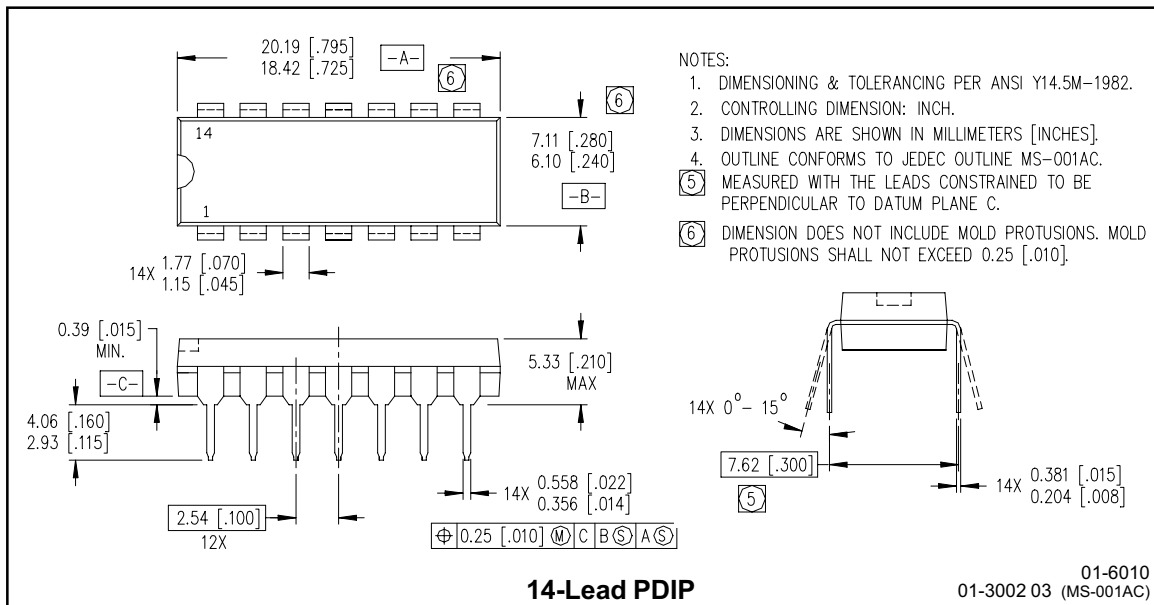
Figure 36. IR21814s vs. Frequency (RFPE50),
 $R_{gate}=10\Omega, V_{cc}=15V$

Case outlines

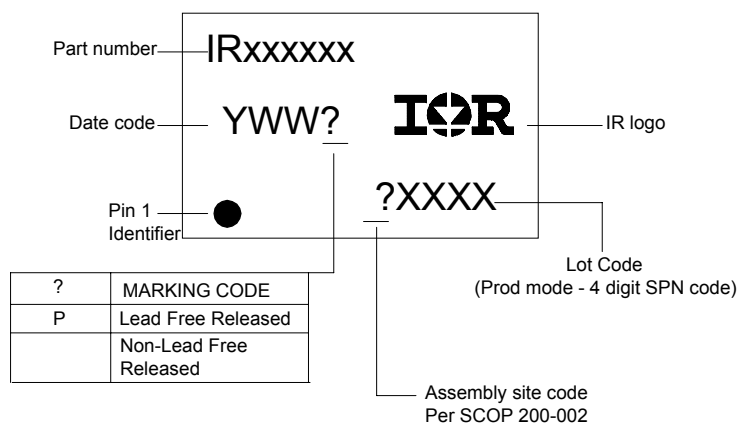


IR2181(4) (S) & (PbF)

International
IR Rectifier



LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2181 order IR2181
 8-Lead SOIC IR2181S order IR2181S
 14-Lead PDIP IR21814 order IR21814
 14-Lead SOIC IR21814 order IR21814S

Leadfree Part

8-Lead PDIP IR2181 order IR2181PbF
 8-Lead SOIC IR2181S order IR2181SPbF
 14-Lead PDIP IR21814 order IR21814PbF
 14-Lead SOIC IR21814 order IR21814SPbF