International
IOR Rectifier

IR3500A

DATA SHEET

XPHASE3™ VR11.0 & AMD PVID CONTROL IC

DESCRIPTION

The IR3500A Control IC combined with an *xPHASE3*™ Phase IC provides a full featured and flexible way to implement a complete VR11.0 or AMD PVID power solution. The Control IC provides overall system control and interfaces with any number of Phase ICs which each drive and monitor a single phase of a multiphase converter. The X*Phase3*™ architecture implements a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- 1 to X phase operation with matching Phase IC
- VID Select pin configures AMD 5 or 6 bit PVID, Intel VR11 with/out startup to 1.1V Boot voltage
- 0.5% overall system set point accuracy
- Programmable 250kHz to 9MHz Daisy-chain digital phase timing clock oscillator frequency provides a per phase switching frequency of 250kHz to 1.5MHz without external components
- Programmable Dynamic VID Slew Rate
- Programmable VID Offset or No Offset
- Programmable Load Line Output Impedance
- High speed error amplifier with wide bandwidth of 30MHz and fast slew rate of 12V/us
- Programmable converter current limit during soft start, hiccup with delay during normal operation
- Central over voltage detection with programmable threshold and communication to phase ICs
- Over voltage signal output to system with overvoltage detection during powerup and normal operation
- Detection and protection of open remote sense line and open control loop
- IC bias linear regulator control with programmable output voltage and UVLO
- Programmable VRHOT function monitors temperature of power stage through a NTC thermistor
- Remote sense amplifier with true converter voltage sensing and less than 50uA bias current
- Simplified PGOOD output provides indication of proper operation and avoids false triggering
- Small thermally enhanced 32L 5mm x 5mm MLPQ package
- RoHS Compliant

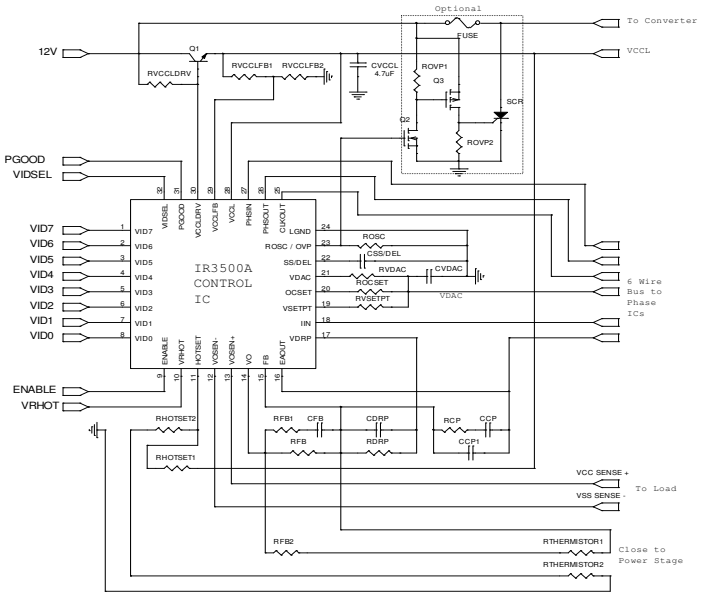

Figure 1 – Application Circuit

ORDERING INFORMATION

Device	Package	Order Quantity
IR3500A MTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
* IR3500A MPBF *Samples only	32 Lead MLPQ (5 x 5 mm body)	100 piece strips

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Operating Junction Temperature…….. 0°C to 150°C
Storage Temperature Range……-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1-8	VID7-0	7.5V	-0.3V	1mA	1mA
9	ENABLE	3.5V	-0.3V	1mA	1mA
10	VRHOT	7.5V	-0.3V	1mA	50mA
11	HOTSET	7.5V	-0.3V	1mA	1mA
12	VOSEN-	1.0V	-0.5V	5mA	1mA
13	VOSEN+	7.5V	-0.5V	5mA	1mA
14	VO	7.5V	-0.3V	5mA	25mA
15	FB	7.5V	-0.3V	1mA	1mA
16	EAOUT	7.5V	-0.3V	25mA	10mA
17	VDRP	7.5V	-0.3V	35mA	1mA
18	IIN	7.5V	-0.3V	100mA	1mA
19	VSETPT	3.5V	-0.3V	1mA	1mA
20	OCSET	7.5V	-0.3V	1mA	1mA
21	VDAC	3.5V	-0.3V	1mA	1mA
22	SS/DEL	7.5V	-0.3V	1mA	1mA
23	ROSC/OVP	7.5V	-0.3V	1mA	1mA
24	LGND	n/a	n/a	20mA	1mA
25	CLKOUT	7.5V	-0.3V	100mA	100mA
26	PHSOUT	7.5V	-0.3V	10mA	10mA
27	PHSIN	7.5V	-0.3V	1mA	1mA
28	VCCL	7.5V	-0.3V	1mA	20mA
29	VCCLFB	3.5V	-0.3V	1mA	1mA
30	VCCLDRV	10V	-0.3V	1mA	50mA
31	PGOOD	VCCL + 0.3V	-0.3V	1mA	20mA
32	VIDSEL	7.5V	-0.3V	5mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

4.75V ≤ V_{CCL} ≤ 7.5V, -0.3V ≤ VOSEN- ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, 7.75KΩ ≤ R_{OSC} ≤ 50.0 KΩ

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. $C_{SS/DEL}$ = 0.1µF +/-10%.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy (Deviation from Tables 2 & 4 per test circuit in Fig.3 and Table 3 per test circuit in Fig.2)	VID ≥ 1V	-0.5		0.5	%
	0.8V ≤ VID < 1V	-5		5	mV
	0.5V ≤ VID < 0.8V	-8		8	mV
	0.3V ≤ VID < 0.5V	-8		8	mV
Source & Sink Currents	Include OCSET and VSETPT currents	30	44	58	µA
VR11 VIDx Input Threshold	Float VIDSEL or tie VIDSEL to VCCL	500	600	700	mV
AMD VIDx Input Threshold	R(VIDSEL) = 6.49kΩ or connect VIDSEL to LGND.	0.85	1.00	1.15	V
VR11 VIDx Input Bias Current	Float VIDSEL, or connect VIDSEL to VCCL or LGND. 0V≤V(VIDx)≤2.5V.	-1	0	1	µA
AMD 6-bit VIDx Pull-down Resistance	R(VIDSEL) = 6.49kΩ	100	175	250	kΩ
VIDx OFF State Blanking Delay	Measure time till PGOOD drives low	0.5	1.3	2.1	µs
VIDSEL Threshold between AMD 5-bit VID and AMD 6-bit VID	Note 3.	0.48	0.6	0.75	V
VIDSEL Threshold between AMD 6-bit VID and VR11 with Boot Voltage	Relative to VIDSEL float voltage. Note 3.	84	87	90	%
VIDSEL Threshold between VR11 with/out Boot Voltage	Note 3.	2.97	3.30	3.63	V
VIDSEL Float Voltage	Relative to VIDSEL Threshold between VR11 with/out Boot Voltage	77	83	89	%
VIDSEL Pull-up Resistance		3.0	4.0	5.0	KΩ
Oscillator					
ROSC Voltage		0.570	0.595	0.620	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT Frequency	R_{OSC} = 50.0 KΩ	225	250	275	kHz
PHSOUT Frequency	R_{OSC} = 24.5 KΩ	450	500	550	kHz
PHSOUT Frequency	R_{OSC} = 7.75 KΩ	1.35	1.50	1.65	MHz
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay (TD1)		1.0	2.9	3.5	Ms
Soft Start Time (TD2)	To reach 1.1V	0.8	2.2	3.25	Ms
VID Sample Delay (TD3)		0.3	1.2	3.0	Ms
PGOOD Delay (TD4 + TD5)		0.5	1.2	2.3	Ms
OC Delay Time	V(IIN) – V(OCSET) = 500 mV	75	125	300	us
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.7	1.4	1.9	V
Charge Current		35.0	52.5	70.0	µA
Discharge Current		2.5	4.5	6.5	µA
Charge/Discharge Current Ratio		10	12	16	µA/µA
Charge Voltage			3.75		V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL rising		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL falling		110		mV
Delay Comparator Hysteresis			30		mV
VID Sample Delay Comparator Threshold			3.0		V
Discharge Comp. Threshold		150	200	275	mV
Remote Sense Differential Amplifier					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	-3	0	3	mV
Source Current	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	0.5	1.0	1.7	mA
Sink Current	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V	2	12	18	mA
Slew Rate	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.6V Note1	2	4	8	V/us
VOSEN+ Bias Current	0.5 V < V(VOSEN+) < 1.6V		30	50	uA
VOSEN- Bias Current	-0.3V ≤ VOSEN- ≤ 0.3V, All VID Codes		30	50	uA
VOSEN+ Input Voltage Range	V(VCCL)=7V			5.5	V
High Voltage	V(VCCL) – V(VO)		0.5	1	V
Low Voltage	V(VCCL)=7V			250	mV
Error Amplifier					
Input Offset Voltage	Measure V(FB) – V(VSETPT). Note 2	-1	0	1	mV
FB Bias Current		-1	0	1	µA
VSETPT Bias Current	ROSC= 24.5 KΩ	23.00	24.25	25.50	µA
DC Gain	Note 1	100	110	120	dB
Bandwidth	Note 1	20	30	40	MHz
Slew Rate	Note 1	7	12	20	V/µs
Sink Current		0.40	0.85	1.00	mA
Source Current		5	8	12	mA
Minimum Voltage			120	250	mV
Maximum Voltage	Measure V(VCCL) – V(EAOUT)	500	780	950	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUT) = V(VCCL) to PGOOD = low.		8		Pulses
Enable Input					
VR 11 Threshold Voltage	ENABLE rising	825	850	875	mV
VR 11 Threshold Voltage	ENABLE falling	775	800	825	mV
VR 11 Hysteresis		25	50	75	mV
AMD Threshold Voltage	ENABLE rising	1.1	1.2	1.3	V
AMD Threshold Voltage	ENABLE falling	1.05	1.14	1.23	V
AMD Hysteresis		30	50	80	mV
Bias Current	0V ≤ V(ENABLE) ≤ 3.3V	-5	0	5	µA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 3.3V	-30	-13	0	mV
OCSET Bias Current	ROSC= 24.5 KΩ	23.25	24.50	25.75	µA
Over-Current Delay Counter	ROSC = 7.75 KΩ (PHSOUT=1.5MHz)		4096		Cycle
Over-Current Delay Counter	ROSC = 15.0 KΩ (PHSOUT=800kHZ)		2048		Cycle
Over-Current Delay Counter	ROSC = 50.0 KΩ (PHSOUT=250kHz)		1024		Cycle
Over-Current Limit Amplifier					
Input Offset Voltage		-10	0	10	mV
Transconductance	Note 1	0.50	1.00	1.75	mA/V
Sink Current		35	55	75	uA
Unity Gain Bandwidth		0.75	2.00	3.00	kHz
Over Voltage Protection (OVP) Comparators					
Threshold at Power-up		1.60	1.73	1.83	V
Threshold during Normal Operation	Compare to V(VDAC)	110	130	150	mV
OVP Release Voltage during Normal Operation	Compare to V(VDAC)	-13	3	20	mV
Threshold during Dynamic VID down		1.70	1.73	1.75	V
Dynamic VID Detect Comparator Threshold		25	50	75	mV
Propagation Delay to IIN	Measure time from V(VO) > V(VDAC) (250mV overdrive) to V(IIN) transition to > 0.9 * V(VCCL).		90	180	ns
IIN Pull-up Resistance			5	15	Ω
Propagation Delay to OVP	Measure time from V(VO) > V(VDAC) (250mV overdrive) to V(ROSC/OVP) transition to >1V.		90	180	ns
OVP High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0		1.2	V
OVP Power-up High Voltage	V(VCCLDRV)=1.8V. Measure V(VCCL)-V(ROSC/OVP)	0		0.2	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDRP Buffer Amplifier					
Input Offset Voltage	V(VDRP) – V(IIN), 0.5V ≤ V(IIN) ≤ 3.3V	-5	3	11	mV
Source Current	0.5V ≤ V(IIN) ≤ 3.3V	2		30	mA
Sink Current	0.5V ≤ V(IIN) ≤ 3.3V	0.2	0.4	0.6	mA
Unity Gain Bandwidth	Note 1		8		MHz
Slew Rate	Note 1		4.7		V/µs
IIN Bias Current		-1	0	1	µA
PGOOD Output					
Output Voltage	I(PGOOD) = 4mA		150	300	mV
Leakage Current	V(PGOOD) = 5.5V		0	10	µA
Under Voltage Threshold-VO decreasing	Reference to VDAC	-380	-330	-280	mV
Under Voltage Threshold-VO increasing	Reference to VDAC	-315	-265	-215	mV
Under Voltage Threshold Hysteresis		25	60	95	mV
VCCL_DRV Activation Threshold	I(PG)=4mA, V(PG)<300mV, V(VCCL)=0	1	2	3.6	V
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(VO) < [V(VOSEN+) – V(LGND)] / 2	35	60	85	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	87.5	90.0	92.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(VO) = 100mV	200	500	700	uA
VRHOT Comparator					
Threshold Voltage		1.584	1.600	1.616	V
HOTSET Bias Current		-1	0	1	µA
Hysteresis		75	100	125	mV
Output Voltage	I(VRHOT) = 30mA		150	400	mV
VRHOT Leakage Current	V(VRHOT) = 5.5V		0	10	µA
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.19	1.23	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	30		mA
UVLO Start Threshold	Compare to V(VCCL)	91	93	99	%
UVLO Stop Threshold	Compare to V(VCCL)	83	87	91	%
Hysteresis	Compare to V(VCCL)	7	8.25	9.5	%
General					
VCCL Supply Current		3.0	6.5	10.0	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amplifier input offset errors
Note 3: See VIDSEL Functionality Table

SYSTEM SET POINT TEST

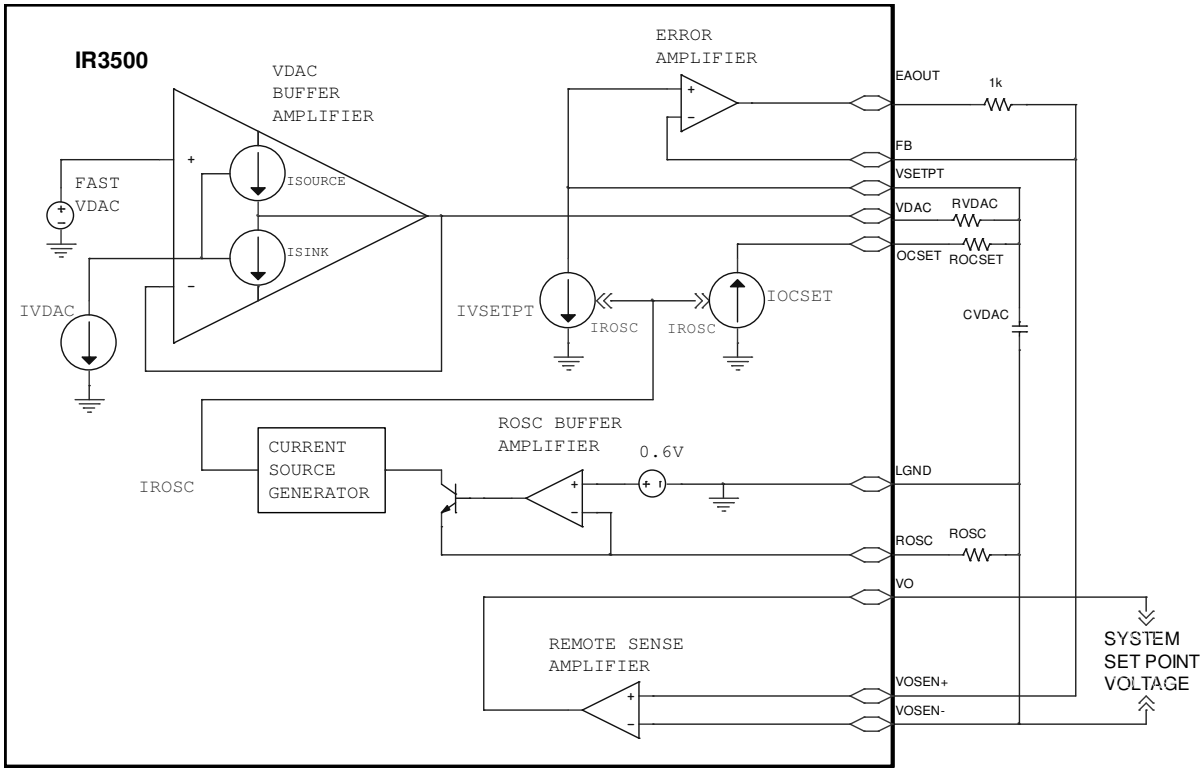

Figure 2 - System Set Point Test Circuit for VR11 VID

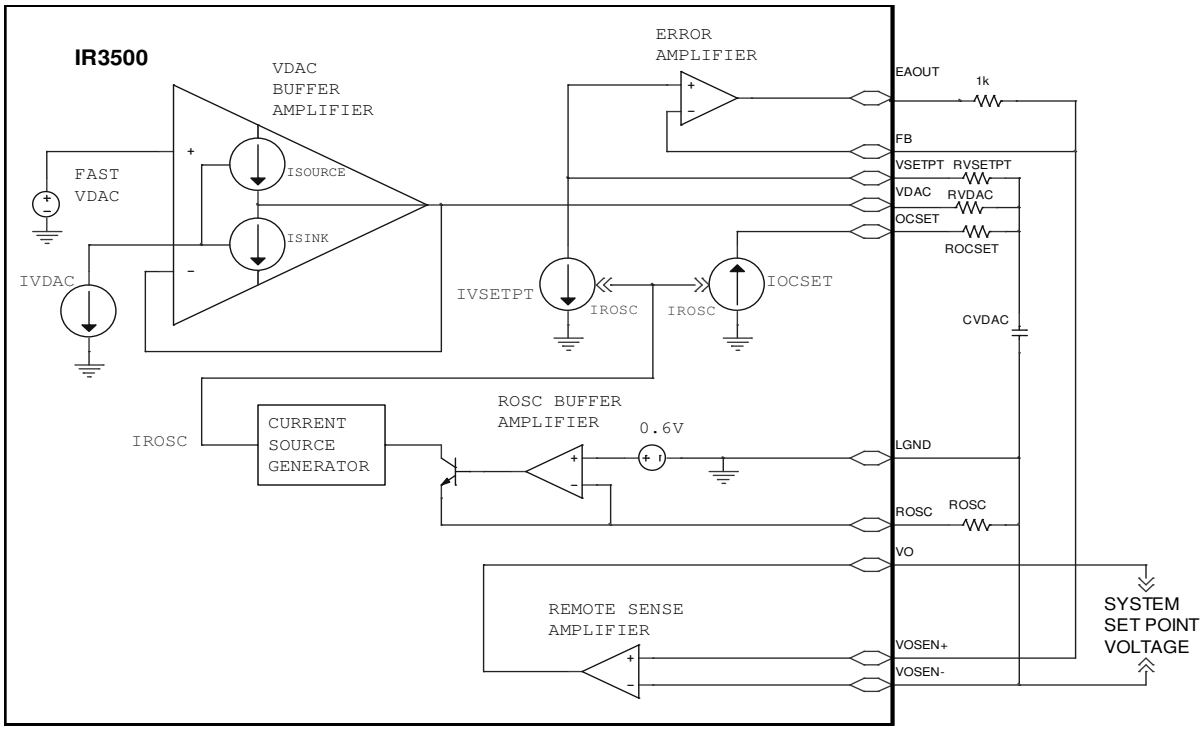

Figure 3 - System Set Point Test Circuit for AMD VIDs (VDAC shifted +50 mV)

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-8	VID7-0	Inputs to VID D to A Converter.
9	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. Do not float this pin as the logic state will be undefined.
10	VRHOT	Open collector output of the VRHOT comparator which drives low if HOTSET pin voltage is lower than 1.6V. Connect external pull-up.
11	HOTSET	A resistor divider including thermistor senses the temperature, which is used for VRHOT comparator.
12	VOSEN-	Remote sense amplifier input. Connect to ground at the load.
13	VOSEN+	Remote sense amplifier input. Connect to output at the load.
14	VO	Remote sense amplifier output.
15	FB	Inverting input to the error amplifier.
16	EAOUT	Output of the error amplifier.
17	VDRP	Buffered IIN signal. Connect external RC network to FB to program converter output impedance.
18	IIN	Average current input from the phase IC(s). This pin is also used to communicate over voltage condition to phase ICs.
19	VSETPT	Error amplifier non-inverting input. Converter output voltage can be decreased from the VDAC voltage with an external resistor connected between VDAC and this pin (there is an internal sink current at this pin).
20	OCSET	Programs the constant converter output current limit and hiccup over-current thresholds through an external resistor tied to VDAC and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC to program the threshold higher than the possible signal into the IIN pin from the phase ICs but no greater than VCCL – 2V (do not float this pin as improper operation will occur).
21	VDAC	Regulated voltage programmed by the VID inputs. Connect external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amp.
22	SS/DEL	Programs converter startup and over current protection delay timing. It is also used to compensate the constant output current loop during soft start. Connect an external capacitor to LGND to program.
23	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency and OCSET, VSETPT and VDAC bias currents. Oscillator frequency equals switching frequency per phase. The pin is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
24	LGND	Local Ground for internal circuitry and IC substrate connection.
25	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
27	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
28	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND.
29	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by the resistor divider connected to VCCL.
30	VCCLDRV	Output of the VCCL regulator error amplifier to control external transistor. The pin senses 12V power supply through a resistor.
31	VRRDY	Open collector output that drives low during startup and under any external fault condition. Connect external pull-up.
32	VIDSEL	The pin configures VIDs for AMD 6-bit, Intel VR11 8-bit with 1.1V Boot voltage, Intel VR11 8-bit without 1.1V Boot voltage or AMD 5-bit Opteron.

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *XPhase3*™ architecture is shown in Figure 4. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. Input voltage is sensed in phase ICs and feed-forward control is realized. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

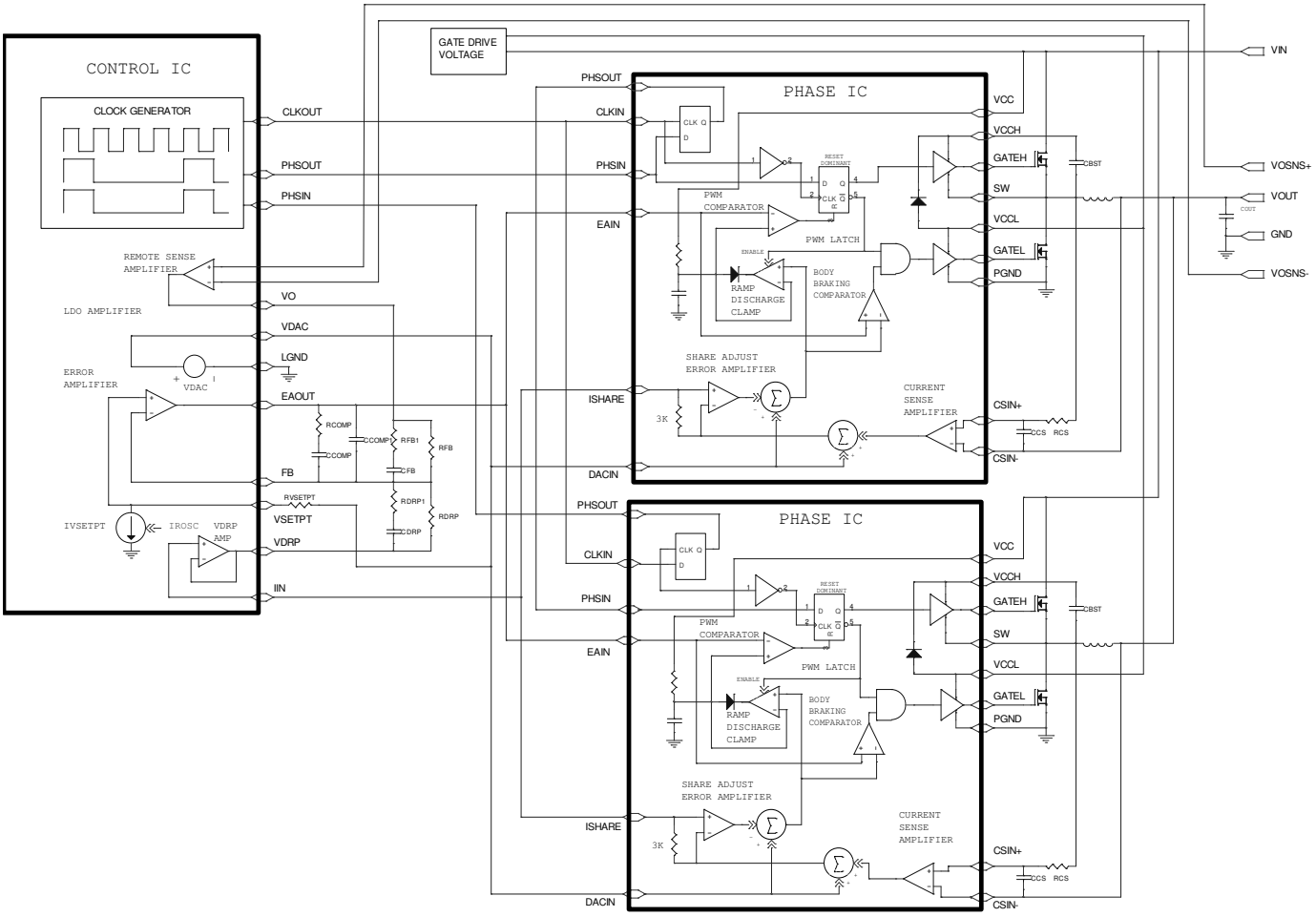

Figure 4 - PWM Block Diagram

Frequency and Phase Timing Control

The oscillator and system clock frequency is programmable from 250kHz to 9MHZ by an external resistor (ROSC). The control IC system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the

second phase IC, etc. and PHSOUT of the last phase IC is connected back to PHSIN of the control IC. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 5 shows the phase timing for a four phase converter. The switching frequency is set by the resistor ROSC as shown in Figure 23. The clock frequency equals the number of phase times the switching frequency.

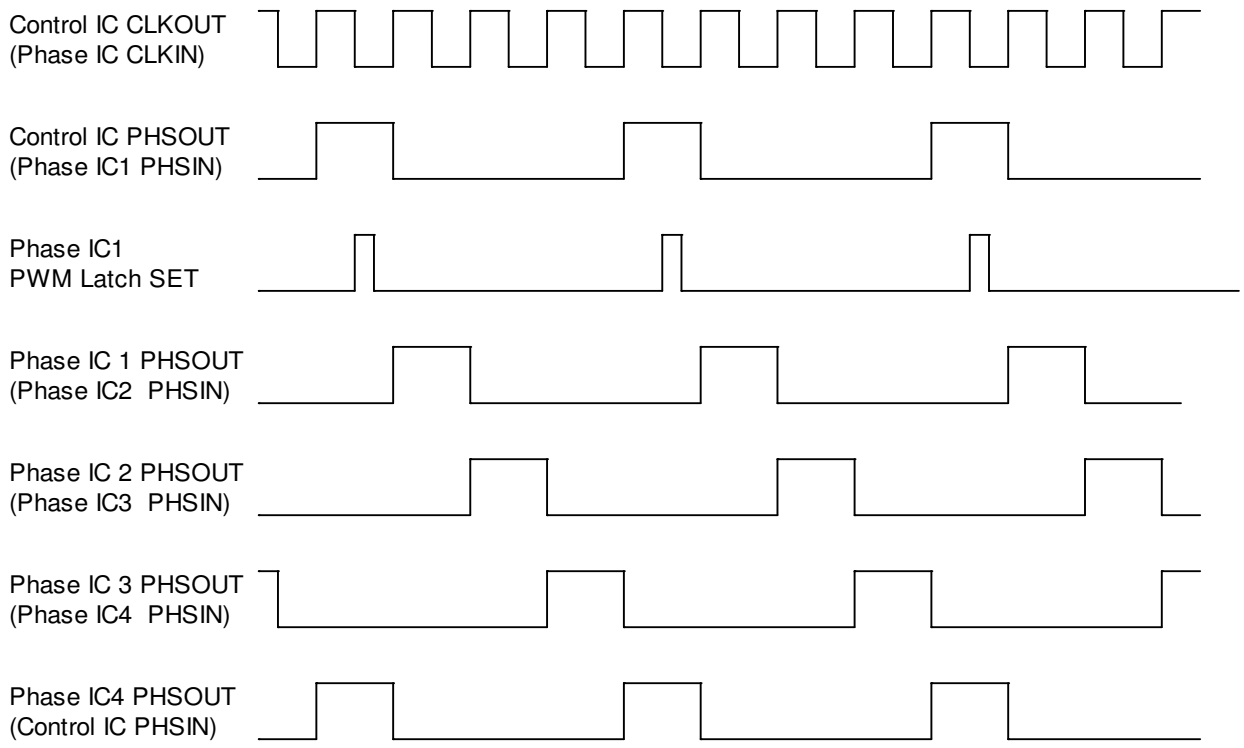

Figure 5 - Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is set; the PWM ramp voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWM ramp voltage exceeds the error amplifier's output voltage the PWM latch is reset. This turns off the high side driver, then turns on the low side driver after the non-overlap time, and activates the ramp discharge clamp. The ramp discharge clamp quickly discharges the PWM ramp capacitor to the output voltage of the share adjust amplifier in the phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC. Figure 6 depicts PWM operating waveforms under various conditions

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The error amplifier is a high speed amplifier with 110 dB of open loop gain. It is not unity gain stable.

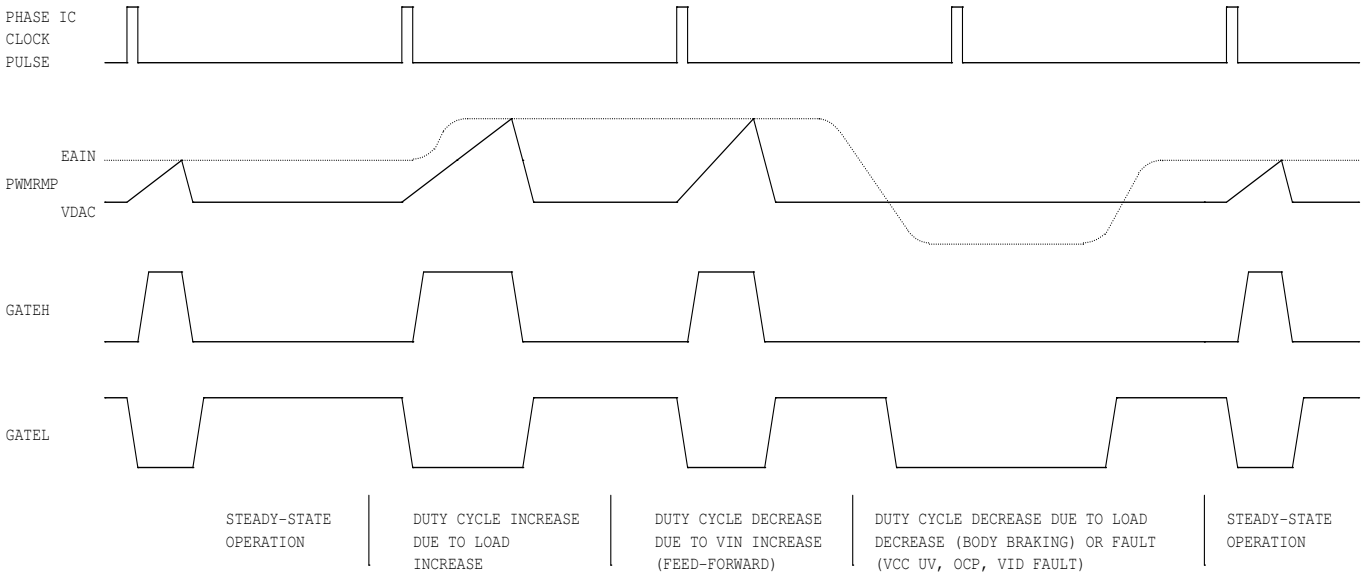


Figure 6 - PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented method is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the output voltage of the share adjust amplifier in the phase IC, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 7. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L+sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (RL). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of RL was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

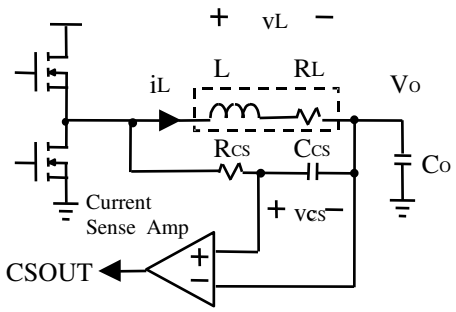


Figure 7 - Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 7. Its gain is nominally 32.5 and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sharing performance, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on ISHARE bus with a frequency of fsw / 896 in a multiphase architecture.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3500A THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3500A is shown in Figure 8, and specific features are discussed in the following sections.

VID Control

The AMD 6-bit VID, VR11 8-bit VID, and AMD Opteron 5-bit VID are shown in Tables 2 to 4 respectively, and are selected by different connections of VIDSEL pin shown in Table 1. The VID pins require an external bias voltage and should not be floated. The VID input comparators monitor the VID pins and control the Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. The VDAC voltage, input offsets of error amplifier and remote sense differential amplifier are post-package trimmed to provide 0.5% **system set-point** accuracy. The actual VDAC voltage does not determine the system accuracy, which has a wider tolerance. **VIDs of less than 0.5V are not supported.**

The IR3500A can accept changes in the VID code while operating and vary the DAC voltage accordingly. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and LGND pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

Adaptive Voltage Positioning

Adaptive voltage positioning is needed to reduce the output voltage deviations during load transients and the power dissipation of the load at heavy load. The circuitry related to voltage positioning is shown in Figure 9. The output voltage is set by the reference voltage VSETPT at the positive input to the error amplifier. This reference voltage can be programmed to have a constant DC offset bellow the VDAC by connecting RSETPT between VDAC and VSETPT. The IVSETPT is controlled by the ROSC as shown in Figure 24.

The voltage at the VDRP pin is a buffered version of the share bus IIN and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor R_{DRP}. Since the error amplifier will force the loop to maintain FB to be equal to the VSETPT, an additional current will flow into the FB pin equal to (VDRP-VSETPT) / R_{DRP}. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor R_{FB}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{DRP} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor should be used for inductor DCR temperature compensation. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 10. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

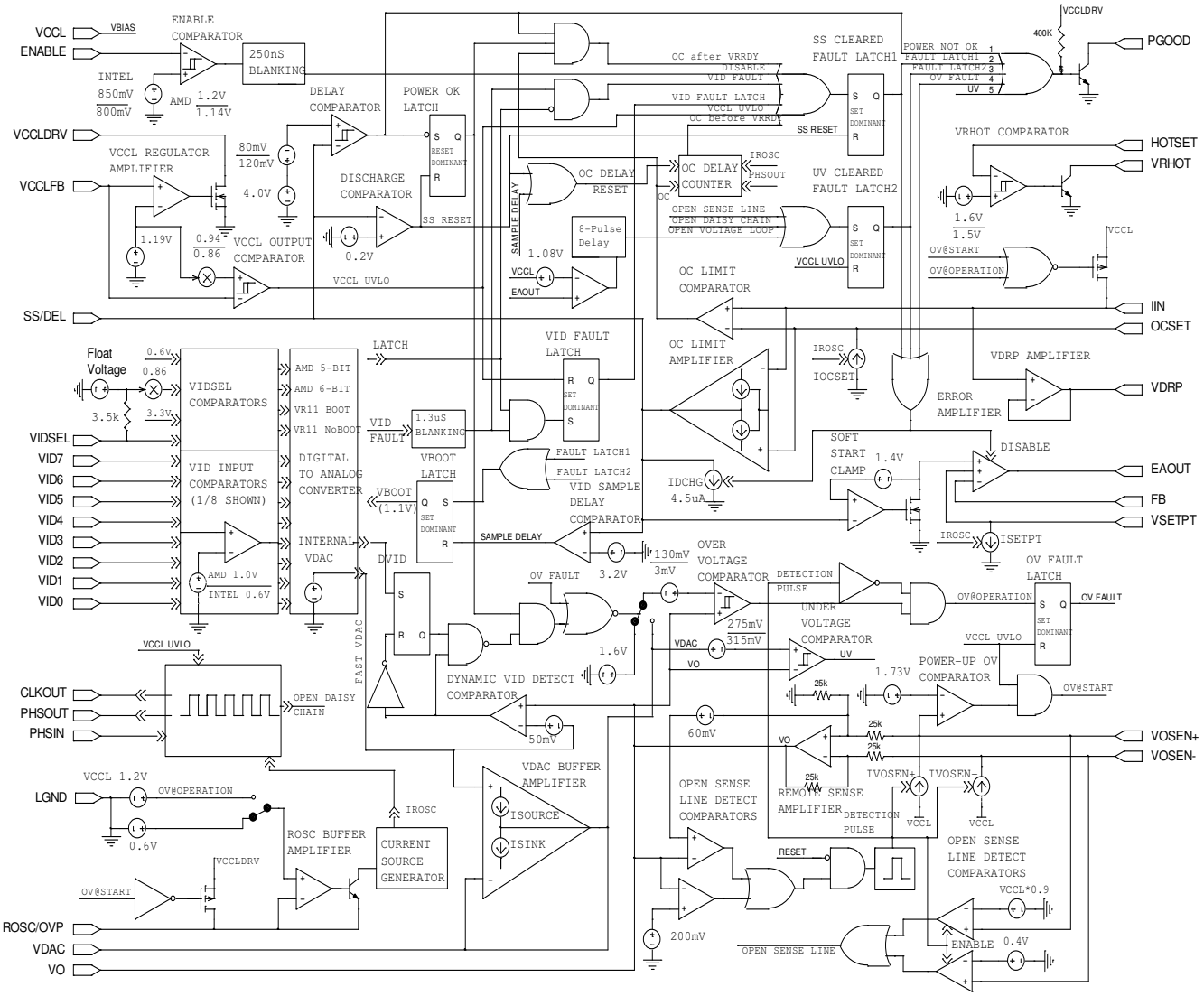


Figure 8 - Block Diagram

TABLE 1 - VIDSEL FUNCTIONALITY

VIDSEL Connection	VID Table	1.1V Boot Voltage during soft start?	Ignore VID Fault during soft start?	VID Fault Latch?
LGND (<0.5V)	AMD 5-BIT OPTERON	NO	NO	NO
6.49 kΩ to GND (0.7V to 83% of FLOAT)	AMD 6-BIT	NO	NO	NO
FLOAT (typ. 83% of VR11w/wo boot Threshold)	VR11 8-BIT	YES	YES	YES
VCCL (4.5V-7V)	VR11 8-BIT	NO	NO	NO

TABLE 2 - AMD 6-BIT VID TABLE

VID5	VID4	VID3	VID2	VID1	VID0	Vout (V)		VID5	VID4	VID3	VID2	VID1	VID0	Vout(V)
0	0	0	0	0	0	1.5500		1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250		1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000		1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750		1	0	0	0	1	1	0.7250
0	0	0	1	0	0	1.4500		1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250		1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000		1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750		1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500		1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250		1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000		1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750		1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500		1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250		1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000		1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750		1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500		1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250		1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000		1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750		1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500		1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250		1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000		1	1	0	1	1	0	n/a
0	1	0	1	1	1	0.9750		1	1	0	1	1	1	n/a
0	1	1	0	0	0	0.9500		1	1	1	0	0	0	n/a
0	1	1	0	0	1	0.9250		1	1	1	0	0	1	n/a
0	1	1	0	1	0	0.9000		1	1	1	0	1	0	n/a
0	1	1	0	1	1	0.8750		1	1	1	0	1	1	n/a
0	1	1	1	0	0	0.8500		1	1	1	1	0	0	n/a
0	1	1	1	0	1	0.8250		1	1	1	1	0	1	n/a
0	1	1	1	1	0	0.8000		1	1	1	1	1	0	n/a
0	1	1	1	1	1	0.7750		1	1	1	1	1	1	n/a

Note: 6.49kΩ connected between VID_SEL and LGND. V(VDAC) is pre-positioned 50mV higher than VID values listed above for load line positioning. VID is measured at EAOUT with EAOUT shorted to FB, ROSC=50 KΩ and a 4200 Ω resistor connecting VSETPT to VDAC to cancel the 50 mV pre-position offset, as shown in Fig. 3.

TABLE 3 - VR11 VID TABLE (PART1)

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
00	00000000	Fault
01	00000001	Fault
02	00000010	1.60000
03	00000011	1.59375
04	00000100	1.58750
05	00000101	1.58125
06	00000110	1.57500
07	00000111	1.56875
08	00001000	1.56250
09	00001001	1.55625
0A	00001010	1.55000
0B	00001011	1.54375
0C	00001100	1.53750
0D	00001101	1.53125
0E	00001110	1.52500
0F	00001111	1.51875
10	00010000	1.51250
11	00010001	1.50625
12	00010010	1.50000
13	00010011	1.49375
14	00010100	1.48750
15	00010101	1.48125
16	00010110	1.47500
17	00010111	1.46875
18	00011000	1.46250
19	00011001	1.45625
1A	00011010	1.45000
1B	00011011	1.44375
1C	00011100	1.43750
1D	00011101	1.43125
1E	00011110	1.42500
1F	00011111	1.41875
20	00100000	1.41250
21	00100001	1.40625
22	00100010	1.40000
23	00100011	1.39375
24	00100100	1.38750
25	00100101	1.38125
26	00100110	1.37500
27	00100111	1.36875
28	00101000	1.36250
29	00101001	1.35625
2A	00101010	1.35000
2B	00101011	1.34375
2C	00101100	1.33750
2D	00101101	1.33125
2E	00101110	1.32500
2F	00101111	1.31875
30	00110000	1.31250
31	00110001	1.30625
32	00110010	1.30000
33	00110011	1.29375
34	00110100	1.28750
35	00110101	1.28125
36	00110110	1.27500
37	00110111	1.26875
38	00111000	1.26250
39	00111001	1.25625
3A	00111010	1.25000
3B	00111011	1.24375
3C	00111100	1.23750
3D	00111101	1.23125
3E	00111110	1.22500
3F	00111111	1.21875

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
40	01000000	1.21250
41	01000001	1.20625
42	01000010	1.20000
43	01000011	1.19375
44	01000100	1.18750
45	01000101	1.18125
46	01000110	1.17500
47	01000111	1.16875
48	01001000	1.16250
49	01001001	1.15625
4A	01001010	1.15000
4B	01001011	1.14375
4C	01001100	1.13750
4D	01001101	1.13125
4E	01001110	1.12500
4F	01001111	1.11875
50	01010000	1.11250
51	01010001	1.10625
52	01010010	1.10000
53	01010011	1.09375
54	01010100	1.08750
55	01010101	1.08125
56	01010110	1.07500
57	01010111	1.06875
58	01011000	1.06250
59	01011001	1.05625
5A	01011010	1.05000
5B	01011011	1.04375
5C	01011100	1.03750
5D	01011101	1.03125
5E	01011110	1.02500
5F	01011111	1.01875
60	01100000	1.01250
61	01100001	1.00625
62	01100010	1.00000
63	01100011	0.99375
64	01100100	0.98750
65	01100101	0.98125
66	01100110	0.97500
67	01100111	0.96875
68	01101000	0.96250
69	01101001	0.95625
6A	01101010	0.95000
6B	01101011	0.94375
6C	01101100	0.93750
6D	01101101	0.93125
6E	01101110	0.92500
6F	01101111	0.91875
70	01110000	0.91250
71	01110001	0.90625
72	01110010	0.90000
73	01110011	0.89375
74	01110100	0.88750
75	01110101	0.88125
76	01110110	0.87500
77	01110111	0.86875
78	01111000	0.86250
79	01111001	0.85625
7A	01111010	0.85000
7B	01111011	0.84375
7C	01111100	0.83750
7D	01111101	0.83125
7E	01111110	0.82500
7F	01111111	0.81875

TABLE 3 - VR11 VID TABLE (PART 2)

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
80	10000000	0.81250
81	10000001	0.80625
82	10000010	0.80000
83	10000011	0.79375
84	10000100	0.78750
85	10000101	0.78125
86	10000110	0.77500
87	10000111	0.76875
88	10001000	0.76250
89	10001001	0.75625
8A	10001010	0.75000
8B	10001011	0.74375
8C	10001100	0.73750
8D	10001101	0.73125
8E	10001110	0.72500
8F	10001111	0.71875
90	10010000	0.71250
91	10010001	0.70625
92	10010010	0.70000
93	10010011	0.69375
94	10010100	0.68750
95	10010101	0.68125
96	10010110	0.67500
97	10010111	0.66875
98	10011000	0.66250
99	10011001	0.65625
9A	10011010	0.65000
9B	10011011	0.64375
9C	10011100	0.63750
9D	10011101	0.63125
9E	10011110	0.62500
9F	10011111	0.61875
A0	10100000	0.61250
A1	10100001	0.60625
A2	10100010	0.60000
A3	10100011	0.59375
A4	10100100	0.58750
A5	10100101	0.58125
A6	10100110	0.57500
A7	10100111	0.56875
A8	10101000	0.56250
A9	10101001	0.55625
AA	10101010	0.55000
AB	10101011	0.54375
AC	10101100	0.53750
AD	10101101	0.53125
AE	10101110	0.52500
AF	10101111	0.51875
B0	10110000	0.51250
B1	10110001	0.50625
B2	10110010	0.50000
B3	10110011	n/a
B4	10110100	n/a
B5	10110101	n/a
B6	10110110	n/a
B7	10110111	n/a
B8	10111000	n/a
B9	10111001	n/a
BA	10111010	n/a
BB	10111011	n/a
BC	10111100	n/a
BD	10111101	n/a
BE	10111110	n/a
BF	10111111	n/a

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
C0	11000000	n/a
C1	11000001	n/a
C2	11000010	n/a
C3	11000011	n/a
C4	11000100	n/a
C5	11000101	n/a
C6	11000110	n/a
C7	11000111	n/a
C8	11001000	n/a
C9	11001001	n/a
CA	11001010	n/a
CB	11001011	n/a
CC	11001100	n/a
CD	11001101	n/a
CE	11001110	n/a
CF	11001111	n/a
D0	11010000	n/a
D1	11010001	n/a
D2	11010010	n/a
D3	11010011	n/a
D4	11010100	n/a
D5	11010101	n/a
D6	11010110	n/a
D7	11010111	n/a
D8	11011000	n/a
D9	11011001	n/a
DA	11011010	n/a
DB	11011011	n/a
DC	11011100	n/a
DD	11011101	n/a
DE	11011110	n/a
DF	11011111	n/a
E0	11100000	n/a
E1	11100001	n/a
E2	11100010	n/a
E3	11100011	n/a
E4	11100100	n/a
E5	11100101	n/a
E6	11100110	n/a
E7	11100111	n/a
E8	11101000	n/a
E9	11101001	n/a
EA	11101010	n/a
EB	11101011	n/a
EC	11101100	n/a
ED	11101101	n/a
EE	11101110	n/a
EF	11101111	n/a
F0	11110000	n/a
F1	11110001	n/a
F2	11110010	n/a
F3	11110011	n/a
F4	11110100	n/a
F5	11110101	n/a
F6	11110110	n/a
F7	11110111	n/a
F8	11111000	n/a
F9	11111001	n/a
FA	11111010	n/a
FB	11111011	n/a
FC	11111100	n/a
FD	11111101	n/a
FE	11111110	FAULT
FF	11111111	FAULT

TABLE 4 - AMD 5-BIT TABLE FOR OPTERON

VID4	VID3	VID2	VID1	VID0	Voltage (V)
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	FAULT

Note: VID_SEL tied to LGND. V(VDAC) is pre-positioned 50mV higher than VID values listed above for load line positioning. VID is measured at EAOUT with EAOUT shorted to FB, ROSC=50 KΩ and a 4200 Ω resistor connecting VSETPT to VDAC to cancel the 50 mV pre-position offset, as shown in Fig. 3.

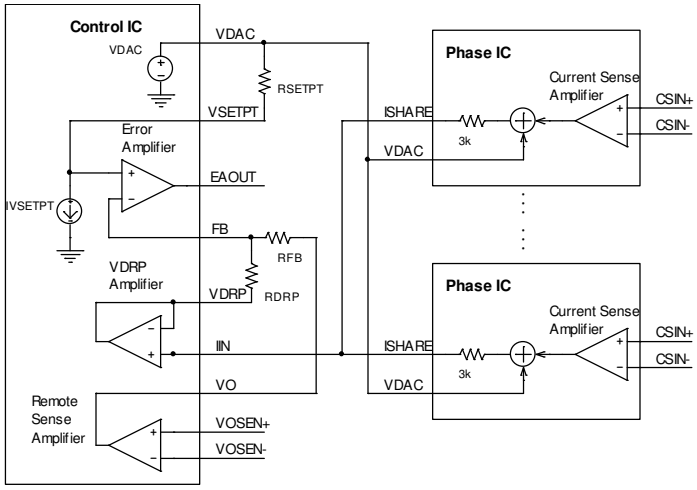


Figure 9 - Adaptive voltage positioning

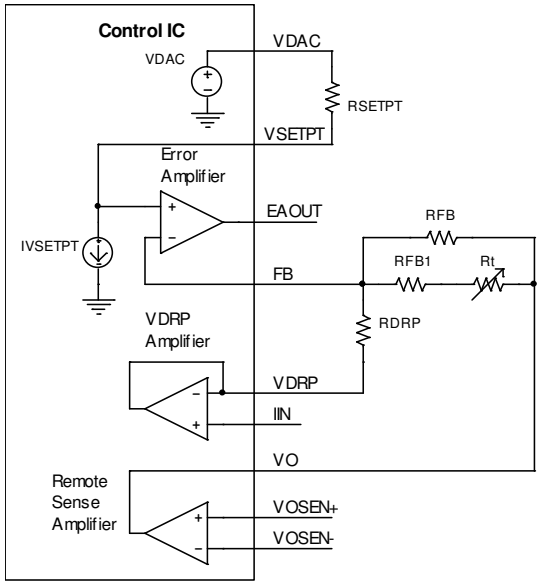


Figure 10 - Temperature compensation of inductor DCR

Remote Voltage Sensing

VOSEN+ and VOSEN- are used for remote sensing and connected directly to the load. The remote sense differential amplifier with high speed, low input offset and low input bias current ensures accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3500A has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. A charge current of 52.5uA and discharge current of 4uA control the up slope and down slope of the voltage at the SS/DEL pin respectively.

Figure 11 depicts start-up sequence of converter with VR 11 VID with boot voltage, which is selected by VIDSEL pin based on Table 1. If there is no fault, the SS/DEL pin will start charging when the enable crosses the threshold. The error amplifier output EAOUT is clamped low until SS/DEL reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.4V offset until the converter output reaches the 1.1V boot voltage. The SS/DEL voltage continues to increase until it rises above the 3.0V threshold of VID delay comparator. The VID set inputs are then activated and VDAC pin transitions to the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.92V and allows the PGOOD signal to be asserted. SS/DEL finally settles at 4.0V, indicating the end of the soft start.

Figure 12 shows start-up sequence of converter VR 11 VID without boot voltage or AMD Opteron, AMD 6-bit VID which is selected by VIDSEL pin based on Table 1. If there is no fault, the SS/DEL pin will start charging. The error amplifier output EAOUT is clamped low until SS/DEL reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.4V offset until the converter output reaches the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.92V and allows the PGOOD signal to be asserted. SS/DEL finally settles at 4.0V, indicating the end of the soft start.

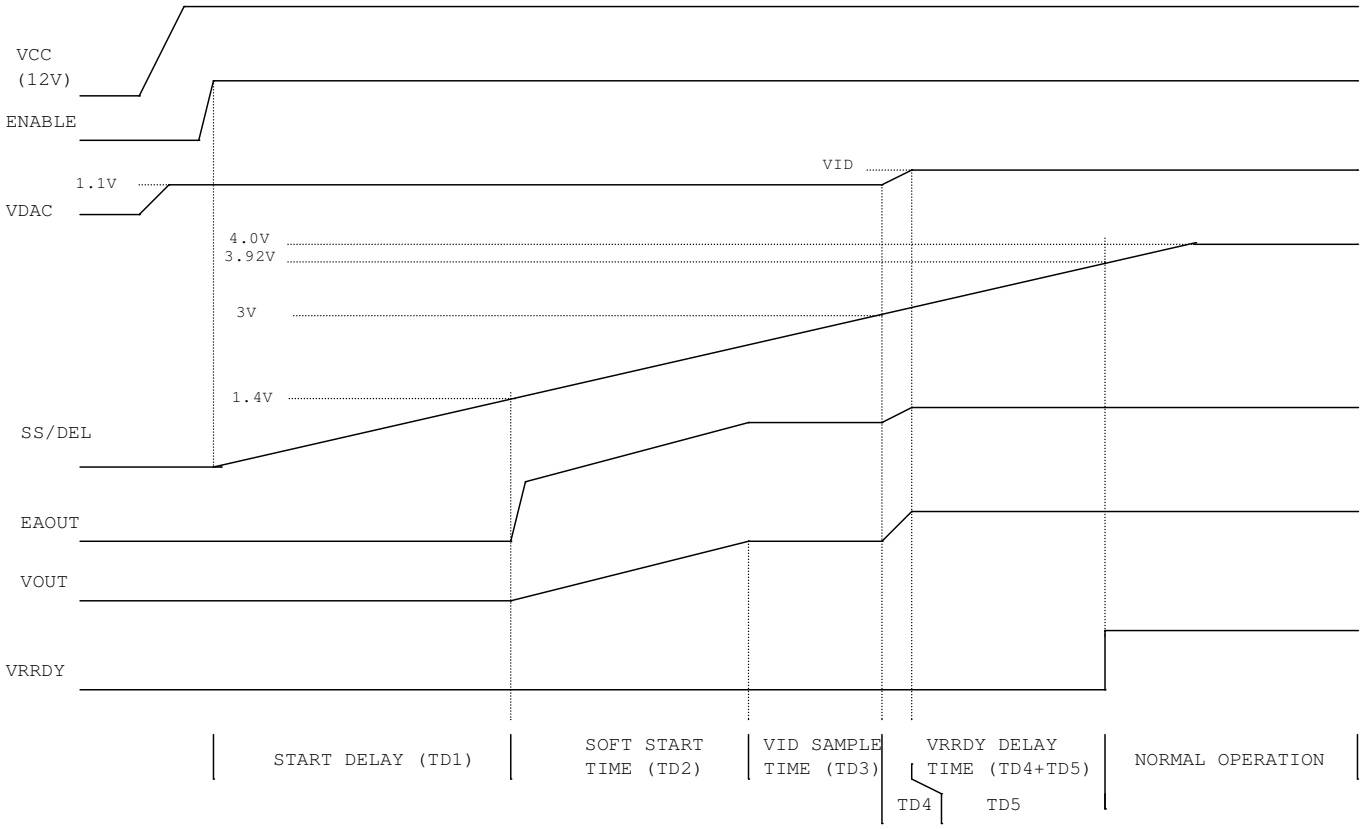


Figure 11 - Start-up sequence of converter with boot voltage

VCCL under voltage lock-out, VID fault modes, over current, as well as a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low turning off the phase IC drivers. The PGOOD pin also drives low, and SS/DEL begin to discharge until the voltage reaches 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

Other fault conditions, such as over voltage, open sense lines, open loop monitor, and open daisy chain, set different fault latches, which start discharging SS/DEL, pull down EAOUT voltage and drive PGOOD low. However, the latches can only be reset by cycling VCCL power.

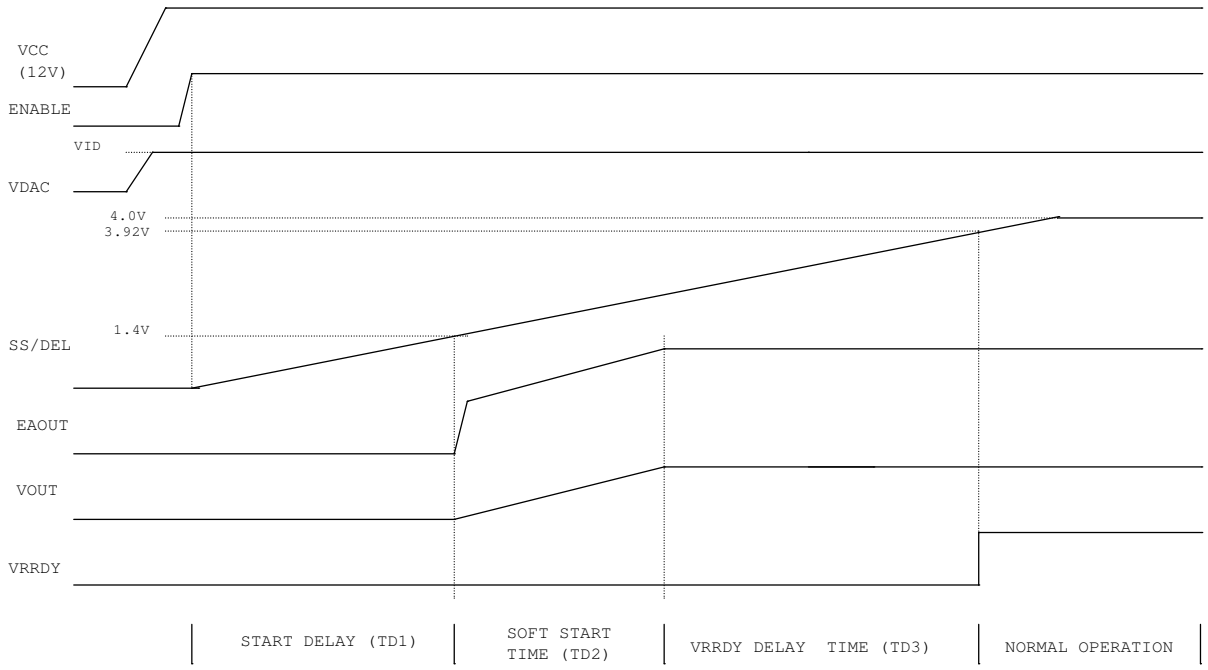


Figure 12 - Start-up sequence of converter without boot voltage

Constant Over-Current Control during Soft Start

The over current limit threshold is set by a resistor connected between OCSET and VDAC. If the IIN pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the OCSET voltage during soft start, the constant over-current control is activated. Figure 13 shows the constant over-current control with delay during soft start. The delay time is set by the ROSC resistor, which sets the number of switching cycles for the delay counter. The delay is required since over-current conditions can occur as part of normal operation due to inrush current. If an over-current occurs during soft start (before PGOOD is asserted), the SS/DEL voltage is regulated by the over current amplifier to limit the output current below the threshold set by OCSET voltage. If the over-current condition persists after delay time is reached, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs. The SS/DEL capacitor will discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the constant over-current control actions will repeat and the converter will be in hiccup mode. The delay time is controlled by a counter which is triggered by clock. The counter values vary with switching frequency per phase in order to have a similar delay time for different switching frequencies.

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between OCSET and VDAC pins. Figure 13 shows the constant over-current control with delay after PGOOD is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IIN pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the OCSET voltage after PGOOD is asserted, it will initiate the discharge of the capacitor at SS/DEL. The magnitude of the discharge current is proportional to the voltage difference between IIN and OCSET and has a maximum nominal value of 55uA. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 120mV offset of the delay comparator, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs and de-asserting the PGOOD signal. The output current is not controlled during the delay time. The SS/DEL capacitor will discharge until it reaches 200 mV and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.

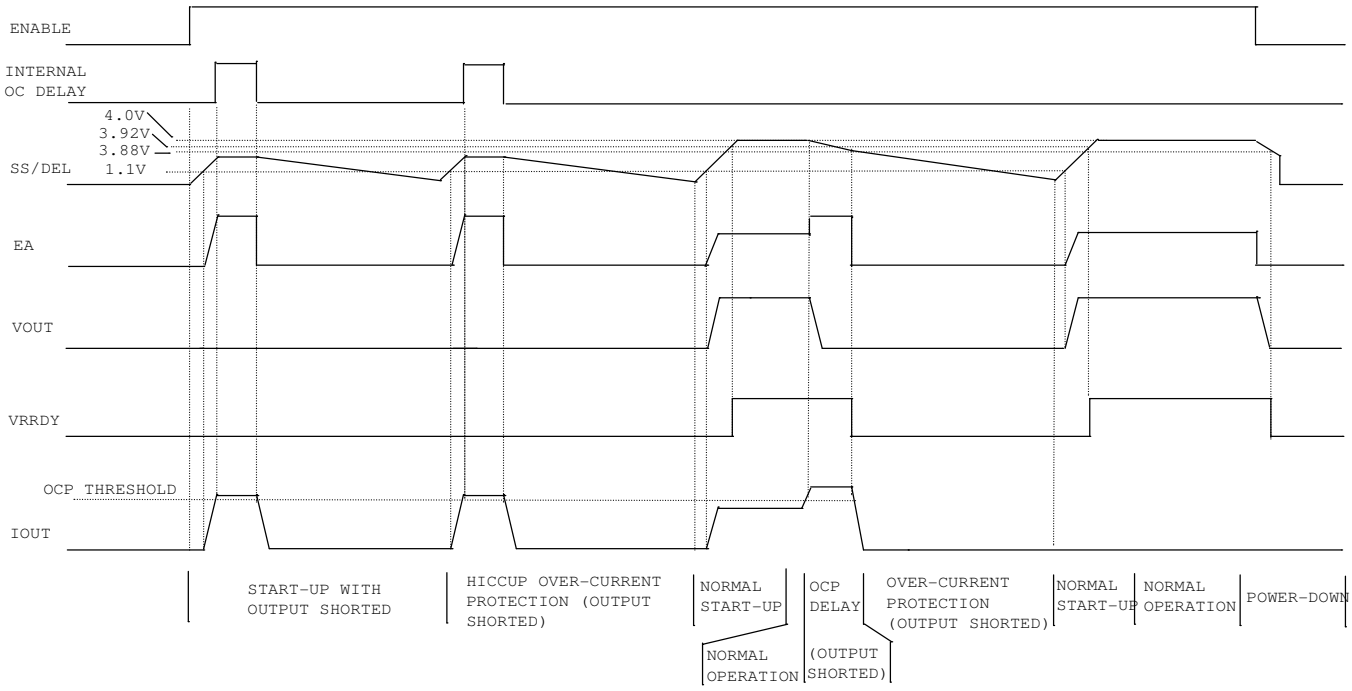


Figure 13 - Over Current Protection waveforms during and after soft start

Linear Regulator Output (VCCL)

The IR3500A has a built-in linear regulator controller, and only an external NPN transistor is needed to create a linear regulator. The output voltage of the linear regulator can be programmed between 4.75V and 7.5V by the resistor divider at VCCLFB pin. The regulator output powers the gate drivers and other circuits of the phase ICs along with circuits in the control IC, and the voltage is usually programmed to optimize the converter efficiency. The linear regulator can be compensated by a 4.7uF capacitor at the VCCL pin. As with any linear regulator, due to stability reasons, there is an upper limit to the maximum value of capacitor that can be used at this pin and it's a function of the number of phases used in the multiphase architecture and their switching frequency. Figure 14 provides Bode plots for the linear regulator with 5 phases switching at 750 kHz.

An external 5V can be connected to this pin to replace the linear regulator with appropriate selection of the VCCLFB resistor divider, and VCCLDRV resistor. While using an external VCCL its essential to adjust it such that VCCLFB is slightly lower than the 1.19V reference voltage. This condition ensures that the VCCLDRV pin doesn't load the ROSC pin. The switching frequency, VSETPT, and OCSET are derived from the loading current of ROSC pin.

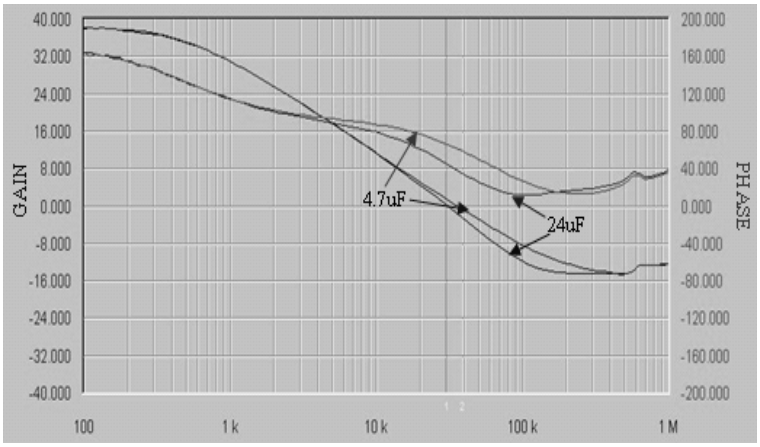


Figure 14 - VCCL regulator stability with 5 phases and PHSOUT equals 750 kHz.

VCCL Under Voltage Lockout (UVLO)

The IR3500A has no under voltage lockout for converter input voltage (VCC), but monitors the VCCL voltage instead, which is used for the gate drivers of phase ICs and circuits in control IC and phase ICs. During power up, the fault latch will be reset if VCCL is above 94% of the voltage set by resistor divider at VCCLFB pin. If VCCL voltage drops below 86% of the set value, the fault latch will be set.

VID Fault Codes

VID codes of 0000000X and 1111111X for VR11, and 11111 for AMD 5-bit Opteron will set the fault latch and disable the error amplifier. A 1.3us delay is provided to prevent a fault condition from occurring during Dynamic VID changes. A VID FAULT condition is latched for VR 11 with boot voltage and can only be cleared by cycling power to VCCL.

Voltage Regulator Ready (PGOOD)

The PGOOD pin is an open-collector output and should be pulled up to a voltage source through a resistor. After soft start cycle is complete, the PGOOD remains high until the output voltage is within regulation and SS/DEL is above 3.92V. The PGOOD pin becomes low if the fault latch, over voltage latch, open sense line latch, or open daisy chain latch is set. A high level at the PGOOD pin indicates that the converter is in operation and has no fault. The PGOOD stays high as long as the output voltage is within 300 mV of the programmed VID. During start-up, it is pulled low with an input voltage as low as 2 V. It stays low until the startup sequence has completed, and the output voltage has moved to the programmed VID.

Open Voltage Loop Detection

The output voltage range of error amplifier is detected all the time to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08V for 8 switching cycles, the fault latch is set. The fault latch can only be cleared by cycling power to VCCL.

Load Current Indicator Output

The VDRP pin voltage represents the average current of the converter plus the VDAC voltage. The load current information can be retrieved by a differential amplifier which subtracts the VDAC voltage from the VDRP voltage.

Enable Input

For Intel VID codes, pulling the ENABLE pin below 0.8V sets the Fault Latch and a voltage above 0.85V enables the soft start of the converter. For AMD VID codes, pulling the ENABLE pin below 1.14V sets the Fault Latch and a voltage above 1.2V enables the soft start of the converter.

Thermal Monitoring (VRHOT)

A resistor divider including a thermistor at the HOTSET pin sets the VRHOT threshold. The thermistor is usually placed at the temperature sensitive region of the converter, and is linearized by a series resistor. The IR3500A compares the HOTSET pin voltage with a reference voltage of 1.6V. The VRHOT pin is an open-collector output and should be pulled up to a voltage source through a resistor. If the thermal trip point is reached the VRHOT output drives low. The hysteresis of the VRHOT comparator is added to eliminate toggling of VRHOT output.

Over Voltage Protection (OVP)

The output over-voltage happens during normal operation if a high side MOSFET short occurs or if output voltage is out of regulation. The over-voltage protection comparator monitors Vo pin voltage. If Vo pin voltage exceeds VDAC by 130mV, as shown in Figure 14, IR3500A raises ROSC/OVP pin voltage to V(VCCL) - 1V, which sends over voltage signal to system. The ROSC/OVP pin can also be connected to a thyrister in a crowbar circuit, which pulls the converter input low in over voltage conditions. The over voltage condition also sets the over voltage fault latch,

which pulls error amplifier output low to turn off the converter output. At the same time IIN pin (ISHARE of phase ICs) is pulled up to VCCL to communicate the over voltage condition to phase ICs, as shown in Figure 15. In each phase IC, the OVP circuit overrides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain on until ISHARE pin voltage drops below V(VCCL) - 800mV, which signals the end of over voltage condition. An over voltage fault condition is latched in the IR3500A and can only be cleared by cycling power to the IR3500A VCCL.

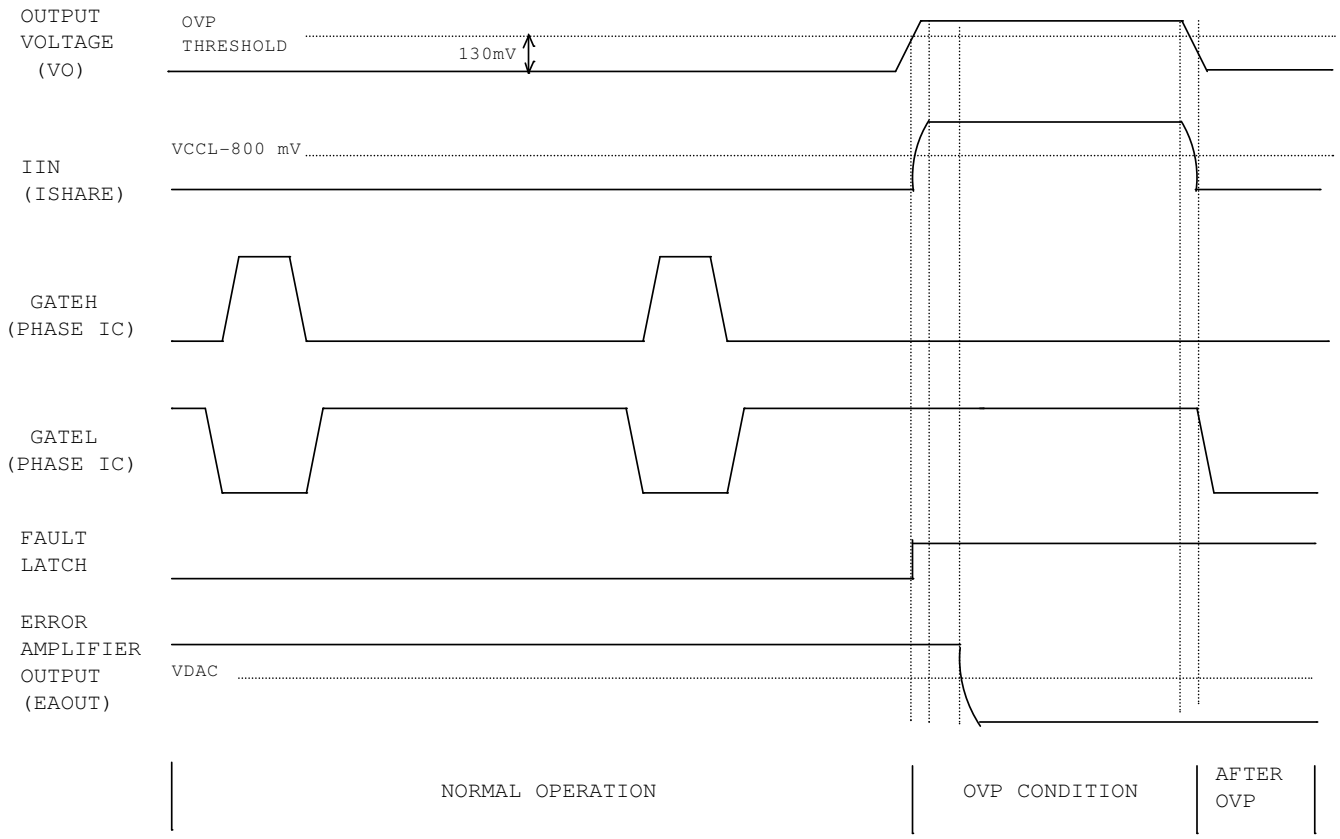


Figure 15 - Over-voltage protection during normal operation

In the event of a high side MOSFET short before power up, the OVP flag is activated with as little supply voltage as possible, as shown in Figure 16. The VOSEN+ pin is compared against a fixed voltage of 1.73V (typical) for OVP conditions at power-up. The ROSC/OVP pin will be pulled higher than 1.6V with VCCLDRV voltage as low as 1.8V. An external MOSFET or comparator should be used to disable the silver box, activate a crowbar, or turn off the supply source. The 1.8V threshold is used to prevent false over-voltage triggering caused by pre-charging of output capacitors.

Pre-charging of converter output voltage may trigger OVP. If the converter output is pre-charged above 1.73V as shown in Figure 17, ROSC/OVP pin voltage will be higher than 1.6V when VCCLDRV voltage reaches 1.8V. ROSC/OVP pin voltage will be VCCLDRV-1V and rise with VCCLDRV voltage until VCCL is above UVLO threshold, after which ROSC/OVP pin voltage will be VCCL-1V. The converter cannot start unless the over voltage condition stops and VCCL is cycled. If the converter output is pre-charged 130mV above VDAC but lower than 1.73V, as shown in Figure 17, the converter will soft start until SS/DEL voltage is above 3.92V (4.0V-0.08V). Then, over voltage comparator is activated and fault latch is set.

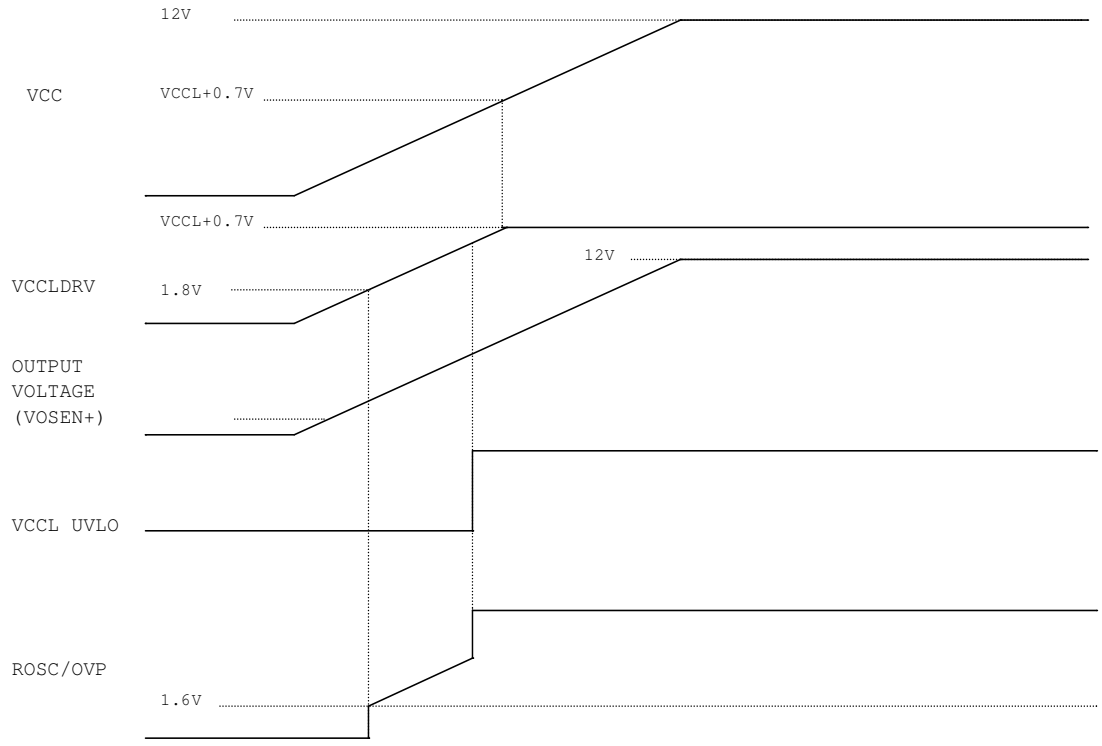


Figure 16 - Over-voltage protection during power-up

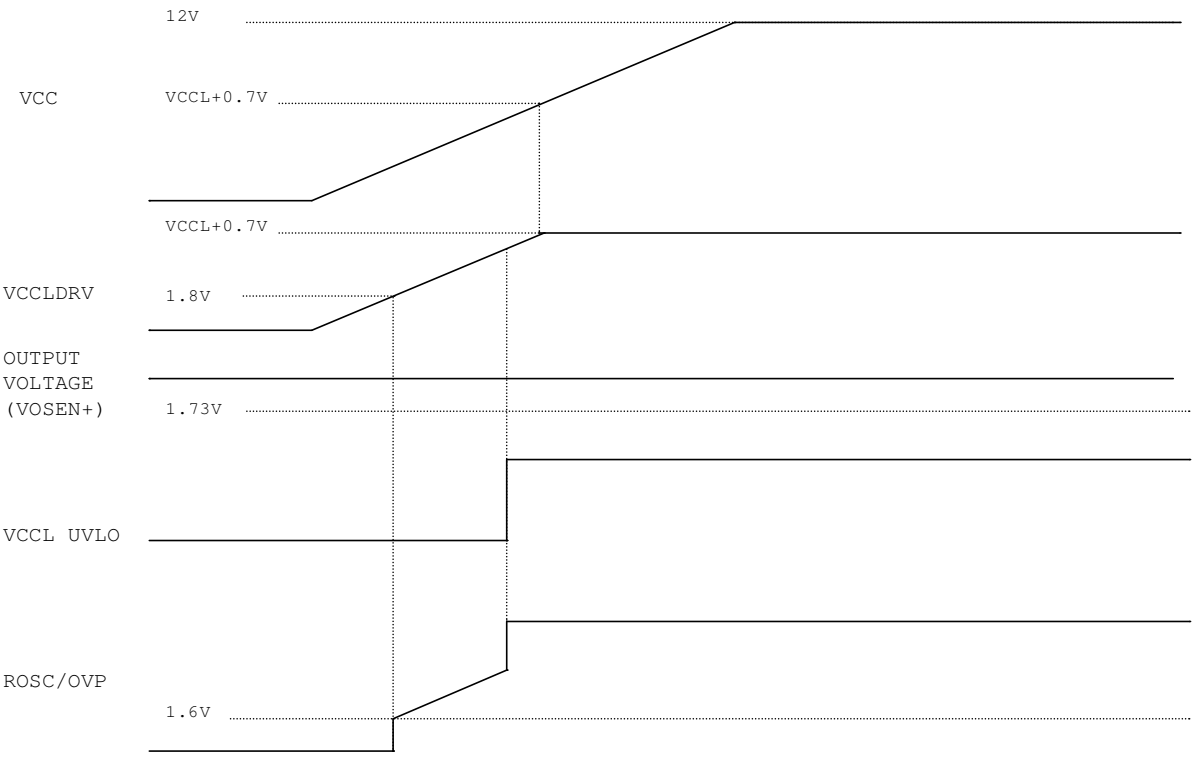


Figure 17 - Over-voltage protection with pre-charging converter output Vo > 1.73V

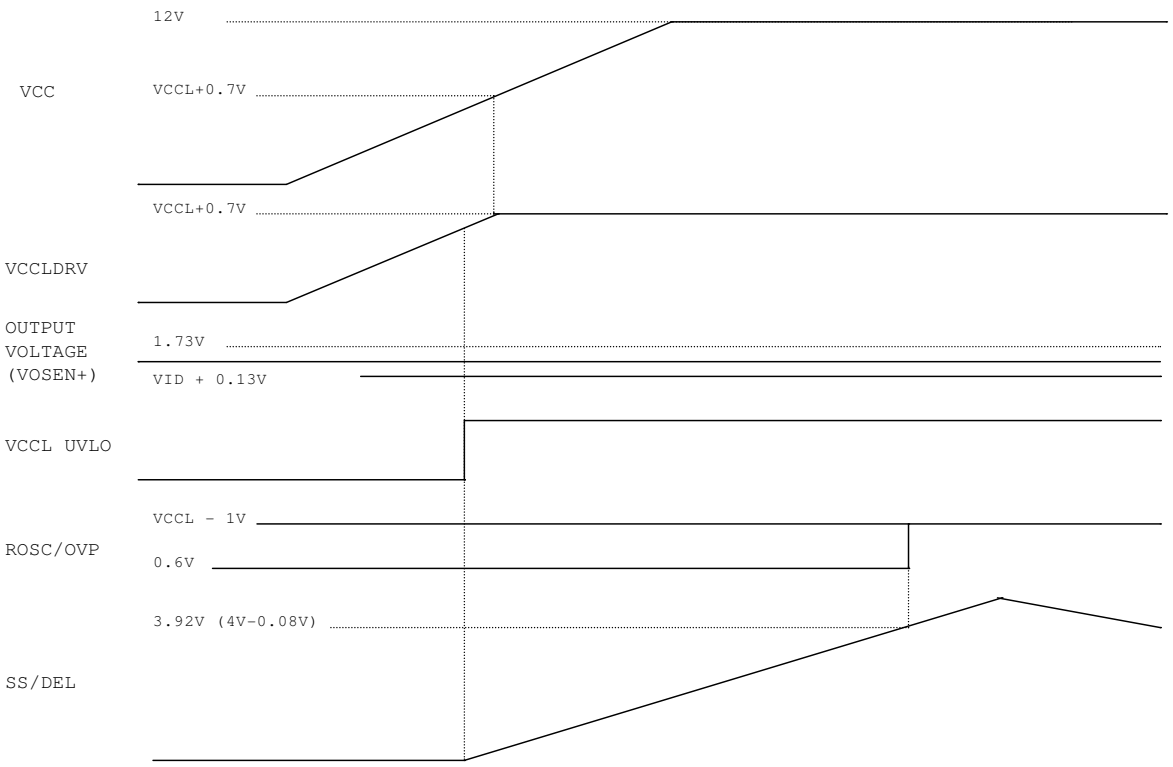


Figure 18 - Over-voltage protection with pre-charging converter output VID + 0.13V <Vo < 1.73V

During dynamic VID down, OVP may be triggered when output voltage can not follow VDAC voltage change at light load with large output capacitance. Therefore, over-voltage threshold is raised to 1.73V from VDAC+130mV whenever dynamic VID is detected and the difference between output voltage and VDAC is more than 50mV, as shown in Figure 19. The over-voltage threshold is changed back to VDAC+130mV if the difference is smaller than 50mV.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered and provide effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

Open Remote Sense Line Protection

If either remote sense line VOSEN+ or VOSEN- or both are open, the output of remote sense amplifier (VO) drops. The IR3500A monitors VO pin voltage continuously. If VO voltage is lower than 200 mV, two separate pulse currents are applied to VOSEN+ and VOSEN- pins respectively to check if the sense lines are open. If VOSEN+ is open, a voltage higher than 90% of V(VCCL) will be present at VOSEN+ pin and the output of open line detect comparator will be high. If VOSEN- is open, a voltage higher than 700mV will be present at VOSEN- pin and the output of open-line-detect comparator will be high. The open sense line fault latch is set, which pulls error amplifier output low immediately and shut down the converter. The SS/DEL voltage is discharged and the fault latch can only be reset by cycling VCCL power.

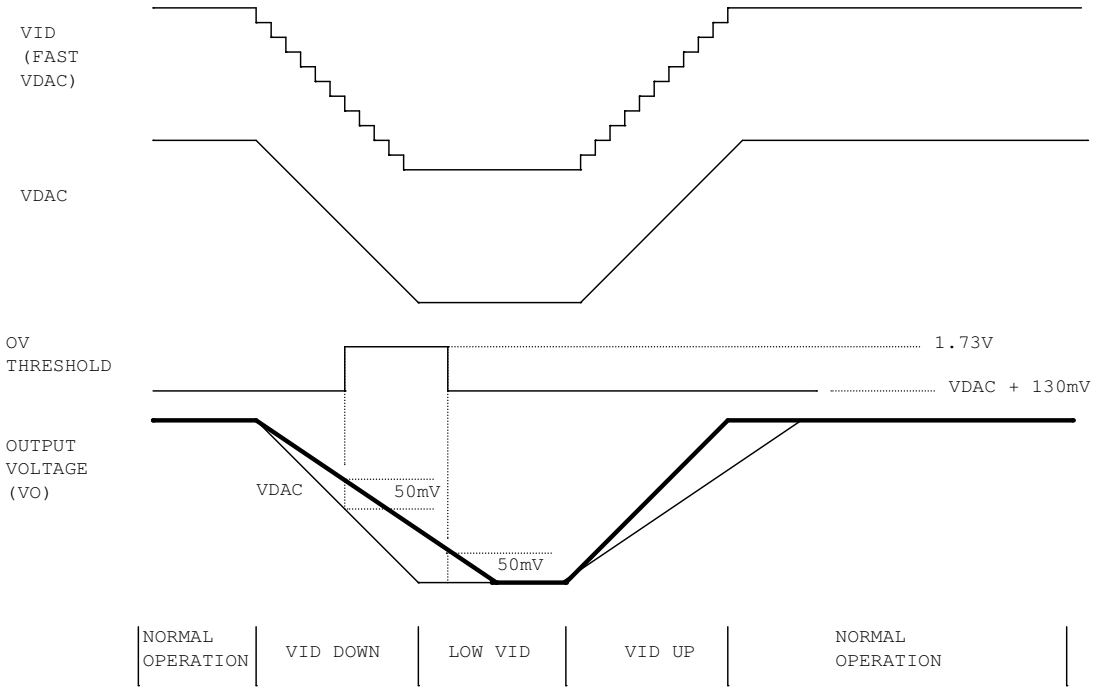


Figure 19 - Over-voltage protection during dynamic VID

Open Daisy Chain Protection

IR3500A checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 32 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the open daisy chain fault is registered, and SS/DEL is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3500A monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an open daisy chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3500A checks the timing of the input pulse at PHSIN pin to determine the phase number. This information is used to have symmetrical phase delay between phase switching without the need of any external component.

Single Phase Operation

In an architecture where only a single phase is needed the switching frequency is determined by the clock frequency.

APPLICATIONS INFORMATION

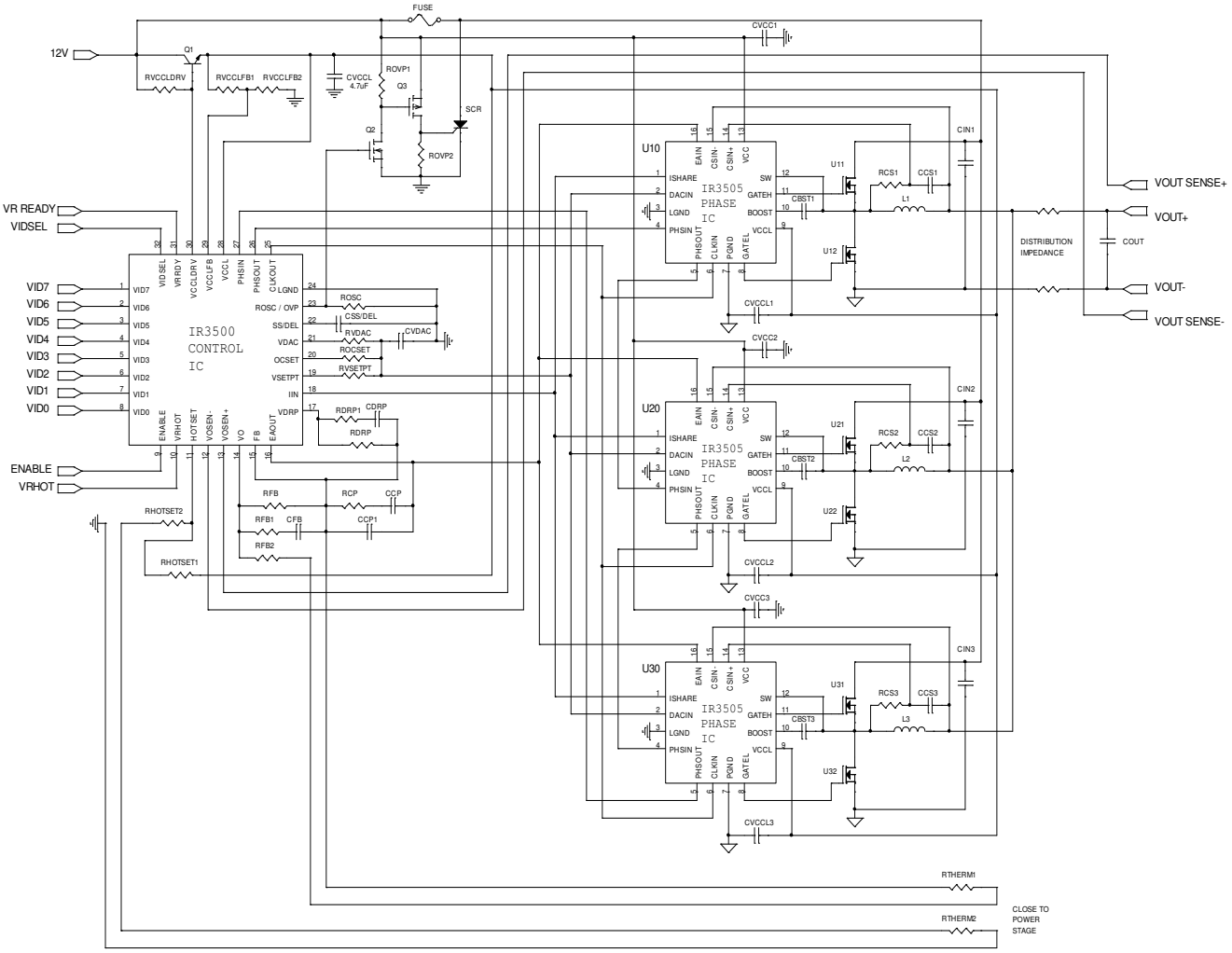


Figure 20 - IR3500A / IR3505 Three Phase AMD Opteron Converter

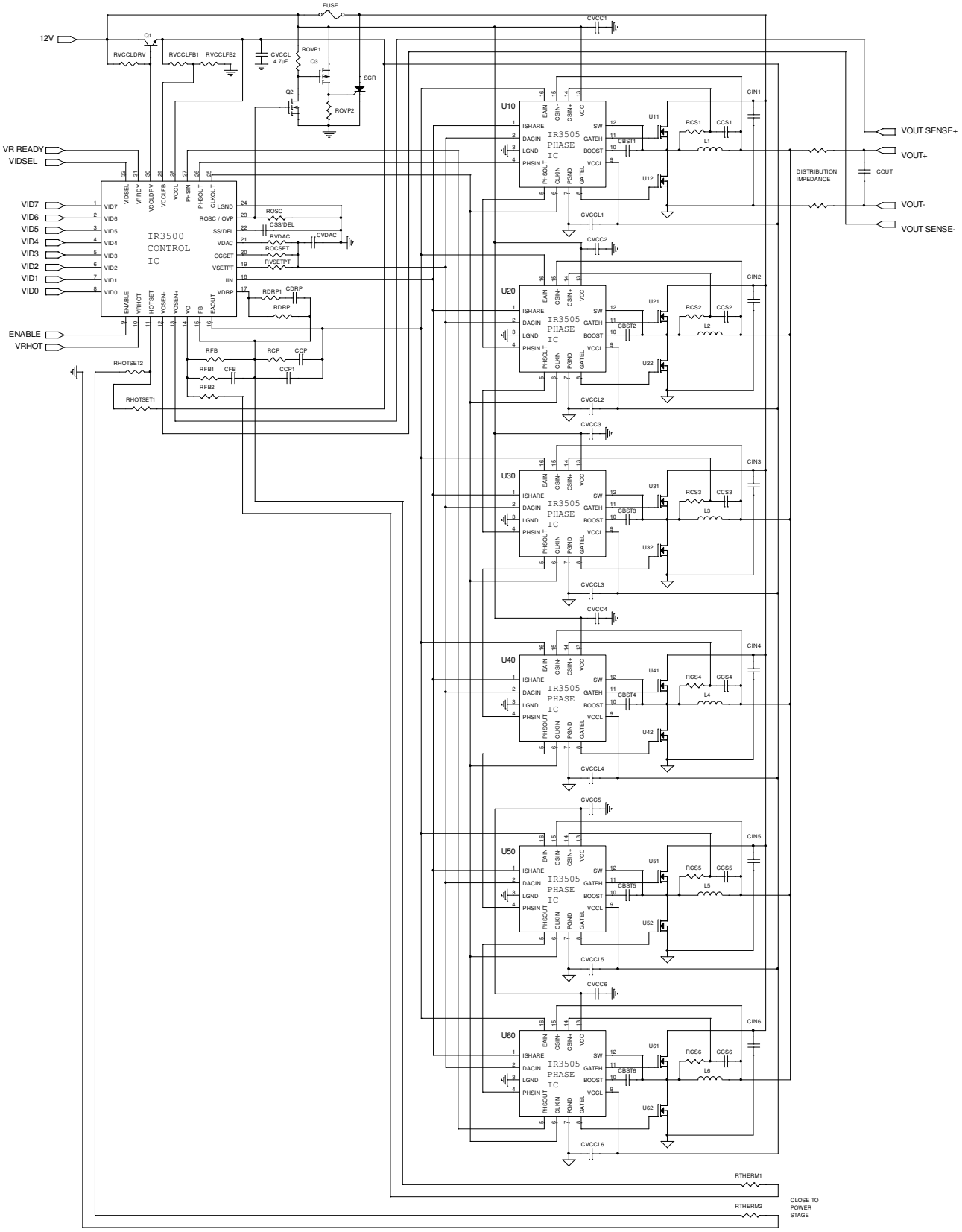


Figure 21 - IR3500A / IR3505 Six Phase VRM11.0 / VRD11.0 / EVRD11.0 Converter

DESIGN PROCEDURE

Oscillator Resistor *Rosc*

The oscillator of IR500 generates square-wave pulses to synchronize the phase ICs. The switching frequency of each phase converter equals the PHSOUT frequency, which is set by the external resistor ROSC according to the curve in Figure 23. The CLKOUT frequency equals the switching frequency multiplied by the phase number. The Rosc sets the reference current used for the no load offset and OCSET which is given by Figure 23 and equals:

$$ISETPT = IOCSET = \frac{0.595}{Rosc} \quad (1)$$

Soft Start Capacitor *CSS/DEL*

The soft start capacitor CSS/DEL programs five different time parameters. They include soft start delay time, soft start time, VID sample delay time, VR ready delay time and over-current fault latch delay time after VR ready.

For the converter using VR11 VID with boot voltage, the SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10. After the ENABLE pin voltage rises above 0.85V, there is a soft-start delay time TD1, after which the error amplifier output is released to allow the soft start of output voltage. The soft start time TD2 represents the time during which converter voltage rises from zero to 1.1V. The VID sample delay time (TD3) is the time period when VID stays at boot voltage of 1.1V. VID rise or fall time (TD4) is the time when VID changes from boot voltage to the final voltage. The VR ready delay time (TD5) is the time period from VR reaching the final voltage to the VR ready signal being issued, which is determined by the delay comparator threshold.
CSS/DEL = 0.1uF meets all the specifications of TD1 to TD5, which are determined by (2) to (6) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \quad (2)$$

$$TD2 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{C_{SS/DEL} * 1.1}{52.5 * 10^{-6}} \quad (3)$$

$$TD3 = \frac{C_{SS/DEL} * (3 - 1.4 - 1.1)}{I_{CHG}} = \frac{C_{SS/DEL} * 0.7}{52.5 * 10^{-6}} \quad (4)$$

$$TD4 = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{I_{CHG}} = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{52.5 * 10^{-6}} \quad (5)$$

$$TD5 = \frac{C_{SS/DEL} * (3.92 - 3)}{I_{CHG}} - TD4 = \frac{C_{SS/DEL} * 0.92}{52.5 * 10^{-6}} - TD4 \quad (6)$$

For the converter using VR 11 VID without boot voltage or AMD 5-bit and 6-bit VIDs, the SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 11. After the ENABLE pin voltage rises above 0.85V/1.2V, there is a soft-start delay time TD1, after which the error amplifier output is released to allow the soft start. The soft start time TD2 represents the time during which converter voltage rises from zero to Vo. VR ready delay time (TD3) is the time period from VR reaching the final voltage to the VR ready signal being issued. Calculate CSS/DEL based on the required soft start time (TD2).

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{V_O} = \frac{TD2 * 52.5 * 10^{-6}}{V_O} \quad (7)$$

The soft start delay time (TD1) and VR ready delay time (TD3) are determined by (8) to (9) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{52.5 * 10^{-6}} \quad (8)$$

$$TD3 = \frac{C_{SS/DEL} * (4.0 - V_O)}{I_{CHG}} = \frac{C_{SS/DEL} * (4.0 - V_O)}{52.5 * 10^{-6}} \quad (9)$$

Once $C_{SS/DEL}$ is chosen, the minimum over-current fault latch delay time t_{OCDEL} is fixed and can be quantified as

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{C_{SS/DEL} * 0.12}{55 * 10^{-6}} \quad (10)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope SR_{DOWN} can be programmed by the external capacitor C_{VDAC} as defined in (11), where I_{SINK} is the sink current of VDAC pin. The slew rate of VDAC up-slope is the same as that of down-slope. The resistor R_{VDAC} is used to compensate VDAC circuit and can be calculated as follows

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44 * 10^{-6}}{SR_{DOWN}} \quad (11)$$

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}^{\ 2}} \quad (12)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/℃, and therefore the maximum inductor DCR can be calculated from (13), where R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature T_{L_MAX} and room temperature $T_{\_ROOM}$ respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (13)$$

The total input offset voltage (V_{CS_TOFST}) of current sense amplifier in phase ICs is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor R_{CS}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS} \quad (14)$$

The over-current limit is set by the external resistor R_{OCSET} and is given by (15). In a multiphase architecture the peak to peak ripple of the net inductor current is much smaller than the stand alone phase due to interleaving. The ratio of the peak to average current in this case can be approximated using (16).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET} \quad (15)$$

$$K_P = \frac{\left[V_I \cdot D \cdot (1-D) \cdot n \cdot (D - \frac{m}{n}) \cdot (\frac{m+1}{n} - D)\right]}{(I_{LIMIT}/n) \cdot L \cdot f_{sw} \cdot 2 \cdot D \cdot (1-D)} \quad (16)$$

Where; I_{LIMIT}=Over current limit, n=Number of phases, K_P=Ratio of the peak to average current for the inductor, G_{CS}=Gain of the current sense amplifier, I_{OCSET}= Determined by the ROSC and given by Figure 24, D=V_o/V_I, m=Maximum integer that doesn't exceed (n*D)

No Load Output Voltage Setting Resistor *RVSETPT*,

A resistor between VSETPT pin and VDAC is used to create output voltage offset VO_NLOFST, which is the difference between VDAC voltage and output voltage at no load condition. RVSETPT is determined by (17), where IVSETPT is the current flowing out of VSETPT pin as shown in Figure 23.

$$R_{VSETPT} = \frac{V_{O\_NLOFST}}{I_{VSETPT}} \quad (17)$$

VCCL Capacitor *CVCCL*

The capacitor is selected based on the stability requirement of the linear regulator and the load current to be driven. The linear regulator supplies the bias and gate drive current of the phase ICs. A 4.7uF normally ensures stable VCCL performance for Intel VR11 and AMD applications.

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Since VCCL voltage is proportional to the MOSFET gate driver loss and inversely proportional to the MOSFET conduction loss, the optimum voltage should be chosen to maximize the converter efficiency. VCCL linear regulator consists of an external NPN transistor, a ceramic capacitor and a programmable resistor divider. Pre-select RVCCLFB1, and calculate RVCCLFB2 from (18).

$$R_{VCCLFB2} = \frac{R_{VCCLFB1} * 1.19}{VCCL - 1.19} \quad (18)$$

VCCL Regulator Drive Resistor *RVCCLDRV*

The drive resistor is primarily dependent on the load current requirement of the linear regulator and the minimum input voltage requirements. The following equation gives an estimate of the average load current of the switching phase ICs.

$$I_{drive\_avg} = \left[(Q_{gb} + Q_{gt}) \cdot f_{sw} + 10mA\right] \cdot n \quad (19)$$

Q_{gb} and Q_{gt} are the gate charge of the top and bottom FET. For a minimum input voltage and a maximum VCCL, the maximum $R_{VCCLDRV}$ required to use the full pull-down current of the VCCL driver is given by

$$R_{VCCLDRV} = \frac{V_I(\min) - 0.7 - VCCL(\max)}{I_{drive\_avg} / \beta_{\min}} \quad (20)$$

Due to limited pull down capability of the VCCLDRV pin, make sure the following condition is satisfied.

$$\frac{V_I(\max) - 0.7 - VCCL(\min)}{R_{VCCLDRV}} < 10mA \quad (21)$$

In the above equation, V_I(min) and V_I(max) is the minimum and maximum anticipated input voltage. If the above condition is not satisfied there is a need to use a device with higher β_{min} or Darlington configuration can be used instead of a single NPN transistor.

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is fixed at 1.6V, and a negative temperature coefficient (NTC) thermistor RTHERM is required to sense the temperature of the power stage. If we pre-select RTHERM, the NTC thermistor resistance at allowed maximum temperature TMAX is calculated from (22).

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] \quad (22)$$

Select the series resistor $R_{HOTSET2}$ to linearize the NTC thermistor, which has non-linear characteristics in the operational temperature range. Then calculate $R_{HOTSET1}$ corresponding to the allowed maximum temperature TMAX from (23).

$$R_{HOTSET1} = \frac{(R_{TMAX} + R_{HOTSET2}) * (VCCL - 1.6)}{1.6} \quad (23)$$

VOLTAGE LOOP COMPENSATION

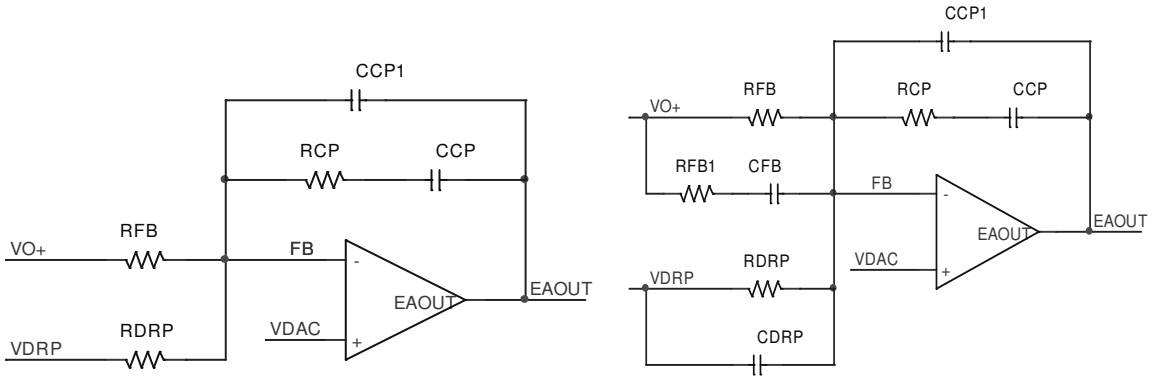
The adaptive voltage positioning (AVP) is usually adopted in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces an extra zero to the voltage loop and splits the double poles of the power stage, which makes the voltage loop compensation much easier.

Adaptive voltage positioning lowers the converter voltage by $R_O * I_O$, where R_O is the required output impedance of the converter. Pre-select feedback resistor R_{FB}, and calculate the droop resistor RDRP,

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS}}{n * R_O} \quad (25)$$

The selection of compensation types depends on the output capacitors used in the converter. For applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 22(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 22(b) is preferred.

For applications where AVP is not required, the compensation is the same as for the regular voltage mode control. For converters using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 22(b) with R_{DRP} and C_{DRP} removed.



(a) Type II compensation (b) Type III compensation

Figure 22 - Voltage loop compensation network

Type II Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine R_{CP} and C_{CP} from (26) and (27), where L_E and C_E are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (26)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (27)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency and phase margin of the voltage loop can be estimated by (28) and (29), where R_{LE} is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (28)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (29)$$

Choose the desired crossover frequency fc around fc1 estimated by (28) or choose fc between 1/10 and 1/5 of the switching frequency per phase, and select the components to ensure the slope of close loop gain is -20dB per decade around the crossover frequency. Choose resistor R_{FB1} according to (30), and determine C_{FB} and C_{DRP} from (31) and (32).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (30)$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \quad (31)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (32)$$

R_{CP} and C_{CP} have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine R_{CP} and C_{CP} from (33) and (34).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I} \quad (33)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (34)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for Non-AVP Applications

Resistor R_{DRP} and capacitor C_{DRP} are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from (35), and determine the component values based on (36) to (40),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \quad (35)$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * 5}{V_I * K} \quad (36)$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \quad (37)$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \quad (38)$$

$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \quad (39)$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \quad (40)$$

DESIGN EXAMPLE 1 – AMD OPTERON CONVERTER (FIGURE 20)

SPECIFICATIONS

Input Voltage: V_I=12 V
DAC Voltage: V_{DAC}=1.3 V
No Load Output Voltage Offset: V_{O_NLOFST}=10 mV
Output Current: I_O=120 ADC
Maximum Output Current: I_{OMAX}=135 ADC
Output Impedance: R_O=0.7 mΩ
Soft Start Delay Time: TD1=1-5mS
Soft Start Time: TD2=2 mS
VR Ready Delay Time: TD3=0-10mS
Maximum Over Current Delay: t_{OCDEL}<2.5mS
Dynamic VID Down-Slope Slew Rate: SR_{DOWN}=2.5mV/uS
Over Temperature Threshold: T_{MAX}=115 ºC

POWER STAGE

Phase Number: n=3
Switching Frequency: f_{SW}=250 kHz
Output Inductors: L=470 nH, R_L= 1mΩ
Output Capacitors: Polymer, C=560uF, R_C= 7mΩ, Number Cn=12

IR3500A EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, R_{OSC} can be determined from the curve in Figure 23. For a switching frequency of 250kHz per phase, choose R_{OSC}=50kΩ. The reference current for VSETPT and OCSET is given by 11.9 uA.

Soft Start Capacitor *CSS/DEL*

Determine the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{V_O} = \frac{2*10^{-3} * 52.5 * 10^{-6}}{1.3} = 0.1uF$$

The soft start delay time is

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{0.1*10^{-6} * 1.4}{52.5*10^{-6}} = 2.67mS$$

The VR ready delay time is

$$TD3 = \frac{C_{SS/DEL} * (4.0 - V_O)}{I_{CHG}} = \frac{0.1*10^{-6} * (4.0 - 1.3)}{52.5*10^{-6}} = 5.14mS$$

The minimum over current fault latch delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{0.1*10^{-6} * 0.12}{55*10^{-6}} = 0.2ms$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate. The up-slope slew rate is the same as the down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44*10^{-6}}{2.5*10^{-3}/10^{-6}} = 18nF$$

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^2} = 0.5 + \frac{3.2*10^{-15}}{(18*10^{-9})^2} = 10\Omega$$

Over Current Setting Resistor *ROCSET*

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 1*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 1.29m\Omega$$

Set the over current limit at 135A. From Figure 24, the bias current of OCSET pin (I_{OCSET}) is 11.9uA with R_{OSC}=50kΩ. The total current sense amplifier input offset voltage is 0.3mV, which includes the offset created by the current sense amplifier (CSA) input bias current through the resistor R_{CS}.

$$V_{CS\_TOFST} = 0.3mV$$

Calculate constant K_P, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{\left[V_I \cdot D \cdot (1-D) \cdot n \cdot (D - \frac{m}{n}) \cdot (\frac{m+1}{n} - D)\right]}{(I_{LIMIT}/n) \cdot L \cdot f_{sw} \cdot 2 \cdot D \cdot (1-D)} = \frac{\left[12 \cdot 0.108 \cdot (1-0.108) \cdot 3 \cdot (0.108 - \frac{0}{3}) \cdot (\frac{0+1}{3} - 0.108)\right]}{(135/3) \cdot 0.47u \cdot 250k \cdot 2 \cdot 0.108 \cdot (1-0.108)} = 0.082$$

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET}$$

$$= (\frac{135}{3} * 1.29 * 10^{-3} * 1.082 + 0.3 * 10^{-3}) * 34 / (11.9 * 10^{-6}) = 181k\Omega$$

No Load Output Voltage Setting Resistor *RVSETPT* and Adaptive Voltage Positioning Resistor *RDRP*

From Figure 24, the bias current of VSETPT pin is 11.9uA with ROSC=50kΩ.

$$R_{VSETPT} = \frac{V_{CS\_TOFST}}{I_{VSETPT}} = \frac{10*10^{-3}}{11.9*10^{-6}} = 840\Omega$$, choose RVSETPT=825Ω.

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Choose VCCL=7V to maximize the converter efficiency. Pre-select RVCCLFB1=20kΩ, and calculate RVCCLFB2.

$$R_{VCCLFB2} = \frac{R_{VCCLFB1}*1.19}{VCCL-1.19} = \frac{20*10^3*1.19}{7-1.19} = 4.05k\Omega$$

VCCL Drive Resistor *RVCCLDRV*

The maximum drive current for the linear regulator is dependent on the type of MosFET used. For this example its assumed that IR6622/ IRF6691 are used as buck switches.

$$I_{drive\_avg} = \left[(47n+11n)\cdot 250k + 10mA\right]\cdot 3 = 75mA \qquad (19)$$

The minimum input voltage is assumed to be 10 V and VCCL is fixed at 6.5V for this design.

$$R_{VCCLDRV} = \frac{10V-0.7V-6.5V}{75mA/50} = 1.8k\Omega \qquad (20)$$

Assuming the maximum input voltage to as 14 V,

$$\frac{14V-0.7-6.5}{1.8k\Omega} = 3mA < 10mA \qquad (21)$$

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

Choose NTC thermistor RTHERM=2.2kΩ, which has a constant of BTHERM=3520, and the NTC thermistor resistance at the allowed maximum temperature TMAX is,

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] = 2.2*10^3 * EXP[3520*(\frac{1}{273+115} - \frac{1}{273+25})] = 142\Omega$$

Select RHOTSET2 = 931Ω to linearize the NTC, which has non-linear characteristics in the operational temperature range. Then calculate RHOTSET1 corresponding to the allowed maximum temperature TMAX.

$$R_{HOTSET1} = \frac{(R_{TMAX}+R_{HOTSET2})*(VCCL-1.6)}{1.6} = \frac{(142+931)*(7-1.6)}{1.6} = 3.63k\Omega,$$ choose RHOTSET1=3.65kΩ.

VOLTAGE LOOP COMPENSATION

Type II compensation is used for the converter with Polymer output capacitors. Choose the crossover frequency fc=25kHz, which is 1/10 of the switching frequency per phase, and determine Rcp and CCP.

Pre-select RFB=2.00kΩ, and calculate RDRP, RCP and CCP.

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS}}{n * R_O} = \frac{2000 * 1.29 * 10^{-3} * 34}{3 * 0.7 * 10^{-3}} = 41.8k\Omega$$, choose RDRP=42.2kΩ

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} = \frac{(2\pi * 25 * 10^3)^2 * (470 * 10^{-9} / 3) * (560 * 10^{-6} * 12) * 2000 * 5}{12 * \sqrt{1 + (2\pi * 25 * 10^3 * 560 * 10^{-6} * 7 * 10^{-3})^2}} = 21.5k\Omega,$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(470 * 10^{-9} / 3) * (560 * 10^{-6} * 12)}}{21.5 * 10^3} = 15nF$$

Choose CCP1=47pF to reduce high frequency noise.

DESIGN EXAMPLE 2 – VR11 HIGH FREQUENCY ALL-CERAMIC CONVERTER (FIG. 21)

SPECIFICATIONS

Input Voltage: VI=12 V
DAC Voltage: VDAC=1.3 V
No Load Output Voltage Offset: VO_NLOFST=20 mV
Output Current: IO=105 ADC
Maximum Output Current: IOMAX=120 ADC
Output Impedance: RO=0.91 mΩ
Soft Start Delay Time: TD1=1-5mS
Soft Start Time: TD2=0-3mS
VID Sample Delay Time: TD3=0.05-3mS
VID Rise Time: TD4=0-2.5mS
VR Ready Delay Time: TD5=0-3mS
Maximum Over Current Delay Time: tOCDEL<2.5mS
Dynamic VID Down-Slope Slew Rate: SRDOWN=2.5mV/uS
Over Temperature Threshold: TMAX=115 ºC

POWER STAGE

Phase Number: n=6
Switching Frequency: fSW = 800 kHz
Output Inductors: L=100 nH, RL=0.5 mΩ
Output Capacitors: Ceramic, C=22uF, RC= 2mΩ, Number Cn=62

IR3500A EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, ROSC can be determined from the curve in Figure 23 data sheet. For a switching frequency of 800kHz per phase, choose ROSC = 15.0 kΩ. The reference current is given by 40uA.

Soft Start Capacitor *CSS/DEL*

Determine the soft start capacitor to meet the specifications of the delay time.

Choose CSS/DEL=0.1uF. The soft start delay time is

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{0.1 * 10^{-6} * 1.4}{52.5 * 10^{-6}} = 2.67mS$$

The soft start time is

$$TD2 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{0.1*10^{-6} * 1.1}{52.5*10^{-6}} = 2.1mS$$

The VID sample delay time is

$$TD3 = \frac{C_{SS/DEL} * (3.2 - 1.4 - 1.1)}{I_{CHG}} = \frac{0.1*10^{-6} * 0.7}{52.5*10^{-6}} = 1.33mS$$

VID rise time is

$$TD4 = \frac{C_{SS/DEL} * |V_{DAC} - 1.1|}{I_{CHG}} = \frac{0.1*10^{-6} * |1.3 - 1.1|}{52.5*10^{-6}} = 0.38mS$$

The VR ready delay time is

$$TD5 = \frac{C_{SS/DEL} * (3.92 - 3)}{I_{CHG}} - TD4 = \frac{0.1*10^{-6} * 0.92}{52.5*10^{-6}} - TD4 = 1.37mS$$

Minimum over current fault latch delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{OCDISCHG}} = \frac{0.1*10^{-6} * 0.12}{55*10^{-6}} = 0.21ms$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate. The up-slope slew rate is the same as the down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{44*10^{-6}}{2.5*10^{-3}/10^{-6}} = 18nF$$

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}^{2}} = 0.5 + \frac{3.2*10^{-15}}{(18*10^{-9})^2} = 10\Omega$$

Over Current Setting Resistor *ROCSET*

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.5*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 0.64m\Omega$$

Set the over current limit at 135A. From Figure 22, the bias current of OCSET pin (I_{OCSET}) is 40uA with R_{OSC}=15kΩ. The total current sense amplifier input offset voltage is 0.3mV, which includes the offset created by the current sense amplifier (CSA) input bias current through the resistor R_{CS}.

$$V_{CS\_TOFST} = 0.3mV$$

Calculate constant KP, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{\left[V_I \cdot D \cdot (1-D) \cdot n \cdot (D - \frac{m}{n}) \cdot (\frac{m+1}{n} - D)\right]}{(I_{LIMIT}/n) \cdot L \cdot f_{sw} \cdot 2 \cdot D \cdot (1-D)} = \frac{\left[12 \cdot 0.108 \cdot (1-0.108) \cdot 6 \cdot (0.108 - \frac{0}{6}) \cdot (\frac{0+1}{6} - 0.108)\right]}{(135/6) \cdot 0.1u \cdot 800k \cdot 2 \cdot 0.108 \cdot (1-0.108)} = 0.126$$

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET}$$

$$= (\frac{135}{6} * 0.64 * 10^{-3} * 1.126 + 0.3 * 10^{-3}) * 34 / (40 * 10^{-6}) = 14k\Omega$$

Calculate constant KP, the ratio of inductor peak current over average current in each phase,

No Load Output Voltage Setting Resistor *RVSETPT* and Adaptive Voltage Positioning Resistor *RDRP*

From Figure 24, the bias current of VSETPT pin is 40uA with ROSC=15kΩ.

$$R_{VSETPT} = \frac{V_{O\_NLOFST}}{I_{VSETPT}} = \frac{20 * 10^{-3}}{40 * 10^{-6}} = 500\Omega$$

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Choose VCCL=7V to maximize the converter efficiency. Pre-select RVCCLFB1=20kΩ, and calculate RVCCLFB2.

$$R_{VCCLFB2} = \frac{R_{VCCLFB1} * 1.19}{VCCL - 1.19} = \frac{20 * 10^3 * 1.19}{7 - 1.19} = 4.05k\Omega$$

VCCL Drive Resistor *RVCCLDRV*

The maximum drive current for the linear regulator is dependent on the type of MosFET used. For this example, it's assumed that IR6622/ IRF6691 are used as buck switches.

$$I_{drive\_avg} = [(47n + 11n) \cdot 800k + 10mA] \cdot 6 = 350mA \qquad (19)$$

The minimum input voltage is assumed to be 10.5 V and VCCL is fixed at 6.5V for this design.

$$R_{VCCLDRV} = \frac{10.5V - 0.7V - 6.5V}{350mA / 70} = 660\Omega \qquad (20)$$

Choose a transistor with β(min) of 70. The maximum input voltage is assumed 13.5 V,

$$\frac{13.5V - 0.7 - 6.5}{660\Omega} = 9.5mA < 10mA \qquad (21)$$

Thermistor *RTHERM* and Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

Choose NTC thermistor RTHERM=2.2kΩ, which has a constant of BTHERM=3520, and the NTC thermistor resistance at the allowed maximum temperature TMAX is,

$$R_{TMAX} = R_{THERM} * EXP[B_{THERM} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] = 2.2 * 10^3 * EXP[3520 * (\frac{1}{273+115} - \frac{1}{273+25})] = 142\Omega$$

Select RHOTSET2 = 931Ω to linearize the NTC, which has non-linear characteristics in the operational temperature range. Then calculate RHOTSET1 corresponding to the allowed maximum temperature TMAX.

$$R_{HOTSET1} = \frac{(R_{TMAX} + R_{HOTSET2}) * (VCCL - 1.6)}{1.6} = \frac{(142 + 931) * (7 - 1.6)}{1.6} = 3.63k\Omega$$, choose $R_{HOTSET1}$=3.65kΩ.

VOLTAGE LOOP COMPENSATION

Type III compensation is used for the converter with only ceramic output capacitors. The crossover frequency and phase margin of the voltage loop can be estimated as follows.

Choose R_{FB} = 1.65kΩ, and calculate R_{DRP}.

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS}}{n * R_O} = \frac{1.65*10^3 * 0.64*10^{-3} * 34}{6 * 0.91 * 10^{-3}} = 6.58k\Omega$$, choose R_{DRP}=6.65kΩ.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} = \frac{6.65*10^3}{2\pi * (62*22*10^{-6}) * 34 * 1.65*10^3 * (0.5*10^{-3} / 6)} = 165kHz$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} = 63°$$

Choose $R_{FB1} = \frac{2}{3} * R_{FB} = \frac{2}{3} * 1.65*10^3 = 1.10k\Omega$

Choose the desired crossover frequency fc (=150kHz) around fc1 estimated above, and calculate

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} = \frac{1}{4\pi * 150*10^3 * 1.1*10^3} = 4.8nF$$, choose C_{FB}=4.7nF.

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} = \frac{(1.65*10^3 + 1.1*10^3) * 4.7*10^{-9}}{6.65*10^3} = 2.0nF$$, choose C_{DRP}=2.2nF.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I} = \frac{(2\pi * 150*10^3)^2 * (100*10^{-9} / 6) * (22*10^{-6} * 62) * 1.65*10^3 * 5}{12} = 13.9k\Omega$$

Choose R_{FB}=13.7kΩ.

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(100*10^{-9} / 6) * (22*10^{-6} * 62)}}{13.7*10^3} = 3.5nF$$, choose C_{CP}=3.3nF.

Choose C_{CP1}=47pF to reduce high frequency noise.

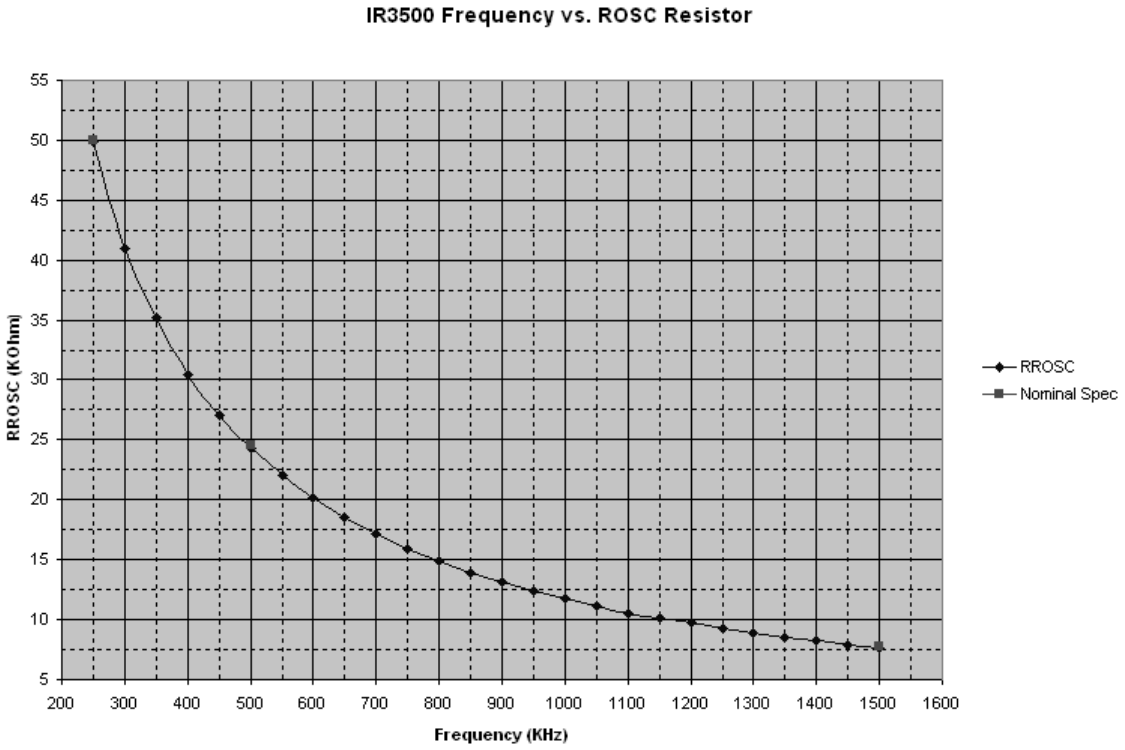


Figure 23 - Frequency variation with ROSC.

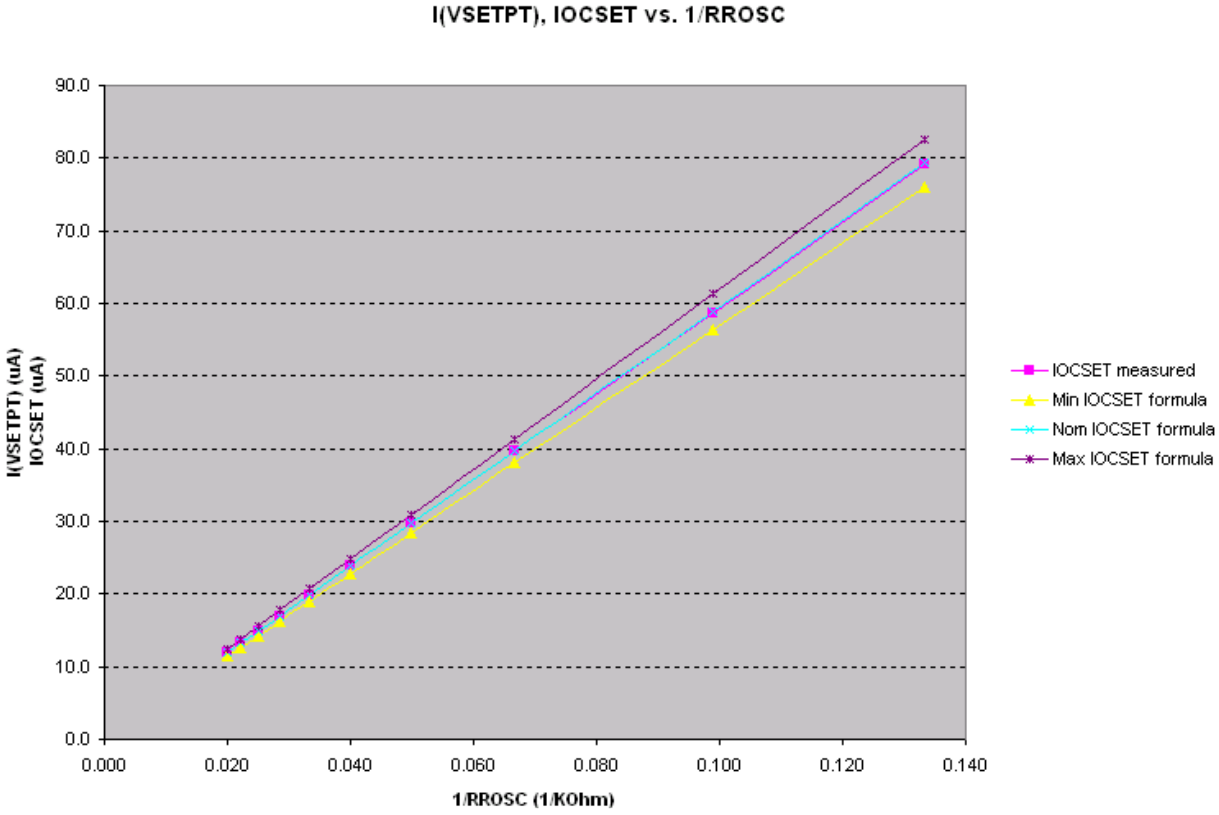
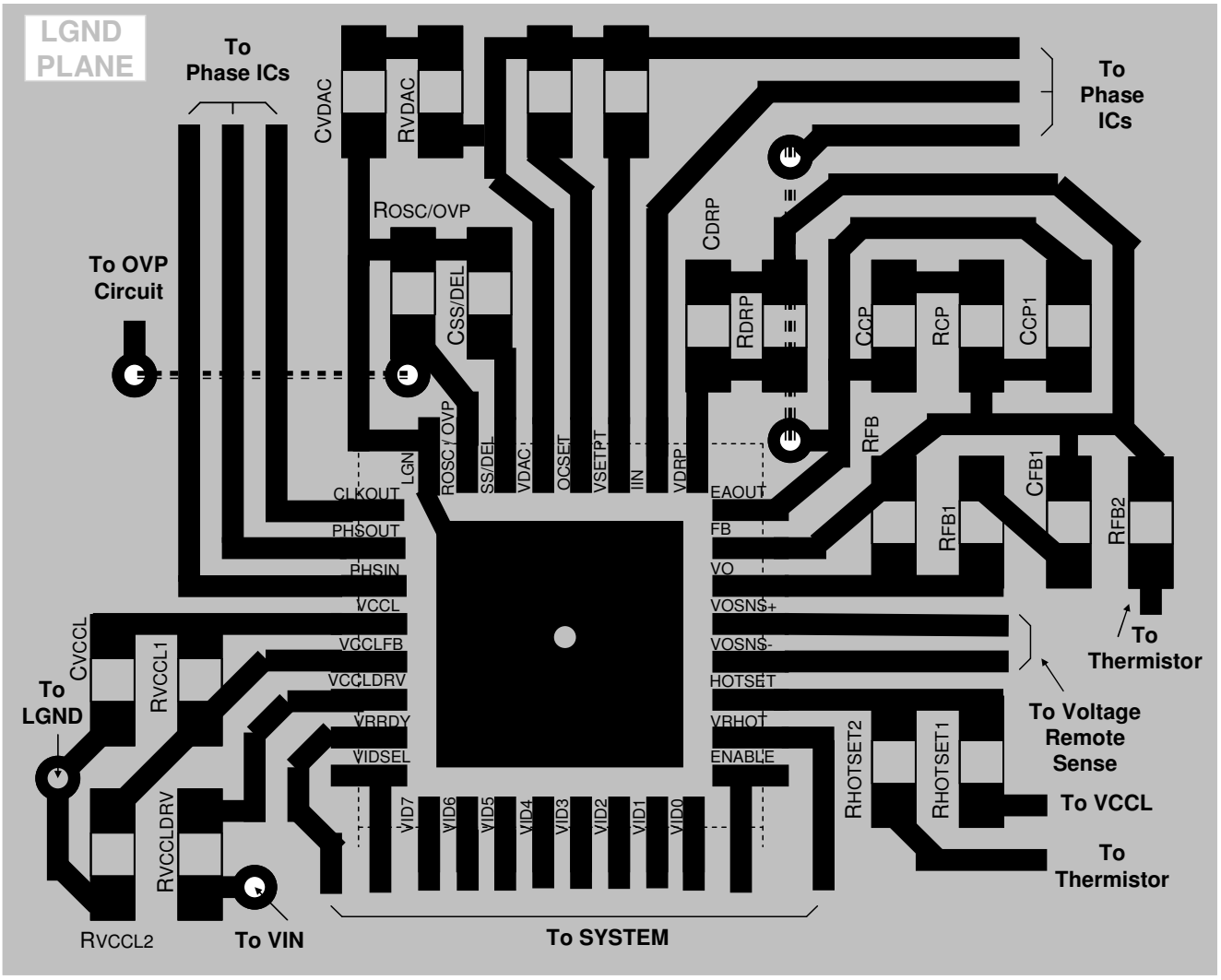


Figure 24 - ISETPT, OCSET with ROSC.

LAYOUT GUIDELINES

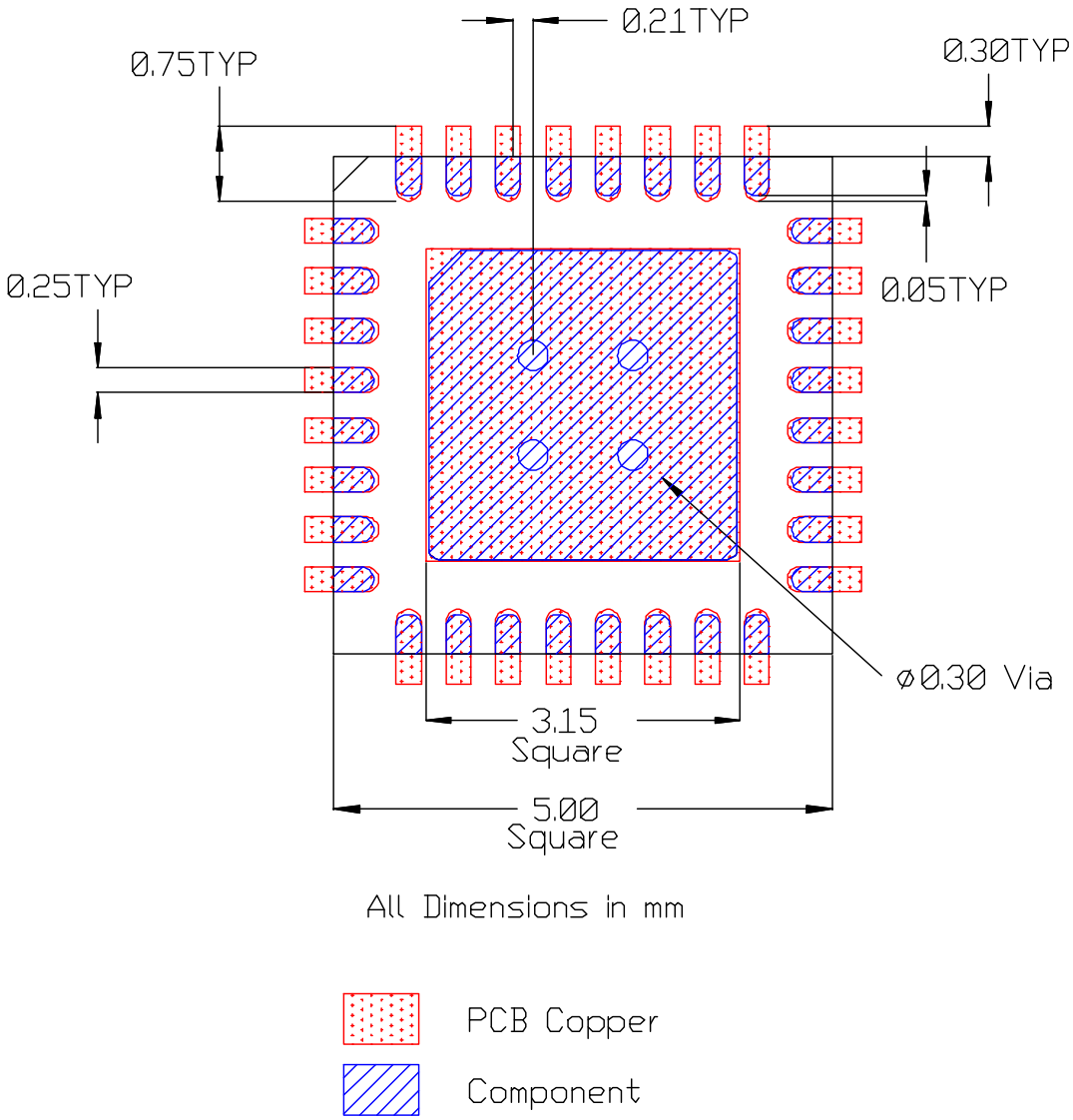
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Place VCCL decoupling capacitor VCCL as close as possible to VCCL and LGND pins.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, and CSS/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB, VO and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Avoid analog control bus signals, VDAC, IIN, and especially EAOUT, crossing over the fast transition nodes.
- Separate digital bus, CLKOUT, PHSOUT and PHSIN from the analog control bus and other compensation components.



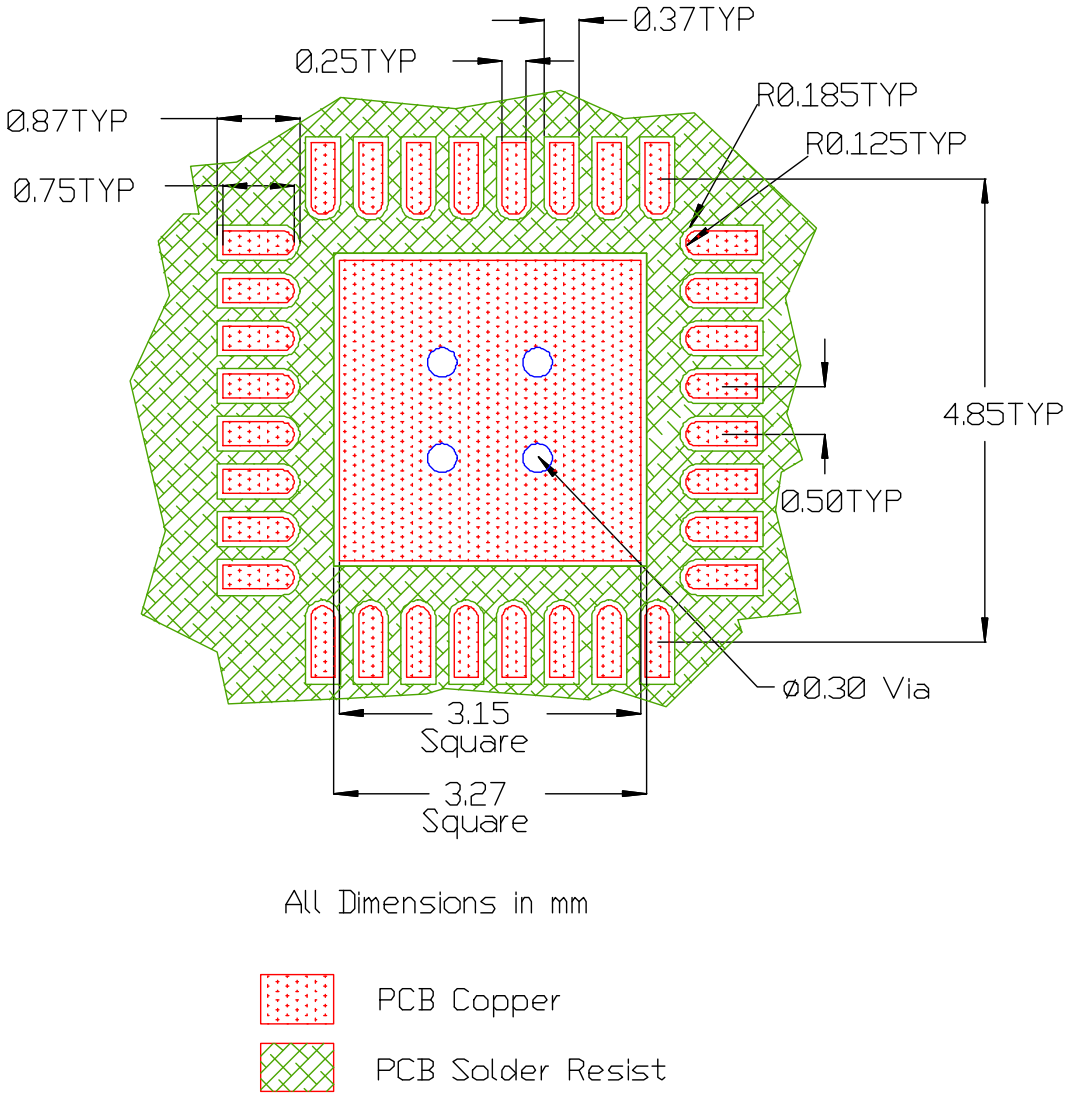
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.3mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



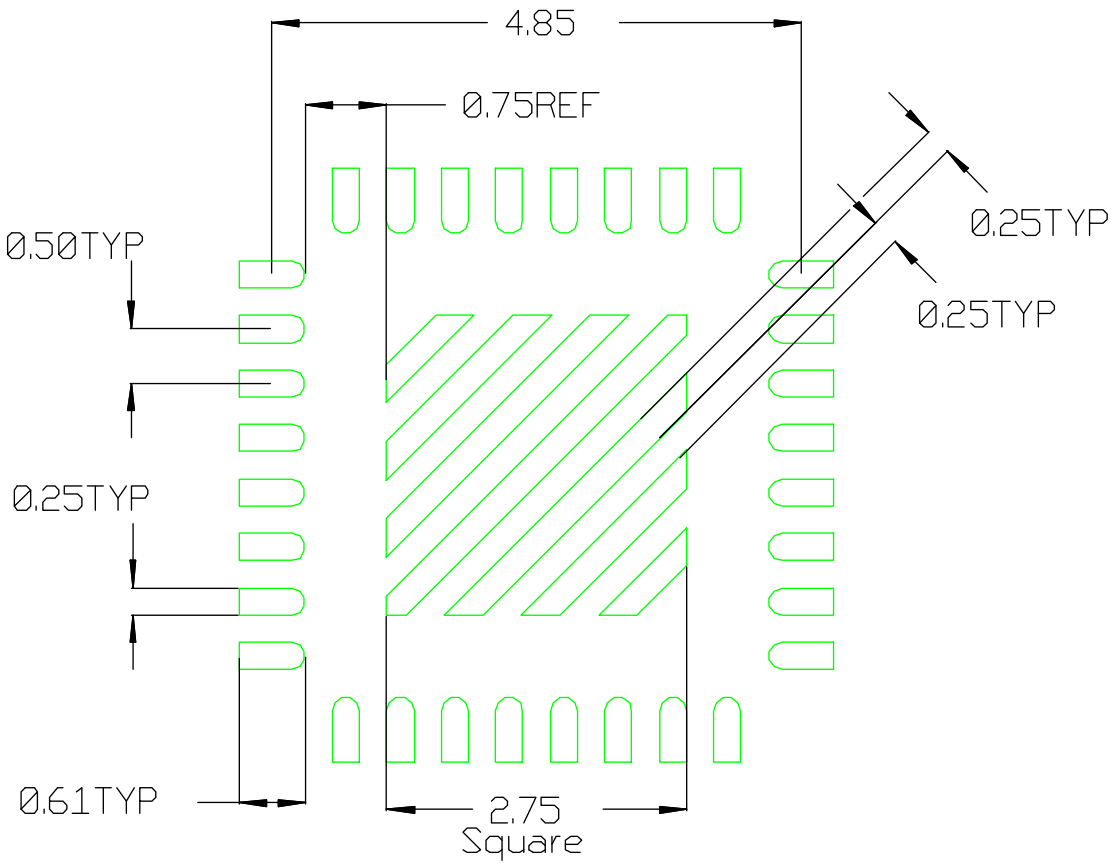
SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The four vias in the land pad should be tented or plugged from bottom board side with solder resist.



STENCIL DESIGN

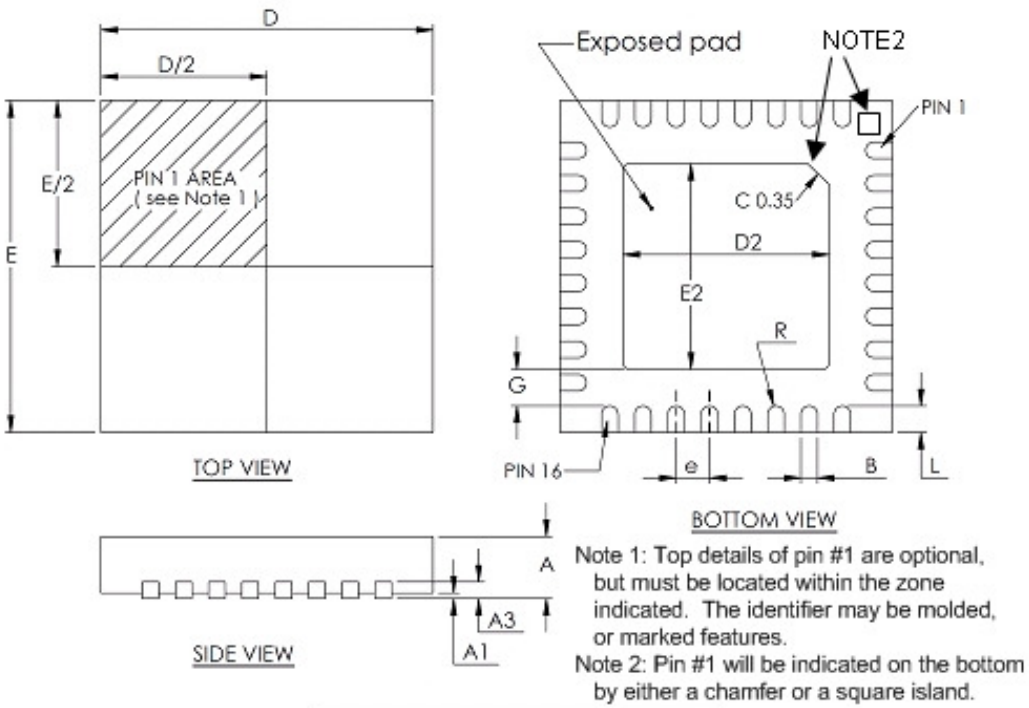
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) – θ_{JA} = 28°C/W, θ_{JC} = 2°C/W



Note 1: Top details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.
Note 2: Pin #1 will be indicated on the bottom by either a chamfer or a square island.

32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e		0.5 REF	
G		0.55 REF	
L	0.30	0.40	0.50
R		0.125 TYP	

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