ICM7231-ICM7234
Numeric/Alphanumeric Triplexed LCD Display Driver

INTERSIL

GENERAL DESCRIPTION

The ICM7231-7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

FEATURES

- **ICM7231: Drives 8 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232: Drives 10 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **ICM7233: Drives 4 Characters of 18 Segments Address and Data Input in Parallel Format**
- **ICM7234: Drives 5 Characters of 18 Segments Address and Data Input in Serial Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display Are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**
- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**
- **Direct Interface to High-Speed Microprocessors**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7231AFIJL	-25°C to +85°C	40 pin CERDIP
ICM7231AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7231BFIJL	-25°C to +85°C	40 pin CERDIP
ICM7231BFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7231CFIJL	-25°C to +85°C	40 pin CERDIP
ICM7231CFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7232AFIJL	-25°C to +85°C	40 pin CERDIP
ICM7232AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7232BFIJL	-25°C to +85°C	40 pin CERDIP
ICM7232BFIPL	-25°C to +85°C	40 pin PLASTIC Dip

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7232CR/D	—	DICE
ICM7232CRIJL	-25°C to +85°C	40 pin CERDIP
ICM7232CRIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7233AEV/KIT		Evaluiation Kit.
ICM7233AF/D	—	DICE
ICM7233AFIJL	-25°C to +85°C	40 pin CERDIP
ICM7233AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7233AF/D	—	DICE
ICM7234AFIJL	-25°C to +85°C	40 pin CERDIP
ICM7234AFIPL	-25°C to +85°C	40 pin PLASTIC Dip

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Note: All typical values have been guaranteed by characterization and are not tested.

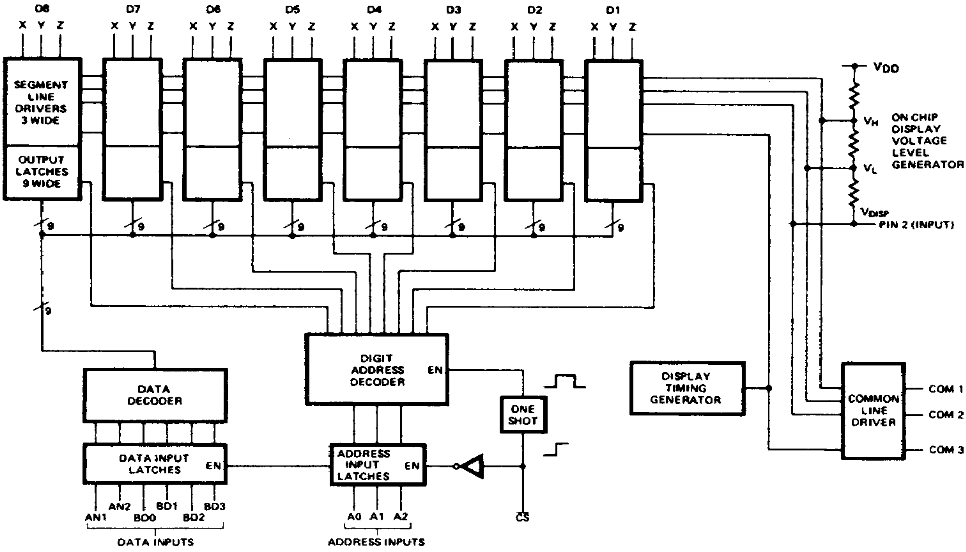

Figure 1: ICM7231 Functional Diagram

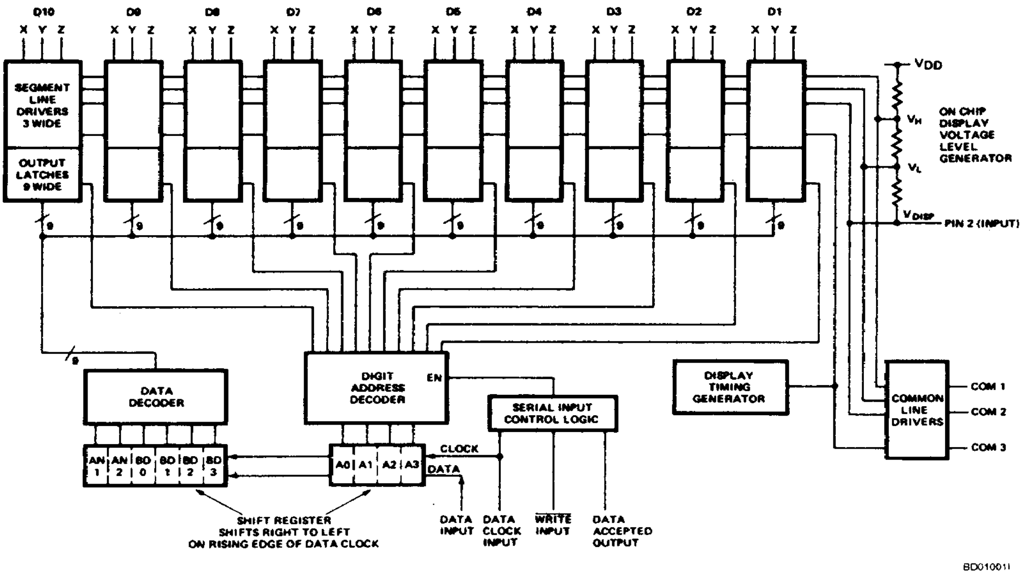

Figure 2: ICM7232 Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

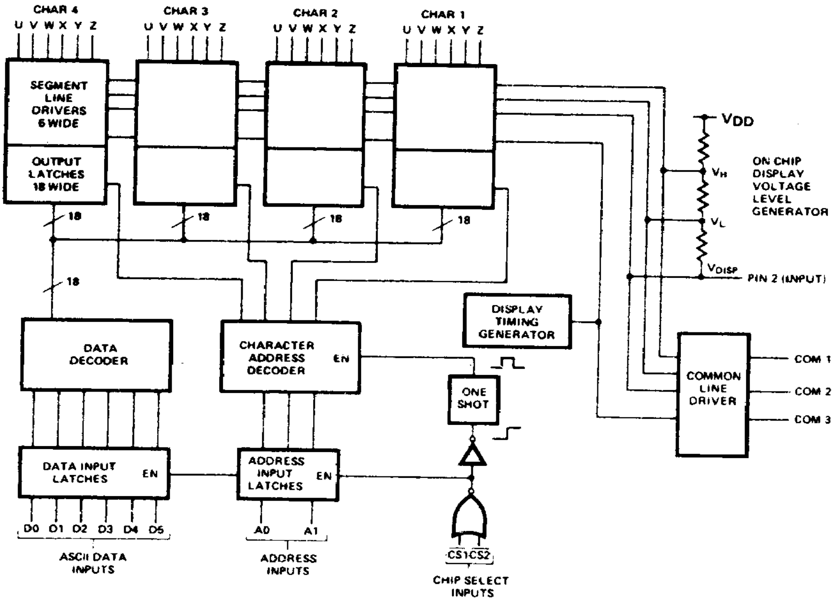

Figure 3: ICM7233 Functional Diagram

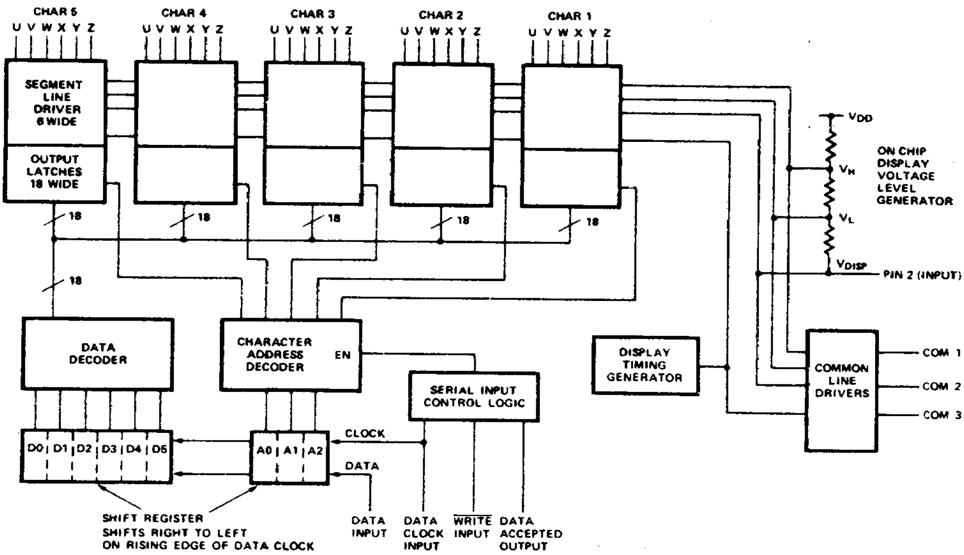

Figure 4: ICM7234 Functional Diagram

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Input Voltage[2] .... $V_{SS} - 0.3 \le V_{IN} \le 6.5$
Display Voltage[2] .... $-0.3 \le V_{DISP} \le +0.3$

Power Dissipation[1] .... 0.5W @ 70°C
Operating Temperature Range .... −25°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. This limit refers to that of the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than −0.3 volts below ground, but may be connected to voltages above V_{DD} but not more than 6.5 volts above V_{SS}.

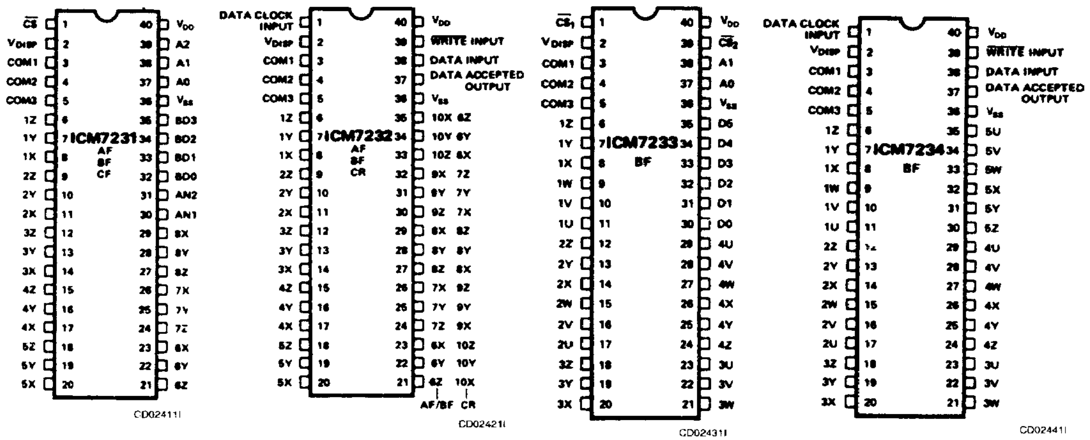

Figure 5: Pin Configuration (Outline dwg PL)

ELECTRICAL CHARACTERISTICS ($V^+ = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -25°C$ to $+85°C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		4.5	> 4	5.5	V
V_{DD}	Data Retention Supply Voltage	Guaranteed Retention at 2V	2	1.6		V
I_{DD}	Logic Supply Current	Current from V_{DD} to Ground excluding Display. $V_{DISP} = 2V$		30	100	μA
I_S	Shutdown Total Current	V_{DISP} Pin 2 Open		1	10	μA
V_{DISP}	Display Voltage Range	$V_{SS} \le V_{DISP} \le V_{DD}$	0		V_{DD}	V
I_{DISP}	Display Voltage Setup Current	$V_{DISP} = 2V$ Current from V_{DD} to V_{DISP} On-Chip		15	30	μA
R_{DISP}	Display Voltage Setup Resistor Value	One of Three Identical Resistors in String	40	75		kΩ
	DC Component of Display Signals	(Sample Test only)		1/4	1	% ($V_{DD} - V_{DISP}$)
f_{DISP}	Display Frame Rate	See Figure 7	60	90	120	Hz
V_{IL}	Input Low Level	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
V_{IH}	Input High Level		2.0			V
I_{ILK}	Input Leakage	ICM7232, ICM7234 Pins 1, 38, 39 (Note 1)		0.1	1	μA
C_{IN}	Input Capacitance			5		pF
V_{OL}	Output Low Level	Pin 37, ICM7232, ICM7234, $I_{OL} = 1mA$,			0.4	V
V_{OH}	Output High Level	$V_{DD} = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
T_{OP}	Operating Temperature Range	Industrial Range	−25		+85	°C

Note: All typical values have been guaranteed by characterization and are not tested.

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AC CHARACTERISTICS (V_{DD} = 5V±10% V_{SS} = 0V, −20°C ≤ T_A ≤ +85°C)

PARALLEL INPUT (ICM7231, ICM7233) See Figure 13

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{cs}	Chip Select Pulse Width	(Note 1)	500	350		ns
t_{ds}	Address/Data Setup Time	(Note 1)	200			ns
t_{dh}	Address/Data Hold Time	(Note 1)	0	−20		ns
t_{ics}	Inter-Chip Select Time	(Note 1)	3			μs

SERIAL INPUT (ICM7232, ICM7234) See Figures 16, 17, 18

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{cl}}$	Data Clock Low Time	(Note 1)	350			ns
t_{cl}	Data Clock High Time	(Note 1)	350			ns
t_{ds}	Data Setup Time	(Note 1)	200			ns
t_{dh}	Data Hold Time	(Note 1)	0	−20		ns
t_{wp}	Write Pulse Width	(Note 1)	500	350		ns
t_{wil}	Write Pulse to Clock at Initialization	(Note 1)	1.5			μs
t_{odl}	Data Accepted Low Output Delay	(Note 1)		200	400	ns
t_{odh}	Data Accepted High Output Delay	(Note 1)		1.5	3	μs
t_{cws}	Write Delay After Last Clock	(Note 1)	350			ns

NOTE 1: For design reference only, not 100% tested.

TABLE OF FEATURES

TYPE NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AF	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7231BF	Code B			
ICM7231CF	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7232AF	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7232B	Code B			
ICM7232CR	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7234AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters
ICM7234BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

Note: All typical values have been guaranteed by characterization and are not tested.

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant ┐ 4 Bit Binary Data Inputs Most Significant ┘	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant ┐ 3 Bit Digit Address Inputs Most Significant ┘	Input Address (See Table 2)	
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

NOTE: 3. $\overline{CS}$ has a special" mid-level" sense ci rcuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant ┐ 6 Bit (ASCII) Data Inputs Most Significant ┘	Input Data See Table 4	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1	37 38	Least Significant ┐ Address Inputs Most Significant ┘	Input Add. See Table 5	
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 3)	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.	

NOTE: $\overline{CS1}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

Note: All typical values have been guaranteed by characterization and are not tested.

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD}) chip is shutdown; oscillator stops, all display pins to V_{DD}.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6–29 6–35	(On ICM7231/33) (On ICM7232/34)	Drive display segments, or columns.
V_{DD}	40	Chip Positive Supply	
V_{SS}	36	Chip Negative Supply	

ICM7231 FAMILY DESCRIPTION

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge.

TRIPLEXED (1/3 MULTIPLEXED) LIQUID CRYSTAL DISPLAYS

Figure 6 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 7 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 7 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 8. Figure 9 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 7.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always 1.92 $V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 10 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS}. This can cause device latchup and destruction of the chip.

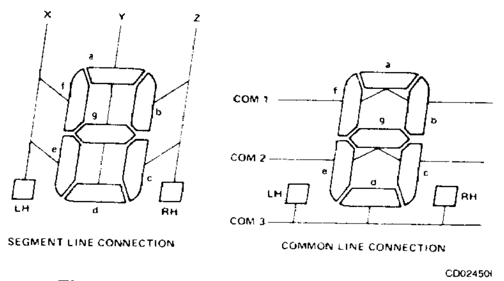

Figure 6: Connection Diagrams for Typical 7-Segment Displays

Note: All typical values have been guaranteed by characterization and are not tested.

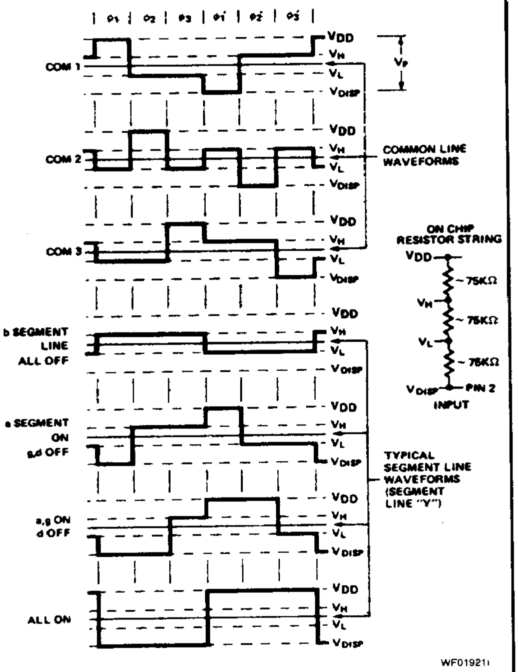

Figure 7: Display Voltage Waveforms

NOTE: ϕ_1, ϕ_2, ϕ_3 — COMMON HIGH WITH RESPECT TO SEGMENT.

$\phi_{1'}$, $\phi_{2'}$, $\phi_{3'}$ — COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND $\phi_{1'}$

COM 2 ACTIVE DURING ϕ_2 AND $\phi_{2'}$

COM 3 ACTIVE DURING ϕ_3 AND $\phi_{3'}$

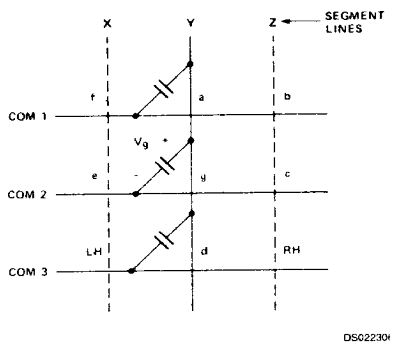

Figure 8: Display Schematic

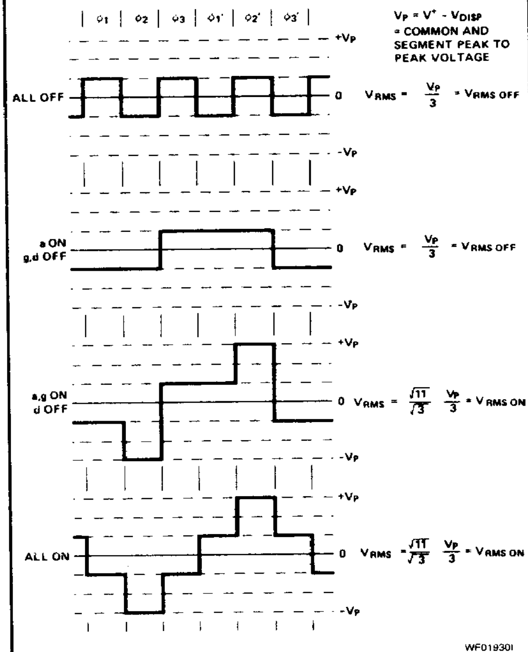

Figure 9: Voltage Waveforms on Segment g(V_g)

$$\text{VOLTAGE CONTRAST RATIO} = \frac{V_{RMS}\ ON}{V_{RMS} OFF} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.

$\phi_{1'}$, $\phi_{2'}$, $\phi_{3'}$ – COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND $\phi_{1'}$

COM 2 ACTIVE DURING ϕ_2 AND $\phi_{2'}$

COM 3 ACTIVE DURING ϕ_3 AND $\phi_{3'}$

8

Note: All typical values have been guaranteed by characterization and are not tested.

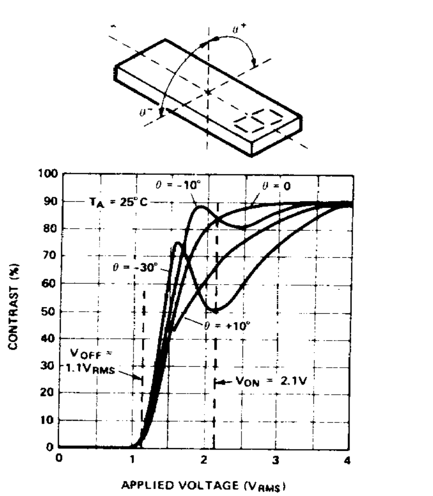

Figure 10: Contrast vs. Applied RMS Voltage

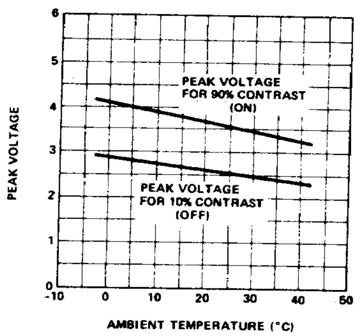

Figure 11: Temperature Dependence of LC Threshold

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (−20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of −7 to −14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 11 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 10.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 12. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

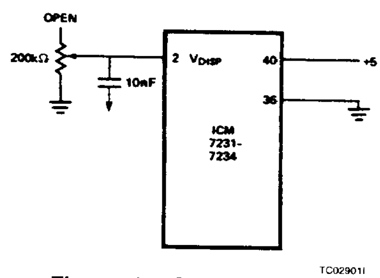

Figure 12: Simple Display Voltage Adjustment

Figure 13(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing

Note: All typical values have been guaranteed by characterization and are not tested.

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through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 10 and 11. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of −2 mV/°C; five in series gives −10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 13(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about −2 mV/°C) is also multipled. The transistor should have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device.

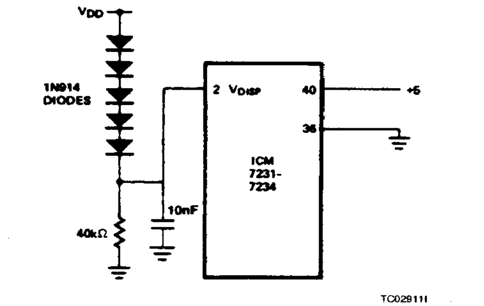

Figure 13(a): String of Diodes

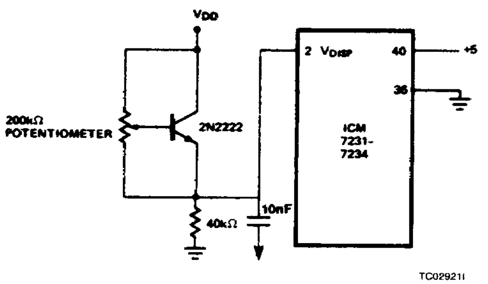

Figure 13(b): Transistor-Multiplier

Figure 13: Diode-based Temperature Compensation

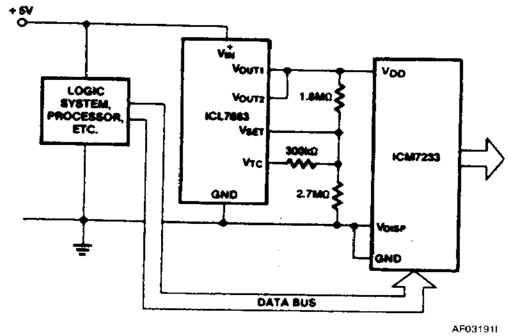

Figure 14: Flexible Temperature Compensation

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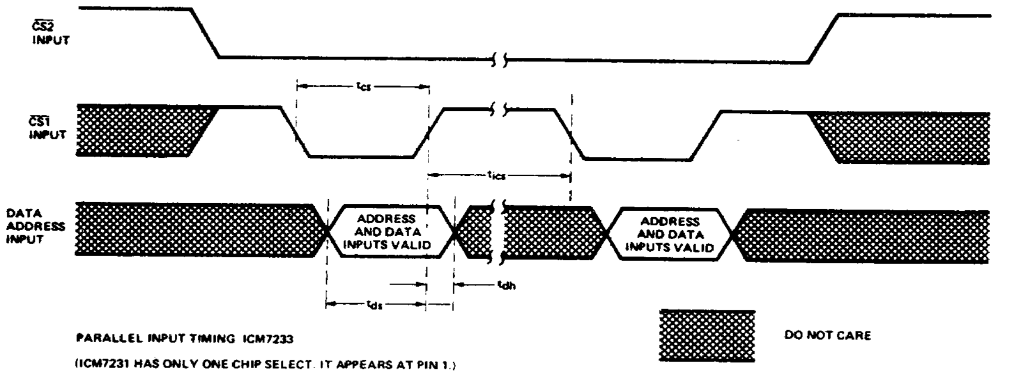


Figure 15: Parallel Input Timing

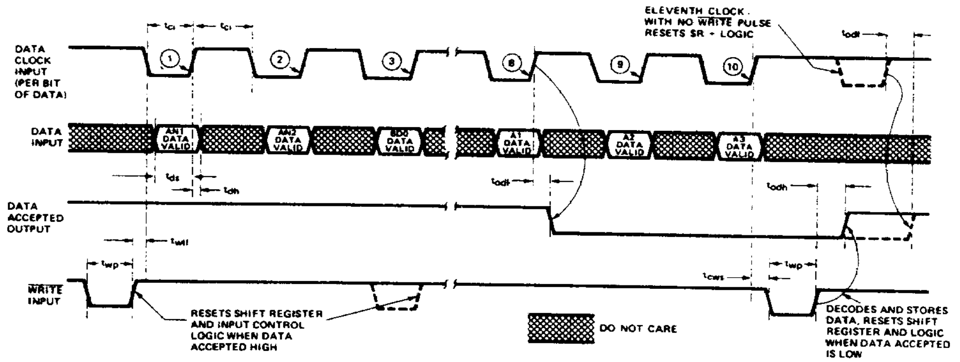


Figure 16: ICM7232 One Digit Input Timing Diagram, Writing Both Annunciators

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS}. The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 14. This circuit allows independent adjustment of both voltage and temperature compensation.

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, (see functional diagrams Figures 1 and 3). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

Note: All typical values have been guaranteed by characterization and are not tested.

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A_0	A_1	A_2	A_3 ENTER LAST

ICM7232 WRITE ORDER

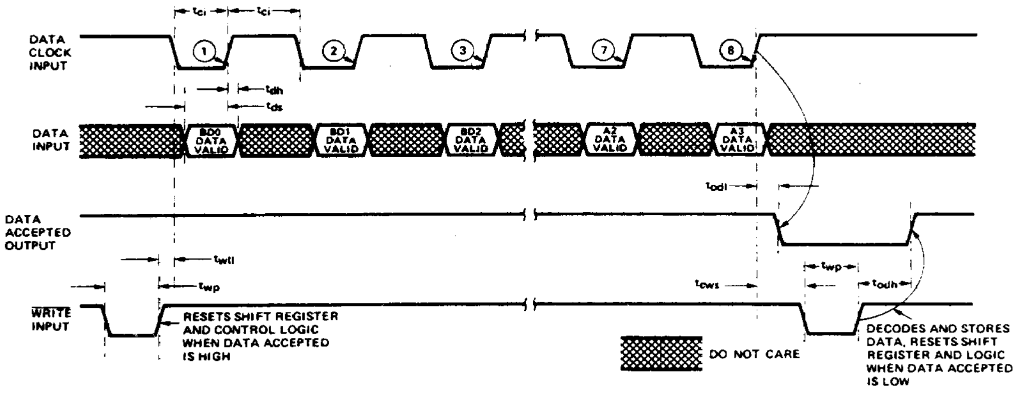


Figure 17: ICM7232 Input Timing Diagram, Leaving Both Annunciators Off

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 15, with the values for setup, hold, and pulse width times shown in the AC Characteristics section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

SERIAL INPUT OF DATA AND ADDRESS (ICM7232, ICM7234)

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to functional diagrams, Figures 2 and 4 and timing diagrams, Figures 16, 17, and 18. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

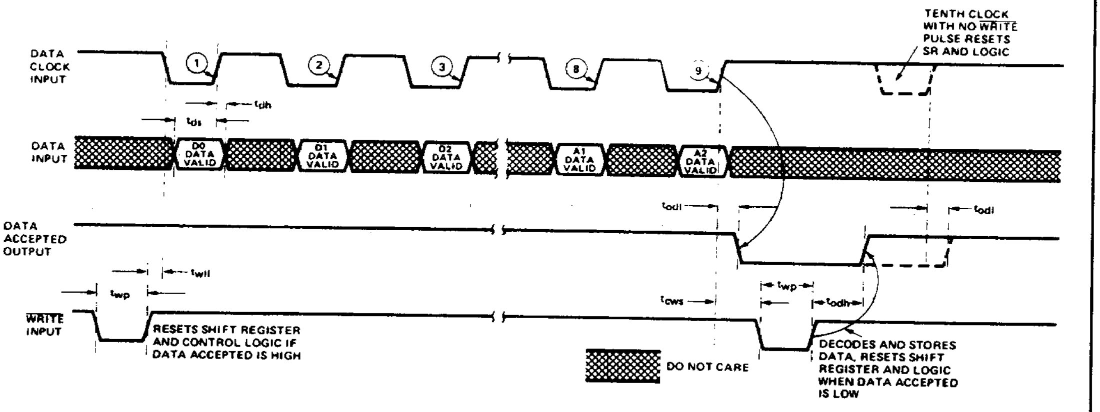
The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 16. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 17.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

Note: All typical values have been guaranteed by characterization and are not tested.



WRITE ORDER	D_0 WRITE FIRST	D_1	D_2	D_3	D_4	D_5	A_0	A_1	A_2 WRITE LAST

Figure 18: ICM7234 One Character Input Timing Diagram

In the ICM7234, nine bits are always required; the control logic is similar, but allows only a $\overline{\text{WRITE}}$ (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 18.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 19. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1). (See Figure 20). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 and ICM7234 are supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 21 with output decoding shown in Table 4.

TABLE 1. BINARY DATA DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

TB000801

Note: All typical values have been guaranteed by characterization and are not tested.

TABLE 2. ADDRESS DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT
ICM7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

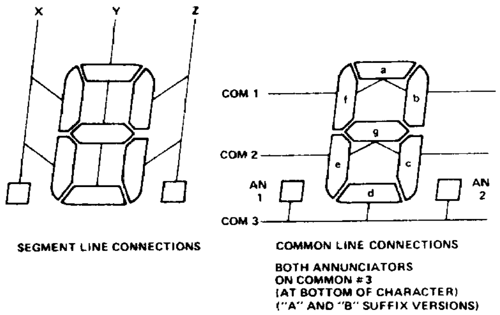
CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0		
0	1		
1	0		
1	1		

TB000901

EVALUATION KITS

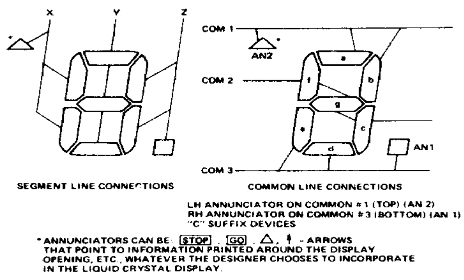
After purchasing a sample of the ICM7231/32/33/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character displays. With the help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

The ICM7233EV/KIT contains the appropriate ICs, a circuit board, a Multiplexed LCD display 16/18 segment, passive components, and miscellaneous hardware.



LC019801

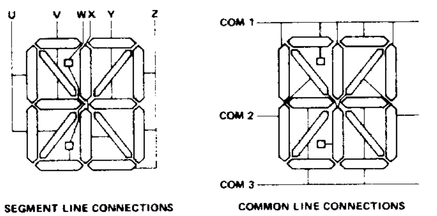
Figure 19: ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)



*ANNUNCIATORS CAN BE: STOP, GO, △, ↑ - ARROWS THAT POINT TO INFORMATION PRINTED AROUND THE DISPLAY OPENING, ETC., WHATEVER THE DESIGNER CHOOSES TO INCORPORATE IN THE LIQUID CRYSTAL DISPLAY.

LC019901

Figure 20: ICM7231 and ICM7232 Display Fonts ("C" Suffix Versions)



LC020001

Figure 21: ICM7233 and ICM7234 Display Font (18-Segment Alphanumeric)

Note: All typical values have been guaranteed by characterization and are not tested.

ICM7231-ICM7234

COMPATIBLE DISPLAYS

Compatible displays are manufactured by:

G.E. Displays Inc., Beechwood, Ohio (216)831-8100 (#356E3R99HJ)

Epson America Inc., Torrance CA (Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA (Custom Displays)

Crystaloid, Hudson, OH

TABLE 4. DATA DECODING 6-BIT ASCII→ 18 SEGMENT (ICM7233/34)

CODE INPUT				DISPLAY OUTPUT				
				D5, D4			A	B
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1	1, 1
0	0	0	0	@	P		0	0
0	0	0	1	A	Q	!	1	1
0	0	1	0	B	R	"	2	2
0	0	1	1	C	S	#	3	3
0	1	0	0	D	T	$	4	4
0	1	0	1	E	U	%	5	5
0	1	1	0	F	V	&	6	6
0	1	1	1	G	W	'	7	7
1	0	0	0	H	X	(	8	8
1	0	0	1	I	Y	)	9	9
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	,	<	
1	1	0	1	M	]	-	=	
1	1	1	0	N	↑	.	>	
1	1	1	1	O	←	/	?	

TB001001

TABLE 5. ADDRESS DECODING (ICM7233/34)

CODE INPUT			DIGIT SELECTED
ICM7234 ONLY			
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

Note: All typical values have been guaranteed by characterization and are not tested.

TYPICAL APPLICATIONS

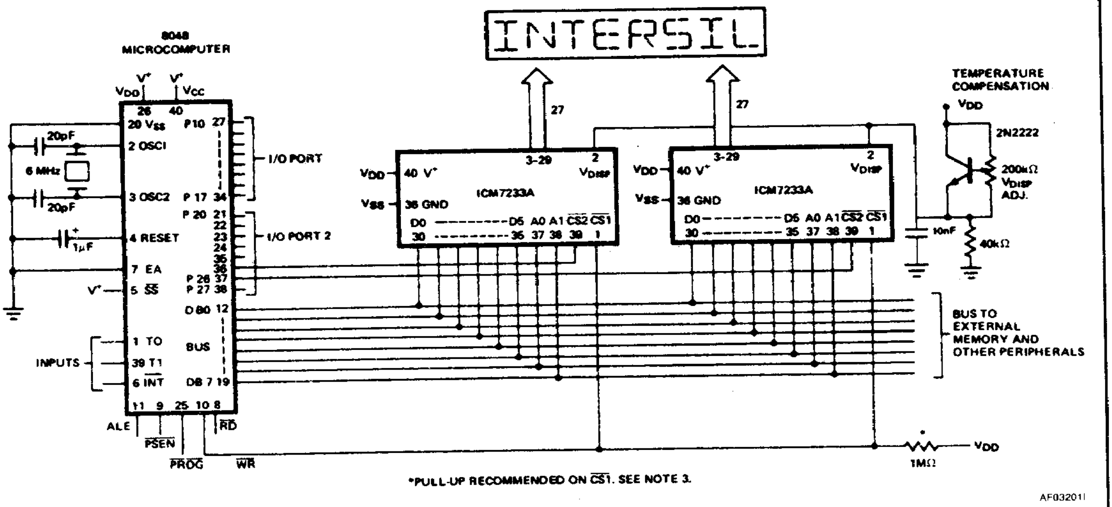


Figure 22: 8048/IM80C48 Microcomputer with 8 Character 16 Segment ASCII Triplex Liquid Crystal Display.

The two bit character address is merged with the data and written to the display driver under the control of the $\overline{WR}$ line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

8

Note: All typical values have been guaranteed by characterization and are not tested.

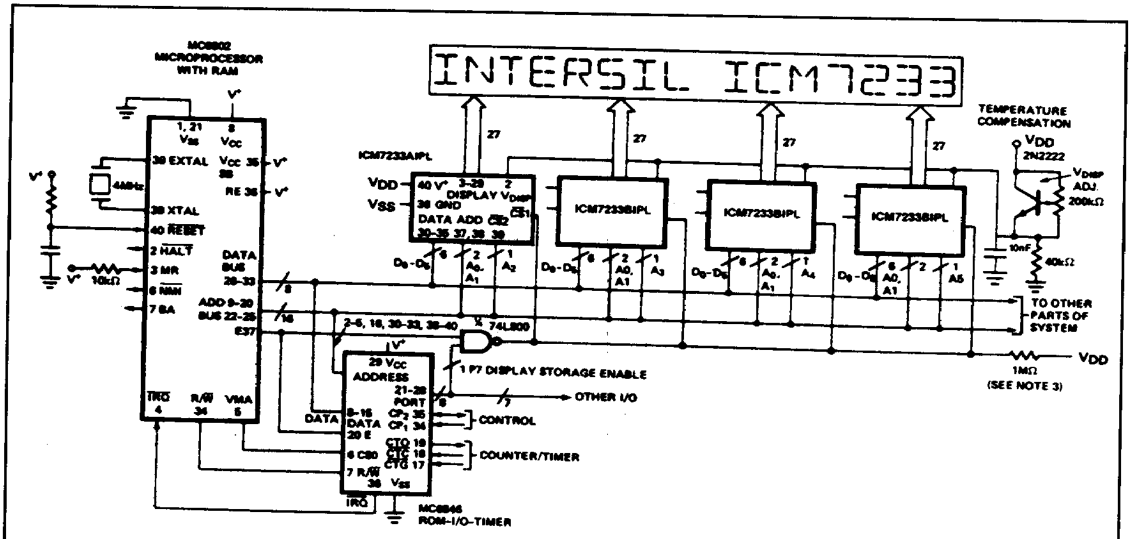


Figure 23: MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed via the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.

Note: All typical values have been guaranteed by characterization and are not tested.

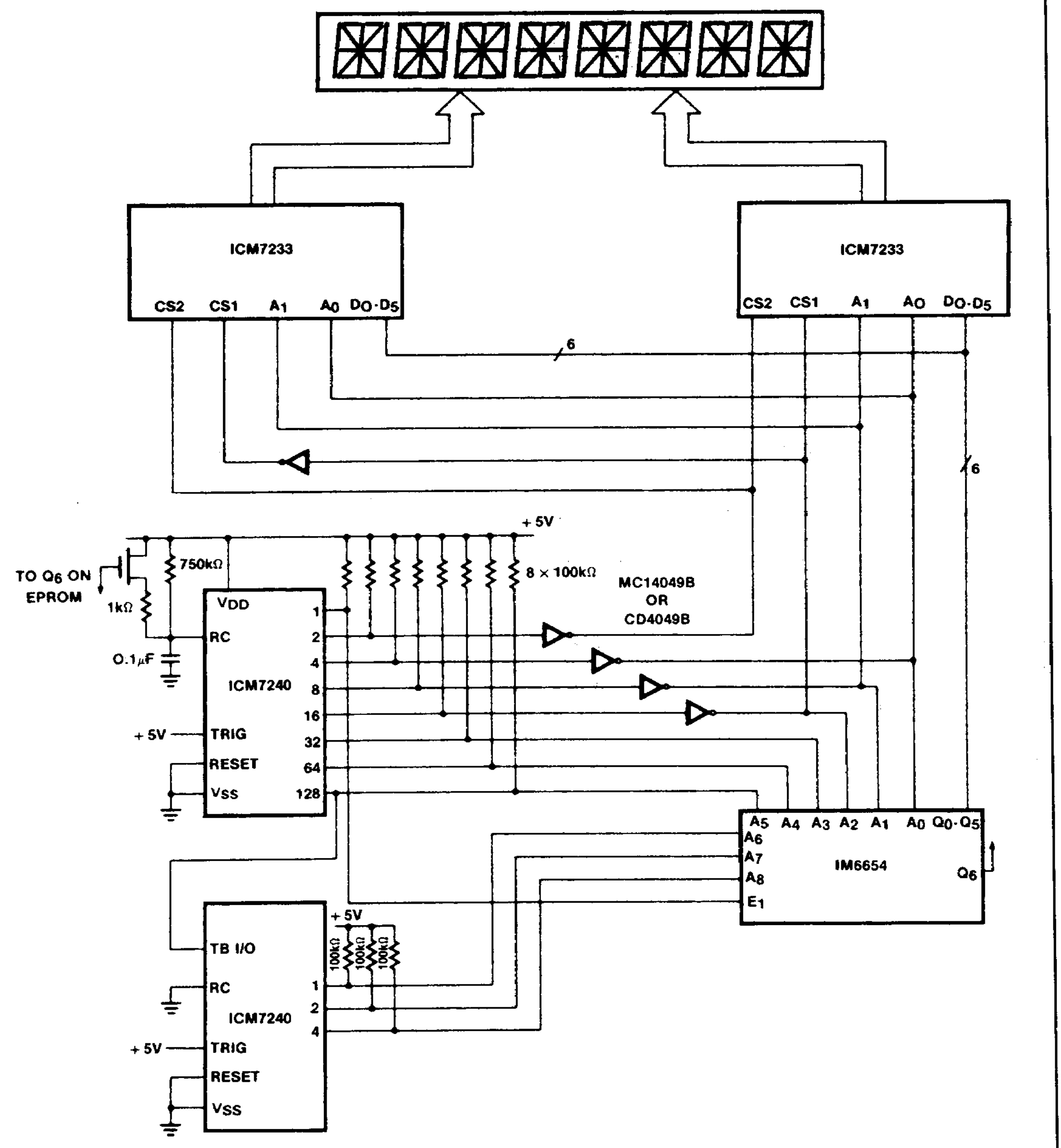
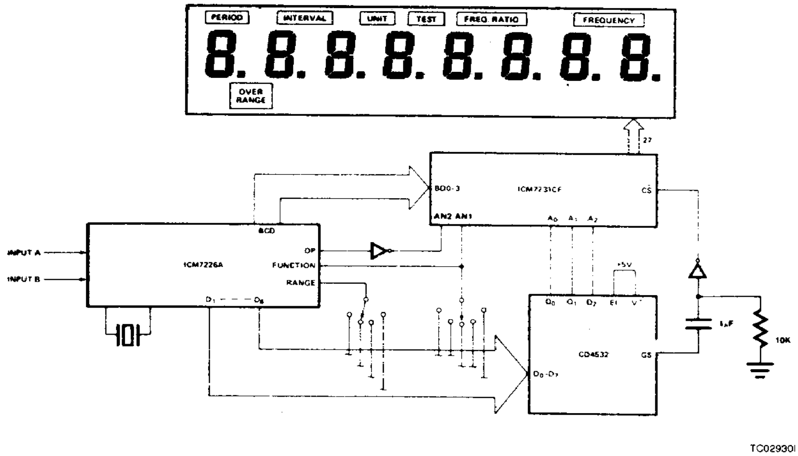


Figure 24: EPROM-Coded Message System.

This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

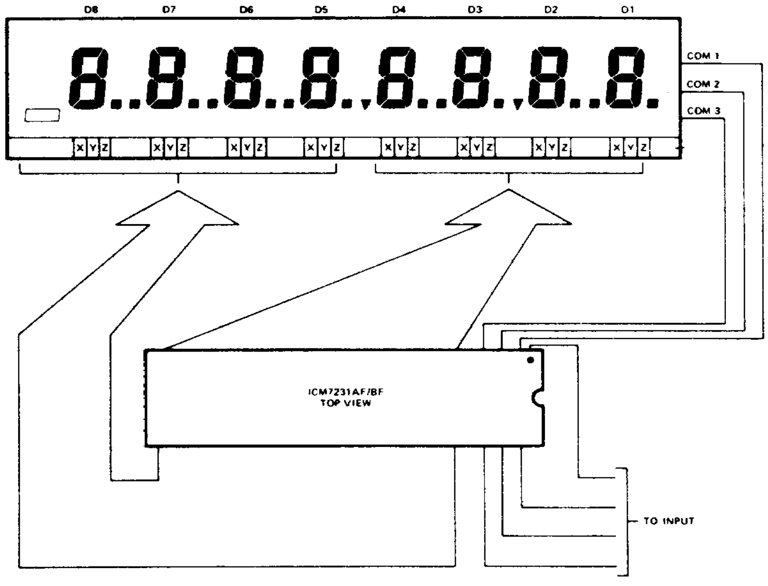
Note: All typical values have been guaranteed by characterization and are not tested.



TC02930I

Figure 25: 10MHz Frequency/Period Pointer with LCD Display.

The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.



CD02460I

Figure 26: "Forward" Pin Orientation and Display Connections

Note: All typical values have been guaranteed by characterization and are not tested.

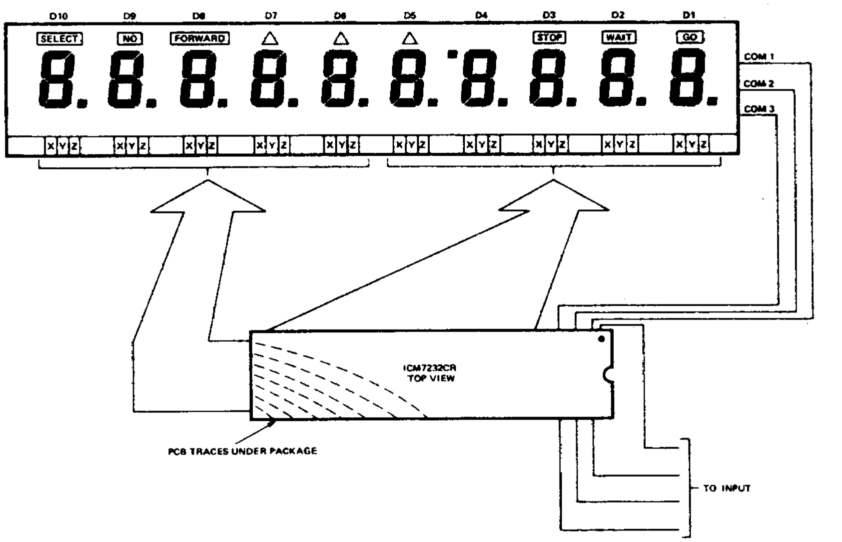


Figure 27: "Reverse" Pin Orientation and Display Connections

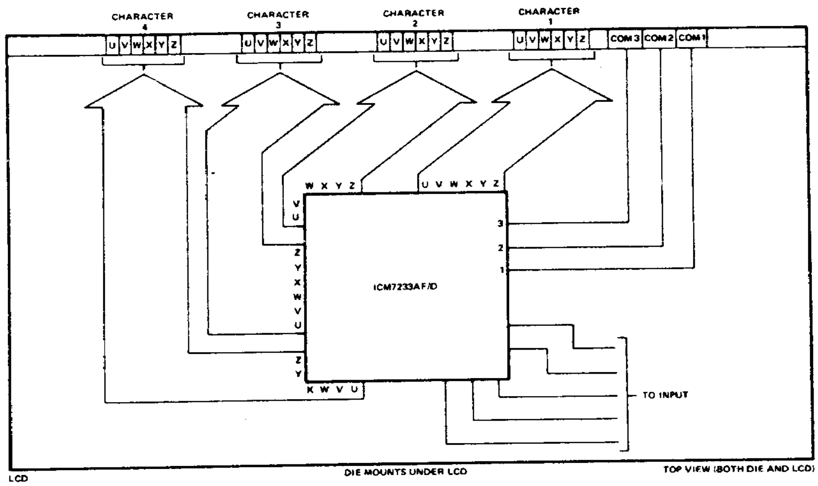


Figure 28: "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections

Note: All typical values have been guaranteed by characterization and are not tested.