*Z86E02 SL 1925*

# *General-Purpose OTP MCU with 14 I/O Lines*

## Product Specification

PS014802-0903

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

**ZiLOG Worldwide Headquarters**
532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

**Document Disclaimer**

# *Table of Contents*

# *List of Figures*

# *List of Tables*

# Architectural Overview

ZiLOG's Z86E02 SL1925 Microcontroller (MCU) is a One-Time Programmable (OTP) member of ZiLOG's single-chip Z8® MCU family that allows easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02 SL1925's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O. One on-chip counter/timer, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

## Z86E02 SL1925 Features

**Table 1.  Z86E02 SL1925 Features**

| Device | OTP (KB) | RAM* (Bytes) | Speed (MHz) |
|---|---|---|---|
| Z86E02 SL1925 | 0.5 | 61 | 8 |

Note:  *General-Purpose.

- 3.5V to 5.5V Operating Range @ 0°C to +70°C

- 4.5V to 5.5V Operating Range @ -40°C to +105°C

- 14 Input/Output Lines

- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 1 timer, 1 software)

- Program Options:
    – Low Noise
    – ROM Protect
    – Auto Latch
    – Watch-Dog Timer (WDT)
    – RC Oscillator

- One Programmable 8-Bit Counter/Timer, with 6-bit Programmable Prescaler

- WDT/Power-On Reset (POR)

- On-Chip Oscillator that accepts XTAL, Ceramic Resonance, LC, RC, or External Clock

- Clock-Free WDT Reset

- Low-Power Consumption (50 m$\Omega$ typical)

- Fast Instruction Pointer (1.5µs @ 8 MHz)

- RAM Bytes (61)

| Connection | Circuit | Device |
|------------|---------|--------|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

## BLOCK DIAGRAMS
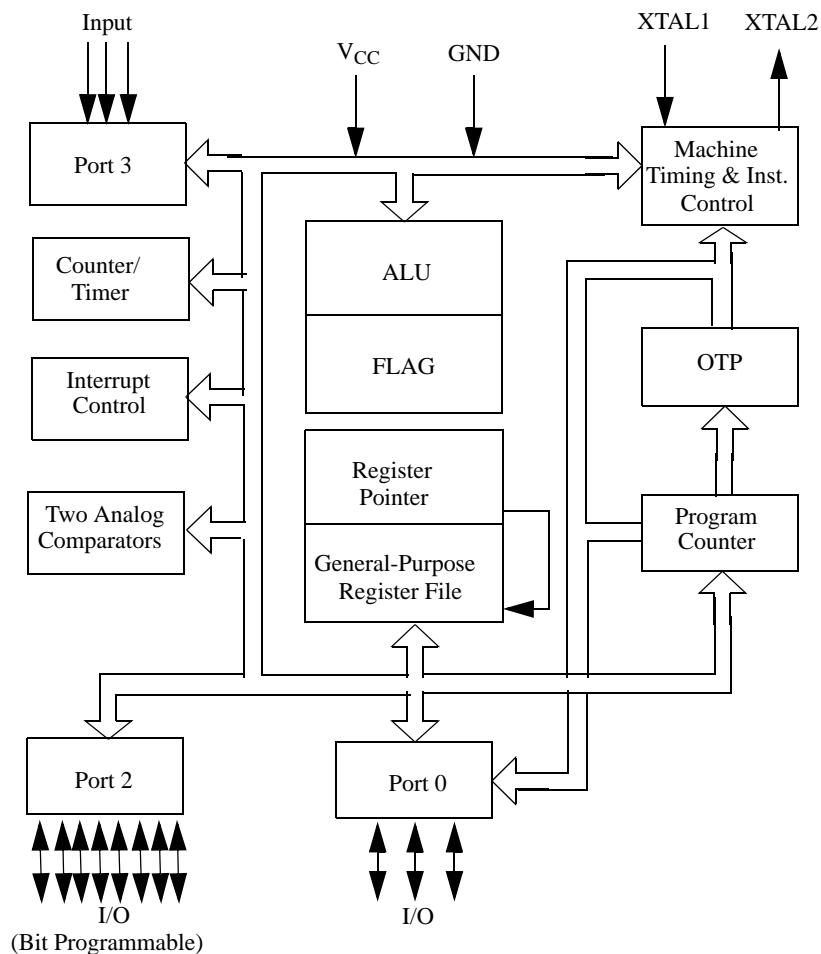


**Figure 1.  Functional Block Diagram**
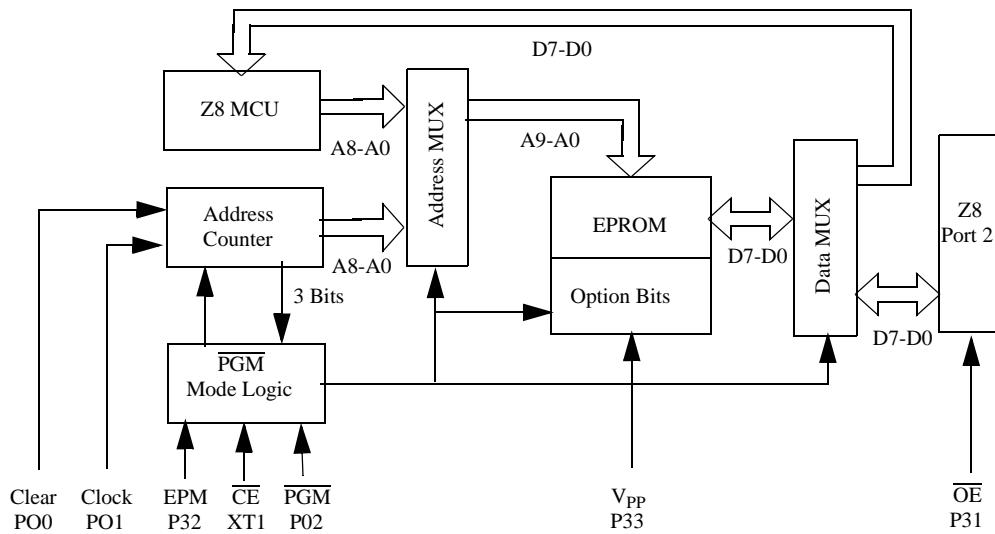
**Figure 2.  EPROM Programming Mode Block Diagram**

## PIN DESCRIPTION

Pin diagrams and identification for the device are displayed in Figure 3 through Figure 6, and in Table 2 through Table 5.

| P24 | 1 | | 18 | P23 |
|---|---|---|---|---|
| P25 | 2 | | 17 | P22 |
| P26 | 3 | | 16 | P21 |
| P27 | 4 | | 15 | P20 |
| $V_{CC}$ | 5 | | 14 | GND |
| XTAL2 | 6 | | 13 | P02 |
| XTAL1 | 7 | | 12 | P01 |
| P31 | 8 | | 11 | P00 |
| P32 | 9 | | 10 | P33 |
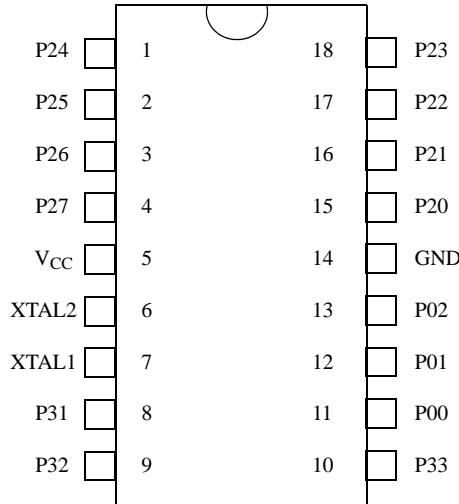
**Figure 3.  18-Pin DIP/SOIC Configuration, STANDARD Mode**

**Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1-4 | P24-P27 | Port 2, Pins 4-7 | Input/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Oscillator Clock | Output |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8 | P31 | Port 3, Pin 1 AN1 | Input |
| 9 | P32 | Port 3, Pin 1 AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11-13 | P00-P02 | Port 0, Pins 0-2 | Input/Output |
| 14 | GND | Ground | |
| 15-18 | P20-P23 | Port 2, Pins 0-3 | Input/Output |
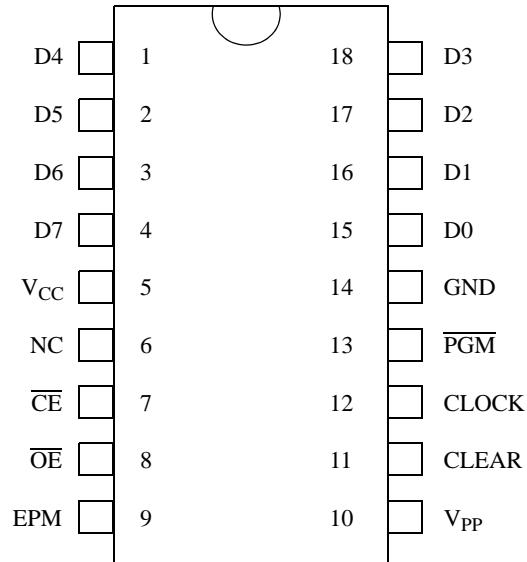
**Figure 4.  18-Pin DIP/SOIC Configuration, EPROM Mode**

**Table 3. 18-Pin DIP/SOIC Pin Identification, EPROM Mode**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1-4 | D4-D7 | Data 4-7 | Input/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | NC | No Connection | |
| 7 | $\overline{CE}$ | Chip Enable | Input |
| 8 | $\overline{OE}$ | Output Enable | Input |
| 9 | EPM | EPROM Program Mode | Input |
| 10 | $V_{PP}$ | Program Voltage | Input |
| 11 | CLEAR | Clear Clock | Input |
| 12 | CLOCK | Address | Input |
| 13 | $\overline{PGM}$ | Program Mode | Input |
| 14 | GND | Ground | |
| 15-18 | D0-D3 | Data 0-3 | Input/Output |
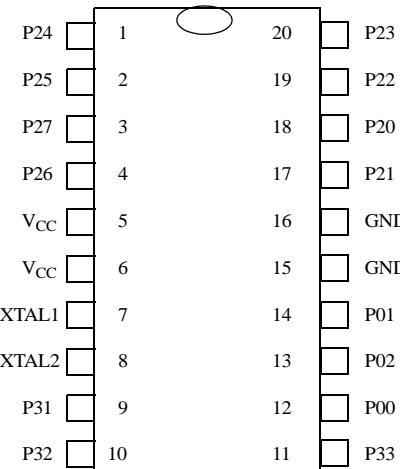
**Figure 5.  20-Pin SSOP Pin Configuration, STANDARD Mode**

**Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode**

| Pin # | Symbol | Function | Direction |
|-------|--------|----------|-----------|
| 1,2 | P24-P25 | Port 2, Pins 4-5 | Input/Output |
| 3 | P27 | Port 2, Pin 7 | Input/Output |
| 4 | P26 | Port 2, Pin 6 | Input/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | $V_{CC}$ | Power Supply | |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8 | XTAL2 | Crystal Oscillator Clock | Output |
| 9 | P31 | Port 3, Pin 1, AN1 | Input |
| 10 | P32 | Port 3, Pin 2, AN2 | Input |
| 11 | P33 | Port 3, Pin 3, REF | Input |
| 12 | P00 | Port 0, Pin 0 | Input/Output |
| 13 | P02 | Port 0, Pin 1 | Input/Output |
| 14 | P01 | Port 0, Pin 1 | Input/Output |
| 15 | GND | Ground | |
| 16 | GND | Ground | |
| 17 | P21 | Port 2, Pin 1 | Input/Output |
| 18 | P20 | Port 2, Pin 0 | Input/Output |
| 19-20 | P22-P23 | Port 2, Pins 2-3 | Input/Output |

| D4 | 1 | 20 | D3 |
| D5 | 2 | 19 | D2 |
| D7 | 3 | 18 | D0 |
| D6 | 4 | 17 | D1 |
| $V_{CC}$ | 5 | 16 | GND |
| $V_{CC}$ | 6 | 15 | GND |
| $\overline{CE}$ | 7 | 14 | CLOCK |
| NC | 8 | 13 | $\overline{PGM}$ |
| $\overline{OE}$ | 9 | 12 | CLEAR |
| EPM | 10 | 11 | $V_{PP}$ |
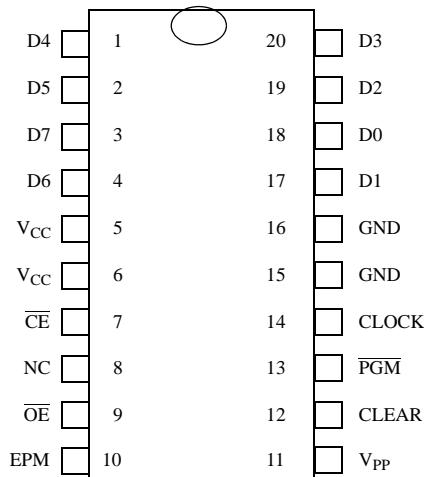
**Figure 6.  20-Pin SSOP Pin Configuration, EPROM Mode**

**Table 5. 20-Pin SSOP Pin Identification, EPROM Mode**

| Pin # | Symbol | Function | Direction |
|-------|--------|----------|-----------|
| 1-2 | D4-D5 | Data 4-5 | Input/Output |
| 3 | D7 | Data 7 | Input/Output |
| 4 | D6 | Data 6 | Input/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | $V_{CC}$ | Power Supply | |
| 7 | $\overline{CE}$ | Chip Enable | Input |
| 8 | NC | No Connection | |
| 9 | $\overline{OE}$ | Output Enable | Input |
| 10 | EPM | EPROM Program Mode | Input |
| 11 | $V_{PP}$ | Program Voltage | Input |
| 12 | CLEAR | Clear Clock | Input |
| 13 | $\overline{PGM}$ | Program Mode | Input |
| 14 | CLOCK | Address | Input |
| 15 | GND | Ground | |
| 16 | GND | Ground | |
| 17 | D1 | Data 1 | Input/Output |
| 18 | D0 | Data 0 | Input/Output |
| 19-20 | D2-D3 | Data 2-3 | Input/Output |

# Electrical Characteristics

## Absolute Maximum Ratings

Stresses greater than those listed on Table 6 may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 m$\Omega$ for the package. See Table 6. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})]$$
$$+ \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}]$$
$$+ \text{sum of } (V_{OL} \times I_{OL})$$

**Table 6. Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Note |
|---|---|---|---|---|
| Ambient Temperature under Bias | -40 | +105 | C | |
| Storage Temperature | -65 | +150 | C | |
| Voltage on any Pin with Respect to $V_{SS}$ | -0.7 | +12 | V | 1 |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$ | -0.3 | +7 | V | |
| Voltage on XTAL1, P31, P32, P33 with respect to $V_{SS}$ | -0.6 | $V_{DD}$+1 | V | 3 |
| Total Power Dissipation | | 462 | m$\Omega$ | |
| Maximum Allowable Current out of $V_{SS}$ | | 300 | mA | |
| Maximum Allowable Current into $V_{DD}$ | | 270 | mA | |
| Maximum Allowable Current into an Input Pin | -600 | +600 | µA | 4 |
| Maximum Allowable Current into an Open-Drain Pin | -600 | +600 | µA | 2 |
| Maximum Allowable Output Current Linked by any I/O Pin | | 20 | mA | |
| Maximum Allowable Output Current Sourced by any I/O Pin | | 20 mA | | |

1. Applies to all pins except where otherwise noted. Maximum current into or out of pin must be ±600 µA.
2. Device pin is not at an output Low state.
3. There is no input protection diode from pin to $V_{DD}$.
4. This excludes XTAL1 and XTAL2.

## Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin See Figure 7.
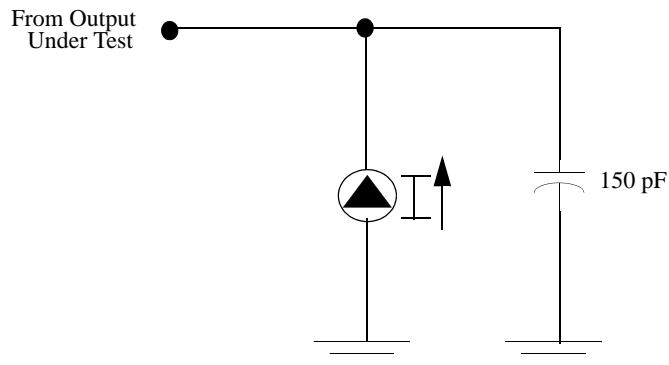
**Figure 7. Test Load Diagram**

## Capacitance

$T_A$ = 25°C, $V_{CC}$ = GND = OV, f = 1.0 MHz, unmeasured pins returned to GND. See Table 7.

**Table 7. Capacitance**

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 10 pF |
| Output capacitance | 0 | 20 pF |
| I/O capacitance | 0 | 25 pF |

# DC Electrical Characteristics

## Standard Temperature Range

Table 8 provides Direct Current characteristics for the Z86E02 SL1925 microcontroller, at a standard ambient temperature range of 0°C to 70°C.

**Table 8. DC Characteristics, Standard Temperature Range**

| | | | | | TA = 0°C to +70°C | | | |
|---|---|---|---|---|---|---|---|---|
| Sym | Parameter | $V_{CC}$ | Min | Max | Typical @ 25°C[1] Units | | Conditions | Notes |
| $V_{INMAX}$ | Max Input Voltage | 3.5V | -12 | 12 | | V | $I_{IN}$ < 250 µA | 2 |
| | | 5.5V | -12 | 12 | | V | $I_{IN}$ < 250 µA | 2 |

**Table 8. DC Characteristics, Standard Temperature Range  (Continued)**

| | | | | | Typical @ | | | |
|---|---|---|---|---|---|---|---|---|
| Sym | Parameter | $V_{CC}$ | Min | Max | 25°C[1] | Units | Conditions | Notes |
| $V_{CH}$ | Clock Input High Voltage | 3.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 3.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 0.8 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 3.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 3.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 0.8 | V | | |
| | | 5.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 3.5V | $V_{CC}$-0.4 | | 3.3 | V | $I_{OH}$ = -2.0 mA | 3 |
| | | 5.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | 3 |
| | | 3.5V | $V_{CC}$-0.4 | | 3.3 | V | $I_{OH}$ = -0.5 mA | 10 |
| | | 5.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -0.5 mA | 10 |
| $V_{OL1}$ | Output Low Voltage | 3.5V | | 0.8 | 0.2 | V | $I_{OL}$ = +4.0 mA | 3 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 3 |
| | | 3.5V | | 0.4 | 0.2 | V | $I_{OL}$=1.0mA | 10 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$=1.0mA | 10 |
| $V_{OL2}$ | Output Low Voltage | 3.5V | | 1.2 | 1.0 | V | $I_{OL}$ = +12 mA | 3 |
| | | 5.5V | | 1.2 | 0.8 | V | $I_{OL}$ = +12 mA | 3 |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | 2.6 | 3.2 | 2.9 | V | @ 4MHz Maximum Internal Clock Frequency | 4 |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 3.5V | -1.0 | 1.0 | | μA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1.0 | 1.0 | | μA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 3.5V | -1.0 | 1.0 | | μA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | -1.0 | 1.0 | | μA | $V_{IN}$ = 0V, $V_{CC}$ | |

TA = 0°C to +70°C

**Table 8. DC Characteristics, Standard Temperature Range  (Continued)**

| Sym | Parameter | $V_{CC}$ | Min | Max | Typical @ 25°C[1] | Units | Conditions | Notes |
|-----|-----------|----------|-----|-----|------------------|-------|------------|-------|
| | | **TA = 0°C to +70°C** | | | | | | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$ - 1.0 | | V | | |
| $I_{CC}$ | Supply Current | 3.5V | 3.5 | | 1.5 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | 7.0 | | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 3.5V | 8.0 | | 3.0 | mA | @ 8 MH | 3,6 |
| | | 5.5V | 11.0 | | 8.2 | mA | @ 8 MHz | 3,6 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 3.5V | 2.5 | | 0.7 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | 4.0 | | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 3.5V | 4.0 | | 1.0 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | 5.0 | | 3.0 | mA | @ 8 MHz | 3,6 |
| $I_{CC}$ | Supply Current (HALT and Low EMI Mode) | 3.5V | 3.5 | | 1.5 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | 7.0 | | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 3.5V | 5.8 | | 2.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | 9.0 | | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 3.5V | 8.0 | | 3.0 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | 11.0 | | 8.2 | mA | @ 4 MHz | 6,10 |
| $I_{CC1}$ | Standby Current (Low EMI Mode) | 3.5V | 1.2 | | 0.4 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | 1.6 | | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 3.5V | 1.5 | | 0.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | 1.9 | | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 3.5V | 2.0 | | 0.8 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | 2.4 | | 3.0 | mA | @ 4 MHz | 6,10 |
| $I_{CC2}$ | Standby Current (STOP Mode) | 3.5V | 10.0 | | 1.0 | µA | WDT is not Running | 6,7,8 |
| | | 5.5V | 10.0 | | 1.0 | µA | WDT is not Running | 6,7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 3.5V | 12.0 | | 3 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | 32.0 | | 16 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

**Table 8. DC Characteristics, Standard Temperature Range  (Continued)**

| Sym | Parameter | $V_{CC}$ | Min | Max | Typical @ 25°C[1] | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{ALH}$ | Auto Latch High Current | 3.5V | -8.0 | | -1.5 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | -16.0 | | -8.0 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

1. Typical values are read at a $V_{CC}$ of 5.0V and $V_{CC}$ of 3.5V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not low EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the $V_{CC}$ or $V_{SS}$ level.
7. If the analog comparator is selected, then the comparator inputs must be at the $V_{CC}$ level.
8. A 10-M pull-up resistor is required in the circuit between the $X_{IN}$ pin to the $V_{CC}$ pin.
9. Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

## Extended Temperature Range

Table 9 provides Direct Current characteristics for the Z86E02 SL1925 microcontroller, at an extended ambient temperature range of -40°C to 105°C.

**Table 9. DC Characteristics, Extended Temperature Range**

TA = -40°C to +105°C

| Sym | Parameter | $V_{CC}$ | Min | Max | Typical @ 25°C[1] | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{INMAX}$ | Max Input Voltage | 4.5V | | 12.0 | | V | $I_{IN} < 250$ µA | 2 |
| | | 5.5V | | 12.0 | | V | $I_{IN} < 250$ µA | 2 |
| $V_{CH}$ | Clock Input High Voltage | 4.5V | $0.8\,V_{CC}$ | $V_{CC}+0.3$ | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | $0.8\,V_{CC}$ | $V_{CC}+0.3$ | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | $V_{SS}-0.3$ | $0.2\,V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}-0.3$ | $0.2\,V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |

**Table 9. DC Characteristics, Extended Temperature Range  (Continued)**

| Sym | Parameter | $V_{CC}$ | TA = -40°C to +105°C | | Typical @ 25°C[1] | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | | | | |
| $V_{IH}$ | Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 4.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| | | 5.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 4.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | 3 |
| | | 5.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$= -2.0 mA | 3 |
| | | 4.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -0.5 mA | 10 |
| | | 5.5V | $V_{CC}$-0.4 | | 4.8 | V | $I_{OH}$ = -0.5 mA | 10 |
| $V_{OL1}$ | Output Low Voltage | 4.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 3 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 3 |
| | | 4.5V | | 0.4 | 0.1 | V | $I_{OL}$=1.0 mA | 10 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$=1.0 mA | 10 |
| $V_{OL2}$ | Output Low Voltage | 4.5V | | 1.0 | 0.3 | V | $I_{OL}$ = +12 mA | 3 |
| | | 5.5V | | 1.0 | 0.3 | V | $I_{OL}$ = +12 mA | 3 |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | 2.3 | 3.5 | 2.9 | V | @ 4 MHz Maximum Internal Clock Frequency | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 4.5V | | -1.0 | 1.0 | µA | $V_{IN}$= 0V, $V_{CC}$ | |
| | | 5.5V | | -1.0 | 1.0 | µA | $V_{IN}$= 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 4.5V | | -1.0 | 1.0 | µA | $V_{IN}$= 0V, $V_{CC}$ | |
| | | 5.5V | | -1.0 | 1.0 | µA | $V_{IN}$= 0V, $V_{CC}$ | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$- 1.5 | | V | | |

**Table 9. DC Characteristics, Extended Temperature Range  (Continued)**

| Sym | Parameter | $V_{CC}$ | TA = -40°C to +105°C | | Typical @ 25°C[1] | Units | Conditions | Notes |
|-----|-----------|-----|-----|-----|-----|-----|-----------|-------|
| | | | Min | Max | | | | |
| $I_{CC}$ | Supply Current | 4.5V | | 7.0 | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | | 7.0 | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 4.5V | | 11.0 | 8.2 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | | 11.0 | 8.2 | mA | @ 8 MHz | 3,6 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 4.5V | | 3.0 | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | | 3.0 | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 4.5V | | 5.0 | 3.0 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | | 5.0 | 3.0 | mA | @ 8 MHz | 3,6 |
| $I_{CC}$ | Supply Current (Low EMI Mode) | 4.5V | | 7.0 | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | | 7.0 | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 4.5V | | 9.0 | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | | 9.0 | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 4.5V | | 11.0 | 8.2 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | | 11.0 | 8.2 | mA | @ 4 MHz | 6,10 |
| $I_{CC1}$ | Standby Current (HALT and Low EMI Mode) | 4.5V | | 1.6 | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | | 1.6 | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 4.5V | | 1.9 | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 5,5V | | 1.9 | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 4.5V | | 2.4 | 3.0 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | | 2.4 | 3.0 | mA | @ 4 MHz | 6,10 |
| $I_{CC2}$ | Standby Current (Stop mode) | 4.5V | | 20 | 1.0 | µA | WDT is not Running | 6,7,8 |
| | | 5.5V | | 20 | 1.0 | µA | WDT is not Running | 6,7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | | 40 | 16 | µA | 0V< $V_{IN}$< $V_{CC}$ | 9 |
| | | 5.5V | | 40 | 16 | µA | 0V< $V_{IN}$< $V_{CC}$ | 9 |

**Table 9. DC Characteristics, Extended Temperature Range  (Continued)**

| Sym | Parameter | $V_{CC}$ | TA = -40°C to +105°C | | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Typical @ 25°C[1] | | | |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | | -20.0 | -8.0 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | | -20.0 | -8.0 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

1.  Typical values are read at a $V_{CC}$ of 5.0V
2.  Port 2, Port 3, and Port 0 only.
3.  STANDARD mode (not Low EMI mode).
4.  These values apply while operating in RUN mode or HALT mode
5.  These values apply while operating in STOP mode
6.  All outputs are unloaded and all inputs are at the $V_{CC}$ or $V_{SS}$ level.
7.  If the analog comparator is selected, then the comparator inputs must be at the $V_{CC}$ level.
8.  A 10-MΩ pull-up resistor is required in the circuit between the XTAL1 pin to the $V_{CC}$ pin.
9.  Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

# AC Electrical Timing Characteristics

Figure 8 illustrates Alternating Current timing for the Z86E02 SL1925 microcontroller.
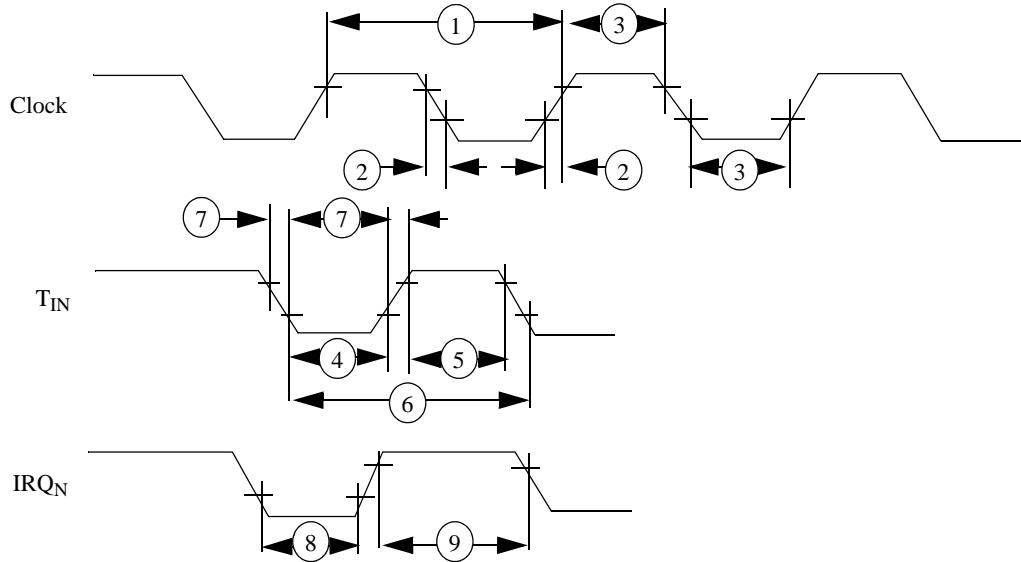


**Figure 8.  AC Electrical Timing**

## STANDARD Mode at Standard Temperature

Table 10 describes timing characteristics in STANDARD mode at standard temperature for the timing diagram noted in Figure 8.

**Table 10. AC Electrical Characteristics, Standard Mode and Temperature**

| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Units | Notes |
|----|--------|-----------|------|-----|-----|-------|-------|
| | | | **TA = 0°C to +70°C** | | | | |
| | | | **8MHz** | | | | |
| 1 | $T_PC$ | Input Clock Period | 3.5V | 125 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | ns | 1 |
| 2 | $T_RC,T_FC$ | Clock Input Rise and Fall Times | 3.5V | | 25 | ns | 1 |
| | | | 5.5V | | 25 | ns | 1 |
| 3 | $T_WC$ | Input Clock Width | 3.5V | 62 | | ns | 1 |
| | | | 5.5V | 62 | | ns | 1 |

**Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)**

| | | | | TA = 0°C to +70°C | | | | |
| | | | | 8MHz | | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 4 | $T_W T_{IN} L$ | Timer Input Low Width | 3.5V | 100 | | ns | 1 |
| | | | 5.5V | 70 | | ns | 1 |
| 5 | $T_W T_{IN} H$ | Timer Input High Width | 3.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1 |
| 6 | $T_P T_{IN}$ | Timer Input Period | 3.5V | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | | 1 |
| 7 | $T_R T_{IN}, T_T T_{IN}$ | Timer Input Rise and Fall Time | 3.5V | | 100 | ns | 1 |
| | | | 5.5V | | 100 | ns | 1 |
| 8 | $T_W IL$ | Interrupt Request Input Low Time | 3.5V | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | ns | 1,2 |
| 9 | $T_W IH$ | Interrupt Request Input High Time | 3.5V | 5TpC | | | 1,2 |
| | | | 5.5V | 5TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay Time before Time-out | 3.5V | 10 | | ms | |
| | | | 5.5V | 5 | | ms | |
| 11 | $T_{POR}$ | Power-On Reset Time | 3.5V | 4 | 36 | ms | |
| | | | 5.5V | 2 | 18 | ms | |

1. Timing reference is 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0
2. Interrupt request through Port 3 (P33-P31)

## STANDARD Mode at Extended Temperature

Table 11 describes timing characteristics in STANDARD mode at extended temperature for the timing diagram noted in Figure 8.

**Table 11. AC Electrical Timing, Standard Mode at Extended Temperature**

| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | | TA = -40°C to +105°C | | | |
| | | | | 8MHz | | | |
| 1 | $T_PC$ | Input Clock Period | 4.5V | 125 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | ns | 1 |
| 2 | $T_RC,T_FC$ | Clock Input Rise and Fall Times | 4.5V | | 25 | ns | 1 |
| | | | 5.5V | | 25 | ns | 1 |
| 3 | $T_WC$ | Input Clock Width | 4.5V | | 62 | ns | 1 |
| | | | 5.5V | | 62 | ns | 1 |
| 4 | $T_WT_{IN}L$ | Timer Input Low Width | 4.5V | 70 | | ns | 1 |
| | | | 5.5V | 70 | | ns | 1 |
| 5 | $T_WT_{IN}H$ | Timer Input High Width | 4.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1 |
| 6 | $T_PT_{IN}$ | Timer Input Period | 4.5V | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | | 1 |
| 7 | $T_RT_{IN}, T_TT_{IN}$ | Timer Input Rise and Fall Time | 4.5V | | 100 | ns | 1 |
| | | | 5.5V | | 100 | ns | 1 |
| 8 | $T_WIL$ | Interrupt Request Input Low Time | 4.5V | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | ns | 1,2 |
| 9 | $T_WIH$ | Interrupt Request Input High Time | 4.5V | 5TpC | | | 1,2 |
| | | | 5.5V | 5TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay Time before Time-out | 4.5V | 5 | | ms | |
| | | | 5.5V | 5 | | ms | |
| 11 | $T_{POR}$ | Power-On Reset Time | 4.5V | 1 | 20 | ms | |
| | | | 5.5V | 1 | 20 | ms | |

1. Timing reference is 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0
2. Interrupt request through Port 3 (P33-P31)

## LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

**Table 12. AC Electrical Timing, Standard Mode at Extended Temperature**

| No | Symbol | Parameter | $V_{CC}$ | 1MHz Min | 1MHz Max | 4MHz Min | 4MHz Max | Units | Notes |
|----|--------|-----------|------|------|------|------|------|-------|-------|
| | | | | **Min** | **Max** | **Min** | **Max** | | |
| 1 | $T_PC$ | Input Clock Period | 3.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | $T_RC, T_FC$ | Clock Input Rise and Fall Times | 3.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | $T_WC$ | Input Clock Width | 3.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4 | $T_WT_{IN}L$ | Timer Input Low Width | 3.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | $T_WT_{IN}H$ | Timer Input High Width | 3.5V | 3TpC | | 3TpC | | | 1 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1 |
| 6 | $T_PT_{IN}$ | Timer Input Period | 3.5V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | $T_RT_{IN}, T_TT_{IN}$ | Timer Input Rise and Fall Time | 3.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | $T_WIL$ | Interrupt Request Input Low Time | 3.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | $T_WIH$ | Interrupt Request Input High Time | 3.5V | 3TpC | | 3TpC | | | 1,2 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay Time before Time-out | 3.5V | 10 | | 10 | | ms | |
| | | | 5.5V | 5 | | 5 | | ms | |

**Table 12. AC Electrical Timing, Standard Mode at Extended Temperature  (Continued)**

| No | Symbol | Parameter | $V_{CC}$ | 1MHz Min | 1MHz Max | 4MHz Min | 4MHz Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | **1MHz** | | **4MHz** | | | |
| 11 | $T_{POR}$ | Power-On Reset Time | 3.5V | 2 | 18 | 2 | 18 | ms | |
| | | | 5.5V | 2 | 18 | 2 | 18 | ms | |

Note: TA = 0°C to +70°C

1.  Timing reference is 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0
2.  Interrupt request through Port 3 (P33-P31)

## LOW EMI Mode at Extended Temperature

Table 13 describes timing characteristics in LOW EMI mode at extended temperature for the timing diagram noted in Figure 8.

**Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature**

| No | Symbol | Parameter | Vcc | 1MHz Min | 1MHz Max | 4MHz Min | 4MHz Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | **1MHz** | | **4MHz** | | | |
| 1 | $T_PC$ | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | $T_RC, T_FC$ | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | $T_WC$ | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4 | $T_WT_{IN}L$ | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | $T_WT_{IN}H$ | Timer Input High Width | 4.5V | 3TpC | | 3TpC | | | 1 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1 |
| 6 | $T_PT_{IN}$ | Timer Input Period | 4.5V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | $T_RT_{IN}, T_TT_{IN}$ | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |

Note: TA = 0°C to +70°C

**Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature  (Continued)**

| No | Symbol | Parameter | Vcc | 1MHz | | 4MHz | | Units | Notes |
|----|--------|-----------|-----|------|-----|------|-----|-------|-------|
| | | | | **TA = 0°C to +70°C** | | | | | |
| | | | | Min | Max | Min | Max | | |
| 8 | $T_WIL$ | Interrupt Request Input | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | $T_WIH$ | Interrupt Request Input | 4.5V | 3TpC | | 3TpC | | | 1,2 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay  Time for Time-out | 4.5V | 5 | | 5 | | ms | |
| | | | 5.5V | 5 | | 5 | | ms | |
| 11 | $T_{POR}$ | Power-On Reset Time | 4.5V | 1 | 20 | 1 | 20 | ms | |
| | | | 5.5V | 1 | 20 | 1 | 20 | ms | |

1. Timing reference is 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0
2. Interrupt request through Port 3 (P33-P31)

## Low-EMI Mode

The device can be programmed to operate in a LOW EMI EMISSION mode by means of a OTP bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical

- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time

- Output drivers typically exhibit resistances of 200 ohms

- Oscillator divide-by-two circuitry eliminated

The LOW EMI mode is a OTP programmable option to be selected by the customer at the time of Device Programming.

## Software Work Around on the Z86CCP01ZEM Emulator to Emulate Low EMI Mode

```
SWFIXLEMI:          PUSH RP
                    LD RP, #0Fh
                    LD R12, #00110110B
                    LD R0,#11010111B
                    POP RP
```

# Pin Functions

## EPROM Mode

**D7–D0 Data Bus.** Data can be read from, or written to, the EPROM through this data bus.

**$V_{CC}$ Power Supply.** It is typically 5V during all EPROM Read Mode and typically 6.4V during other modes (PROGRAM, PROGRAM VERIFY, etc.).

**$\overline{CE}$ Chip Enable (active Low).** This pin is active during EPROM READ mode, PROGRAM mode, and PROGRAM VERIFY mode.

**$\overline{OE}$ Output Enable (active Low).** This pin drives the Data Bus direction. When this pin is Low, the data bus is output. When High, the data bus is input. This pin must toggle for each data output read.

**EPM EPROM Program Mode.** This pin controls the selection of EPROM operation modes by applying different voltages.

**$V_{PP}$ Program Voltage.** This pin supplies the program voltage.

**Clear (active High).** This pin resets the internal address counter at the High level.

**Clock Address Clock.** This pin is a clock input. The internal address counter increases by one count with one clock cycle.

**$\overline{PGM}$ Program Mode (active Low).** A Low level at this pin programs the data to the EPROM through the data bus.

## Pin Function Changes in EPROM Mode

With the exception of $V_{CC}$ and GND, the Z8® changes all of its pin functions in EPROM mode. $X_{OUT}$ offers no function; $X_{IN}$ functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as $V_{PP}$ P00 functions as CLEAR, P01 functions as CLOCK, and P02 functions as $\overline{PGM}$. Please refer to Program Memory for additional EPROM mode descriptions.

## Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above $V_{CC}$ occur on the XTAL1 pin ($\overline{OE}$).

In addition, processor operation of Z8® OTP devices maybe affected by excessive noise surges on the P33 ($V_{PP}$), XTAL1 ($\overline{CE}$), P32 (EPM), P31 ($\overline{OE}$) pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to $V_{CC}$.
- Adding a capacitor to the affected pin.

> **Note:** Programming the EPROM/Test Mode Disable option prevents accidental entry into EPROM Mode or Test Mode.

## STANDARD Mode

**XTAL1, XTAL2.** Crystal In, Crystal Out (time-based input and output, respectively). These pins connect an external parallel-resonant crystal, resonator, RC, LC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

**Port 0, P02–P00.** Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 9).

**Auto Latch.** The Auto Latch places valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch sets the ports to an undetermined state of 0 or 1. The default condition is AUTO LATCH ENABLED. The Auto Latch can be disabled by programming the AUTO LATCH DISABLE option bit.
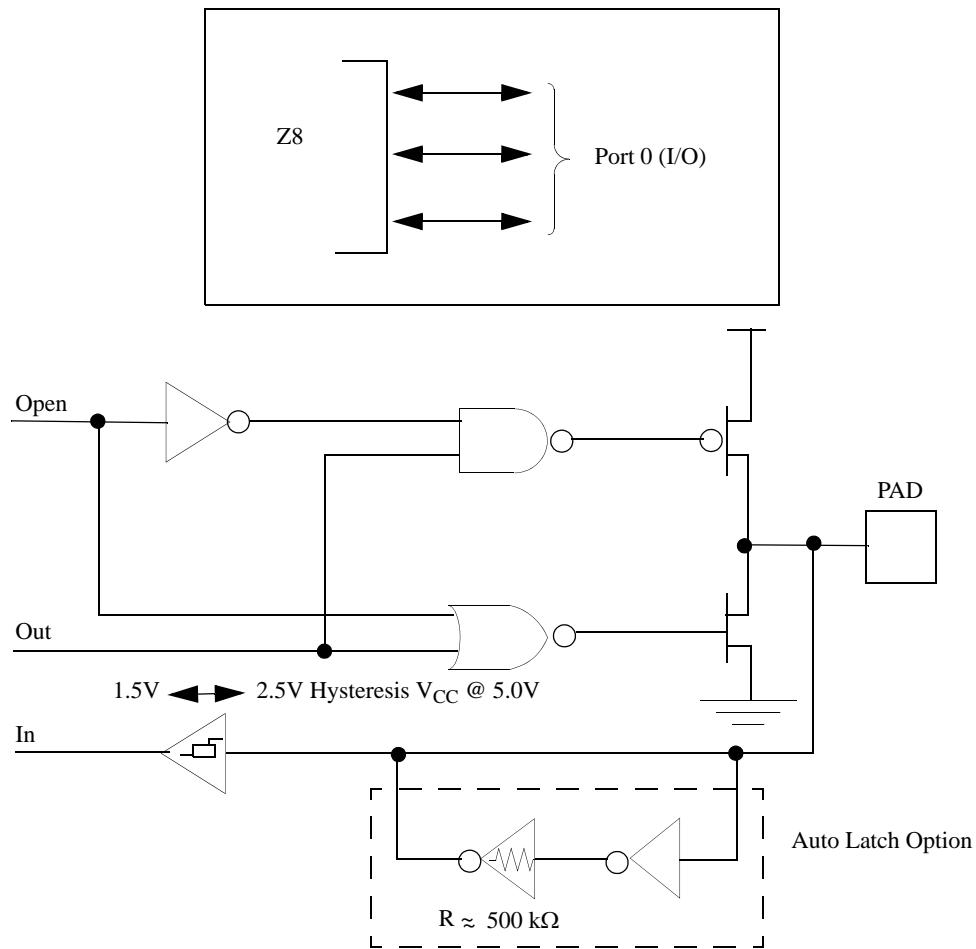
**Figure 9.  Port 0 Configuration**

**Port 2, P27–P20.** Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).
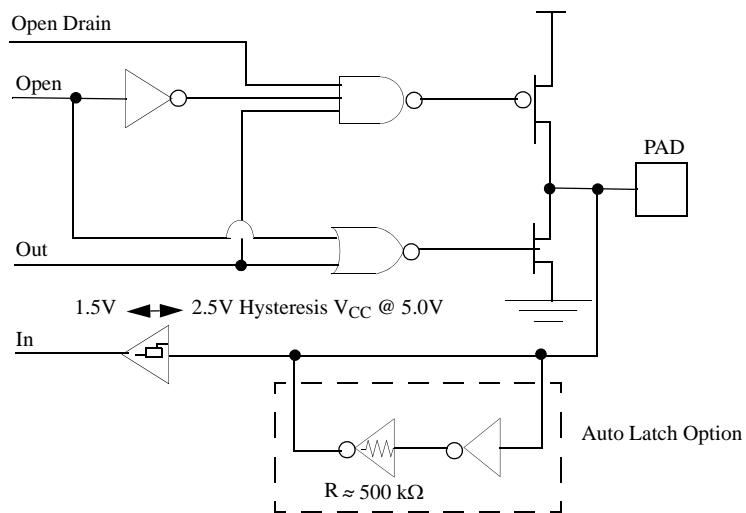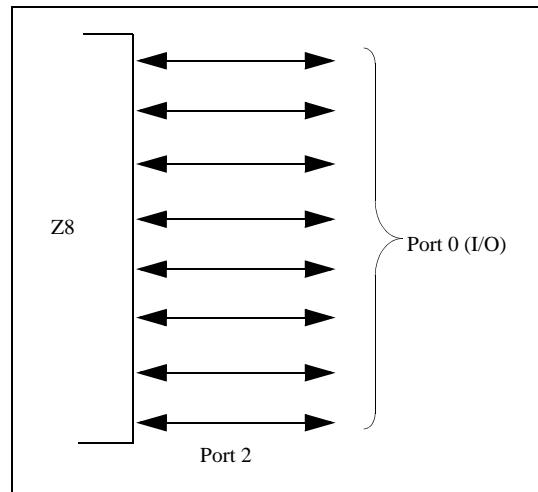
**Figure 10.  Port 2 Configuration**

**Port 3, P33–P31.** Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal $T_{IN}$ (Figure 11).

$0$ = Digital
$1$ = Analog

R247 = P3M

D1

PAD

P31 (AN1)

DIG.

ANL.

$T_{IN}$
P31 Data Latch
IRQ2

PAD

P32 (AN2)

PAD

P33 (REF)

IRQ3
P32 Data Latch
IRQ0

P33 Data Latch
IRQ1

$V_{CC}$

IRQ0,1,2 = Falling Edge Detection
IRQ3      = Rising Edge Detection
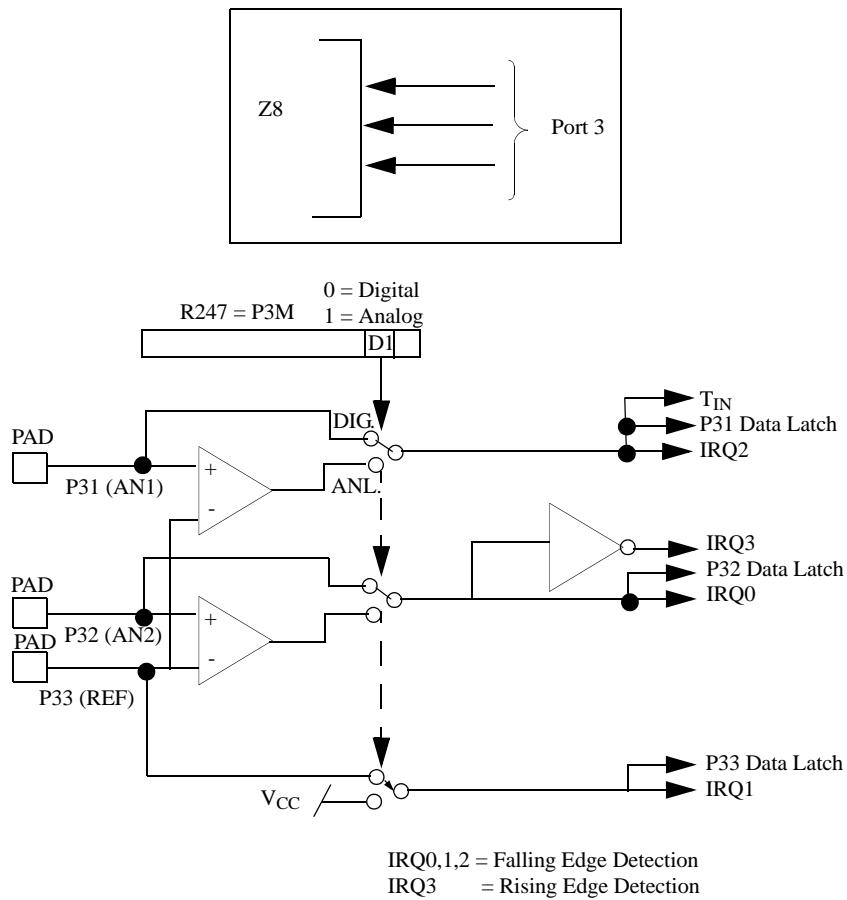
**Figure 11.  Port 3 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, AID conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4 V when the $V_{CC}$ is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt gener-

ation, Port 3 data inputs, or T$_{IN}$ through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

The comparator requires two NOPs to be stable after setting the enable bit. ZiLOG recommends that interrupts IRQ0, IRQ1, and IRQ2 be disabled before setting the enable bit. After enabling the comparator, IRQ0, IRQ1, and IRQ2 should be cleared prior to re-enabling the interrupts. ZiLOG also recommends clearing these interrupts when disabling the comparator.

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1.  Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.

2.  Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1.  Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.

2.  Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX          Push RP
                    LD RP, #0Fh
                    LD R0, #0FFh
                    POP RP
```

# Functional Description

The following special functions are incorporated into the Z8® devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

## RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

### Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, then starts program execution at address 000Ch (Figure 12). The Z8® control registers' reset value is indicated in Table 14.
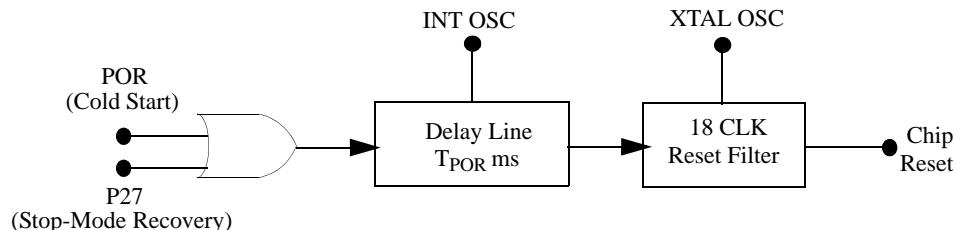


**Figure 12.  Internal Reset Configuration**

**Table 14. Z8® Control Registers Reset Values***

| Address | Register | D7 | D6 | D5 | D4 | D3 | D2 | DI | D0 | Comments |
|---------|----------|----|----|----|----|----|----|----|----|----------|
| | | Reset Condition | | | | | | | | |
| FFh | SPL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FDh | RP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FCh | FLAGS | U | U | U | U | U | U | U | U | |
| FBh | IMR | 0 | U | U | U | U | U | U | U | |
| FAh | IRQ | U | U | 0 | 0 | 0 | 0 | 0 | 0 | IRQ3 is used for positive edge detection |
| F9h | IPR | U | U | U | U | U | U | U | U | |
| F8h* | P01M | U | U | U | 0 | U | 1 | 0 | 1 | |
| F7h* | P3M | U | U | U | 0 | U | U | 0 | 0 | |
| F6h* | P2M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Inputs after reset |
| F3h | PRE1 | U | U | U | 0 | U | U | 0 | 0 | |
| F2h | T1 | U | U | U | 0 | U | U | U | U | |
| F1h | TMR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 14 and the user must avoid bus contention on the port pins or it may affect device reliability

A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows $V_{CC}$ and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out (in Halt mode)

**Watch-Dog Timer Reset**

The WDT is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

## Program Memory

The Z86E02 SL1925 addresses up to 512B of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–511 are on-chip one-time programmable EPROM.

| | |
|---|---|
| 511 | |
| Location of First Byte of Instruction Executed After RESET | On-Chip ROM |
| 12 | |
| 11 | IRQ5 |
| 10 | IRQ5 |
| 9 | IRQ4 |
| 8 | IRQ4 |
| 7 | IRQ3 |
| 6 | IRQ3 |
| 5 | IRQ2 |
| 4 | IRQ2 |
| 3 | IRQ1 |
| 2 | IRQ1 |
| 1 | IRQ0 |
| 0 | IRQ0 |

Interrupt Vector (Lower Byte)

Interrupt Vector (Upper Byte)
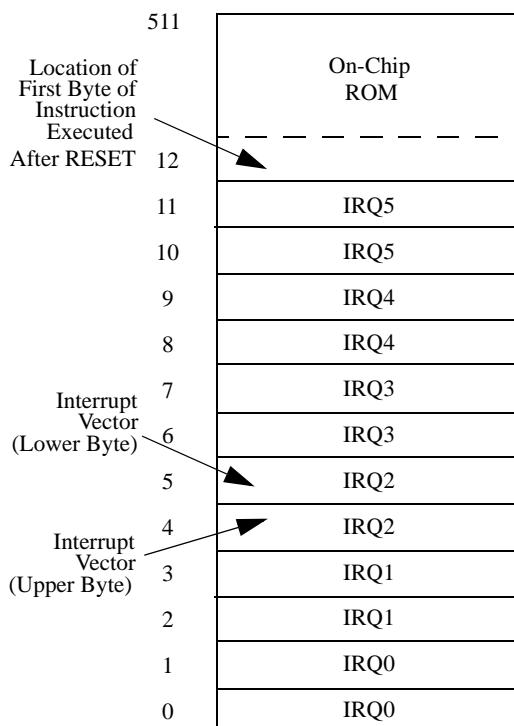
**Figure 13.  Program Memory Map**

## Register File

The Register File consists of three I/O port registers, 61 general-purpose registers, and 14 control and status registers R0, R2-R3, R4–R63, R254 and R241–R253, and R255, respectively (Figure 14). General-purpose registers occupy the 04h to 3Fh address space. I/O ports are mapped as per the existing CMOS Z8.

| Location | | Identifiers |
|---|---|---|
| 255(FFh) | Stack Pointer (Bits 7-0) | SPL |
| 254(FEh) | General-Purpose Register | GPR |
| 253(FDh) | Register Pointer | RP |
| 252(FCh) | Program Control Flags | Flags |
| 251(FBh) | Interrupt Mask Register | IMR |
| 250(FBh) | Interrupt Request Register | IRQ |
| 249(FAh) | Interrupt Priority Register | IRP |
| 248(F8h) | Ports 0-1 Mode | P01M |
| 247(F7h) | Port 3 Mode | P3M |
| 246(F6h) | Port 2 Mode | P2M |
| 245(F5h) | Reserved | Reserved |
| 244(F4h) | Reserved | Reserved |
| 243(F3h) | T1 Prescaler | PRE1 |
| 242(F2h) | TimerCounter1 | T1 |
| 241(F1h) | Timer Mode | TMR |
| 240(F0h)<br>64(40h) | Not Implemented | |
| 63(30h)<br><br>4(04h) | General-Purpose Registers | |
| 3(03h) | Port 3 | P3 |
| 2(02h) | Port 2 | P2 |
| 1(01h) | Reserved | Reserved |
| 0(00h) | Port 0 | P0 |

**Figure 14.  Register File**

The Z8® instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing short 4-bit register addressing mode using the Register Pointer.

In the 4-bit address mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 15) addresses the starting location of the active working-register group.

Must be 0

FDh | r7 r6 r5 r4 | r3 r2 r1 r0 | R253 (Register Pointer)

This upper nibble of the register file addresses provided by the register pointer specifies the active working-register group.

FF

F0 — R15 to R0

The lower nibble of the register file addresses provided by the instruction points to the specified register.

40
3F
    Specified Working
30  Register Group
2F
20
1F
    Register Group 1 — R15 to R0
10
0F
    Register Group 0 — R15 to R4*
    I/O Ports — R3 to R0
00

\* Expanded RegisterGroup [0] is selected in this figure
  by handling bits D3 to D0 as "0" in Register R253(RP).

**Figure 15.  Register Pointer**

## Stack Pointer

The Z8® features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers from 04h to 3Fh.

## General-Purpose Registers (GPR)

These registers are undefined after the device is powered up. The registers keep their most recent value after any reset, as long as the reset occurs in the $V_{CC}$ volt-age-specified operating range.

▶ **Note:** Register R254 is designated as a general-purpose register and is set to 00h after any reset or Stop-Mode Recovery.

## Counter/Timer

There is one 8-bit programmable counter/timer (T1), driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources (Figure 16).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode).

The counter, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The TIMER mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.
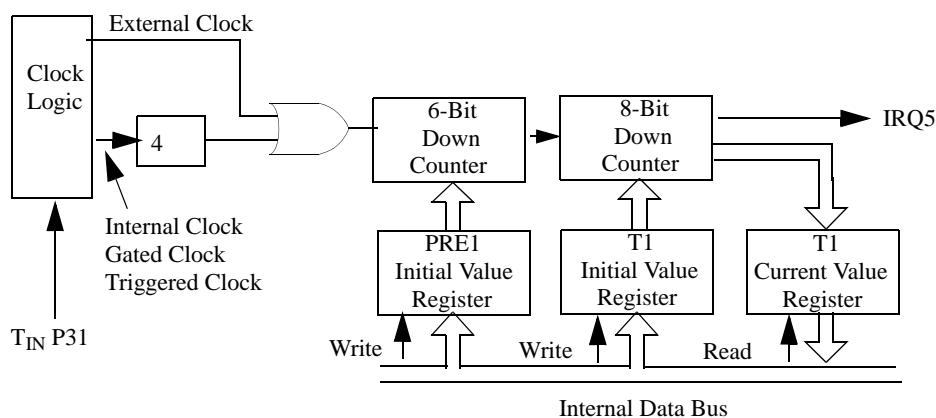


**Figure 16.  Counter/Timer Block Diagram**

## Interrupts

The Z8® features six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN 1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), by software, and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Interrupt Types, Sources, and Vectors).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

▶ **Note:** The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.

2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.

2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX              Push RP
                        LD RP, #0Fh
                        LD R0, #0FFh
                        POP RP
```

**Table 15. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|------|--------|-----------------|----------|
| IRQ0 | AN2(P32) | 0,1 | External (F) Edge |
| IRQ1 | REF(P33) | 2,3 | External (F) Edge |
| IRQ2 | AN1 (P31) | 4,5 | External (F) Edge |
| IRQ3 | AN2 (P32) | 6,7 | External (R) Edge |
| IRQ4 | Software | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |
| Note: Note: F = Falling edge triggered: R = Rising edge triggered | | | |
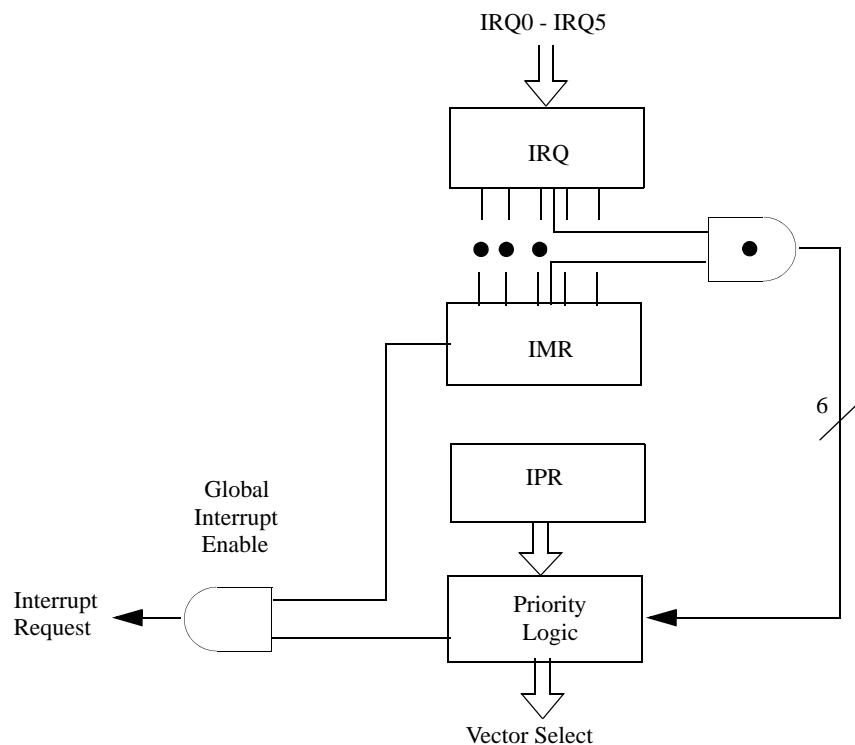


**Figure 17.  Interrupt Block Diagram**

# Clock

The Z8® on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to an external crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, up to 8 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitor values from each pin directly to device ground pin 14 on DIP and SOIC packages or pins 5 and 6 on SSOP package (Figure 18).

> **Note:** The crystal capacitor loads should be connected directly to the Z8® GND pin to reduce Ground noise injection. They should not connect to system Ground.



Ceramic Resonator or Crystal · LC Clock · External Clock · RC Clock
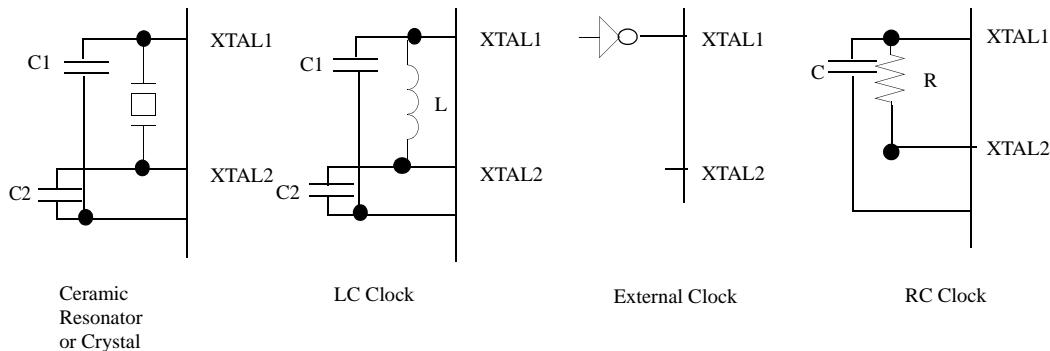
**Figure 18.  Oscillator Configuration**

**Table 16. Typical Frequency (MHz) vs. RC Values $V_{CC}$ = 5.0 V @ 25°C**

| | Load Capacitor | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 33 pF | | 56 pF | | 100 pF | | 0.001 µF | |
| Resistor (R) | A | B | A | B | A | B | A | B |
| 1.0 MΩ | 0.05 | 0.03 | 0.03 | 0.02 | 0.02 | 0.01 | 0.001 | 0.001 |
| 560 KΩ | 0.09 | 0.04 | 0.05 | 0.025 | 0.03 | 0.02 | 0.003 | 0.002 |
| 220 KΩ | 0.23 | 0.11 | 0.12 | 0.07 | 0.07 | 0.043 | 0.007 | 0.005 |
| 100 KΩ | 0.5 | 0.19 | 0.28 | 0.13 | 0.15 | 0.086 | 0.014 | 0.01 |
| 56 KΩ | 0.93 | 0.28 | 0.48 | 0.2 | 0.27 | 0.13 | 0.026 | 0.02 |
| 20 KΩ | 2.2 | 0.57 | 1.1 | 0.41 | 0.71 | 0.28 | 0.07 | 0.05 |
| 10 KΩ | 3.5 | 1.0 | 2.1 | 0.64 | 1.4 | 0.45 | 0.14 | 0.08 |

**Table 16. Typical Frequency (MHz) vs. RC Values V$_{CC}$ = 5.0 V @ 25°C  (Continued)**

| Resistor (R) | Load Capacitor | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 33 pF | | 56 pF | | 100 pF | | 0.001 µF | |
| | **A** | **B** | **A** | **B** | **A** | **B** | **A** | **B** |
| 5 KΩ | 7.6 | 1.6 | 3.6 | 1.0 | 2.3 | 0.7 | 0.28 | 0.14 |
| 2 KΩ | 12.5 | 2.3 | 8.5 | 1.7 | 4.1 | 1.3 | 0.66 | 0.27 |
| 1 KΩ | 17 | 3.1 | 13 | 2.5 | 9.5 | 1.8 | 1.2 | 0.42 |

1. A = Standard mode frequency
2. B = Low EMI mode frequency

## HALT Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

➤ **Note:**  On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

➤ **Note:**  The device can be recovered by a WDT timeout. The WDT reset in HALT Mode generates a full reset similar to the Normal run mode (not STOP Mode).

## STOP Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 A. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A LOW INPUT condition on P27 releases the STOP mode. Program execution begins at location 000C (Hex). Refer to the Watch Dog Timer (WDT) section for information relating to WDT wakeup out of Stop Mode. However, when P27 is used to release STOP mode, the I/O port mode registers are not reconfigured to their default POWER-ON conditions. Thus the I/O, configured as output when the STOP instruction was executed, is prevented from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD       P2M, #1XXX XXXXB
NOP
STOP
```
Note:  X = Dependent on user's application.

> **Note:** Any Low level detected on pin P27 takes the device out of STOP mode, even if it is configured as an output. It is not edge triggered.

To enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

| | | |
|---|---|---|
| FFh | NOP | ; clear the pipeline |
| 6Fh | STOP | ; enter STOP mode |
| | or | |
| FFH | NOP | ; clear the pipeline |
| 7Fh | HALT | ; enter HALT mode |

> **Note:** On the CCP emulator, a software workaround must be used to enable P27 as the Stop-Mode Recovery source. This workaround follows.

## Software Work Around on the Z86CCP01ZEM Emulator
## to Enable P27 as Stop-Mode Recovery Source

| | | |
|---|---|---|
| SWFIXP27: | PUSH RP | |
| | LD RP, #0Fh | |
| | LD R012, #001101X0B | X= 1 for LOW EMI Mode |
| | | X= 0 for STANDARD Mode |
| | POP RP | |

## Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 $T_{WDT}$ period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

**Op Code WDT (5Fh)**

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every $T_{WDT}$; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of $T_{PQR}$, plus 18 crystal clock cycles. The software enabled WDT does not run in STOP mode.

On the CCP emulator, a software workaround must be used to emulate the software WDT. This workaround follows.

```
SWFIXSWDT:     PUSH RP

               LD RP, #0Fh

               LD R15,#00000101B

               POP RP
```

**Op Code WDH (4Fh)**

When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters – it just makes it possible to operate the WDT during HALT mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

▶ **Note:** On the CCP emulator, a software workaround must be used to enable the software in HALT Mode/STOP Mode or hardware-enabled WDT. This workaround follows.

# Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Software WDT Running in HALT Mode

```
SWFIXSWDT:     PUSH RP

               LD RP, #0Fh

               LD R15,#00000101B

               POP RP
```

**Permanent WDT**

Selecting the hardware-enabled Permanent WDT option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in HALT mode and STOP mode, and it cannot be disabled.

## Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Hardware Enabled Permanent WDT in HALT Mode and Stop Mode

The following functions must be performed

1. The first instruction after reset at address 000Ch must be the WDT instruction or op code 5F. The following routine must be added in the initialization of the

```
HSWFIXHWDT:    PUSH RP
               LD RP, #0Fh
               LD R15,#00000101B
               POP RP
```

## Auto Reset Voltage ($V_{LV}$)

The Z8$^{®}$ features an auto-reset built-in. The auto-reset circuit resets the Z8$^{®}$ when it detects the $V_{CC}$ below $V_{LV}$. Figure 19 shows the Auto Reset Voltage versus temperature. If the $V_{CC}$ drops below the $V_{CC}$ operating voltage range, the Z8$^{®}$ functions down to the $V_{LV}$ unless the internal clock frequency is higher than the specified maximum $V_{LV}$ frequency.
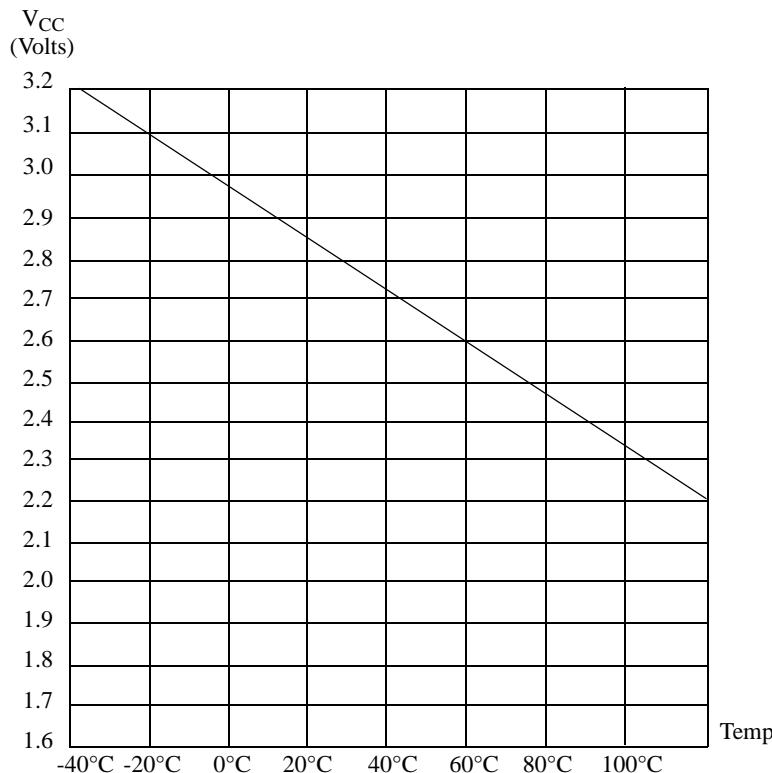
**Figure 19.  Typical Auto Reset Voltage (V$_{LV}$) vs. Temperature**

## OTP Option Bit Description

One-Time Programmable EPROM option bits for the device are described in this section. The
Z86E02 SL1925 must be power-cycled to fully implement the selected option after
programming.

**Low-EMI Emission.** The Low EMI option bit, when programmed, enables the Z8 to operate in a
low-EMI emission (low-noise) mode. Use of this feature results in:

- All pre-driver slew rates are typically reduced to 10 ns

- Internal SCLK /TCLK operation limited to a maximum of 4 MHz–250 ns cycle time

- Output drivers typically exhibit resistances of 200 ohms

- Oscillator divide-by-two circuitry eliminated

**RC Oscillator.** The RC Oscillator option bit, when programmed, enables the inter-
nal RC oscillator to connect to the XTAL2 and XTAL1 pins while disabling the
internal crystal oscillator to XTAL2 and XTAL1.

**EPROM Protect.** EPROM Protect fully protects the Z8 program code from being read externally. When EPROM Protect is selected, the instructions LDC and LDCI are supported (Z86E02 SL1925 does not support the instructions LDE and LDEI). When the device is programmed for ROM Protect, the Low-Noise feature is not automatically enabled.

**Auto Latch Disable.** Auto Latch Disable option bit, when programmed, globally disables all Auto Latches.

**Permanent WDT Enable**. The hardware-enabled permanent WDT Enable option bit, when programmed, enables the WDT permanently after exiting reset. Unlike software-enabled WDT, the hardware-enabled permanent WDT cannot be stopped even in HALT or STOP modes.

**32-KHz Enable.** The 32-KHz Enable option bit enables the 32-KHz oscillator circuit and disables the high-frequency crystal oscillator circuit. This option bit is disabled if the RC oscillator option bit is programmed.

**Application Precaution**

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above $V_{CC}$ occur on the XTAL1 pin ($\overline{CE}$). In addition, processor operation of Z8[®] OTP devices may be affected by excessive noise surges on the P33 ($V_{PP}$), XTAL1 ($\overline{CE}$), P32 (EPM), P31 ($\overline{OE}$) pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to $V_{CC}$.
- Adding a capacitor to the affected pin.

▶ **Note:** Programming the EPROM/Test Mode Disable option prevents accidental entry into EPROM Mode or Test Mode.

## Control Registers

**Table 17. Timer Mode Register, R241 TMR F1h Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note:  R = Read, W = Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|-----|-----|-----|-----|-----|
| 7-6 | Reserved | R/W | 00 | Reserved-must be 0 |
| 5-4 | $T_{IN}$ Mode | R/W | 0 | **$T_{IN}$ Mode**<br>00: External Clock Input<br>01: Gate Input<br>10: Trigger Input (non retriggerable)<br>11: Trigger Input (retriggerable) |
| 3 | T1 Count | R/W | 0 | **TI Count**<br>0: Disable<br>1: Enable |
| 2 | T1 | R/W | 0 | **TI**<br>0: No Function<br>1: Load T1 |
| 1-0 | Reserved | R/W | 0 | Reserved - must be 0 |

**Table 18. Counter/Timer 1 Register, R242 T1 F2h Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | X | X | X | X | X | X | X | X |

Note:  R = Read, W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|-----|-----|-----|-----|-----|
| 7-0 | T1 | R | X | **T1 Current Value** |
|  |  | W | X | **T1 Initial Value**<br>Range = 1-256 decimal; 01h-00h |

**Table 19. Prescaler 1 Register, R243 PRE1 F3h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | X | X | X | X | X | X | X | X |

Note:  R = Read, W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|--------------|-----------|-----|-------------|-------------|
| 7-2 | Prescaler | W | X | **Prescaler Modulo**<br>Range = 1-64 decimal; 01h-00h |
| 1 | Clock | W | 0 | **Clock Source**<br>0: T1 External Timing Input ($T_{IN}$) Mode<br>1: Internal |
| 0 | Count | W | 0 | **TI Count Mode**<br>0: Single Pass<br>1: Modulo N |

**Table 20. Port 2 Mode Register, R246 P2M F6h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | W | W | W | W | W | W | W | W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note:  W = Write,

| Bit Position | Bit Field | R/W | Reset Value | Description |
|--------------|-----------|-----|-------------|-------------|
| 7-0 | P20-P27 | W | 1 | **P20-P27 I/O Definition**<br>0: Defines bit as Output<br>1: Defines bit as Input |

**Table 21. Port 3 Mode Register, R247 P3M F7h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| R/W | W | W | W | W | W | W | W | W |
| Reset | X | X | X | X | X | X | X | X |

Note:  W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|--------------|-----------|-----|-------------|-------------|
| 7-2 | Reserved | W | X | Reserved-must be 0 |
| 1 | Port 3 | W | 0 | **Port 3 Outputs** <br> 0: DIGITAL Mode <br> 1: ANALOG Mode |
| 0 | Port 2 | W | 0 | **Port 2 Outputs** <br> 0: Open-Drain <br> 1: Push-Pull |

**Table 22. Port 0 and 1 Mode Register, R248 P01 F8h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| R/W | W | W | W | W | W | W | W | W |
| Reset | X | X | X | 0 | X | 1 | 0 | 1 |

Note:  W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|--------------|-----------|-----|-------------|-------------|
| 7-5, 3 | Reserved | W | X | Reserved-must be 0 |
| 4 | Reserved | W | 0 | Reserved-must be 0 |
| 2 | Reserved | W | X | Reserved-must be 1 |
| 1-0 | P02-P00 | W | 01 | **P02-P00 Mode** <br> 0: Output <br> 1: Input |

**Table 23. Interrupt Priority Register, R249 IPR F9h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| R/W | W | W | W | W | W | W | W | W |
| Reset | X | X | X | X | X | X | X | X |

Note: W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|--------------|-----------|-----|-------------|-------------|
| 7-6 | Reserved | W | X | Reserved-must be 0 |
| 5 | IRQ3, IRQ5 | W | X | **IRQ3, IRQ5 Priority (Group A)**<br>0: IRQ5 > IRQ3<br>1: IRQ3 < IRQ5 |
| 4, 3, 0 | Interrupt | W | X | **Interrupt Group Priority**<br>000: Reserved*<br>001: C>A>B<br>010: A>B>C<br>011: A>C>B<br>100: B>C>A<br>101: C>B>A<br>110: B>A>C<br>111: Reserved |
| 2 | IRQ0, IRQ2 | W | X | **IRQ0, IRQ2 Priority (Group B)**<br>0: IRQ2 > IRQ0<br>1: IRQ0 < IRQ2 |
| 1 | IRQ1, IRQ4 | W | X | **IRQ1, IRQ4 Priority (Group C)**<br>0: IRQ1 > IRQ4<br>1: IRQ4 < IRQ1 |

Note: *Selecting a Reserved mode causes an undefined operation.

**Table 24. Interrupt Request Register, R250 IPR FAh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note:  R = Read, W = Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-6 | Reserved | R/W | 00 | Reserved-must be 0 |
| 5 | IRQ5 | R/W | 0 | **Interrupt**<br>IRQ5 = T1<br>0: No interrupt pending<br>1: Interrupt pending |
| 4 | IRQ4 | R/W | **0** | **Interrupt**<br>RQ4 = Software generated<br>0: No interrupt pending<br>1: Interrupt pending |
| 3 | IRQ3 | R/W | **0** | **Interrupt**<br>RQ3 = P32 Input (rising edge)<br>0: No interrupt pending<br>1: Interrupt pending |
| 2 | IRQ2 | R/W | **0** | **Interrupt**<br>RQ2 = P31 Input<br>0: No interrupt pending<br>1: Interrupt pending |
| 1 | IRQ1, | R/W | **0** | **Interrupt**<br>RQ1 = P33 Input<br>0: No interrupt pending<br>1: Interrupt pending |
| 0 | IRQ0 | R/W | **0** | **Interrupt**<br>RQ0 = P32 Input<br>0: No interrupt pending<br>1: Interrupt pending |

Note:  *Selecting a Reserved mode causes an undefined operation.

**Table 25. Interrupt Mask Register, R251 IMR FBh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: R = Read, W = Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7 | Master Interrupt Enable | R/W | 0 | 0: Disables global interrupts*<br>1: Enables global interrupts* |
| 6 | Reserved | R/W | X | Reserved-must be 0 |
| 5-0 | IRQ0-IRQ5 | R/W | X | 1: Enables IRQ0-IRQ5 (D0 = IRQ0) |

Note: *Must use Ei/Di instruction to set/reset this bit.

**Table 26. Flag Register, R252 FCh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | X | X | X | X | X | X | X |

Note: R = Read, X= Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7 | Carry | R/W | X | Carry Flag |
| 6 | Zero | R/W | X | Zero Flag |
| 5 | Sign | R/W | X | Sign Flag |
| 4 | Overflow | R/W | X | Overflow Flag |
| 3 | Decimal Adjust | R/W | X | Decimal Adjust Flag |
| 2 | Half Carry | R/W | X | Half Carry Flag |
| 1 | User | R/W | X | User Flag F2* |
| 0 | User | R/W | X | User Flag F1* |

Note: *Not affected by RESET.

**Table 27. Register Pointer, R253 RP FDh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: R = Read, W= Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-4 | Working Register Pointer | R/W | 0 | Working Register Pointer |
| 3-0 | Reserved | R/W | X | Reserved-must be 0 |

**Table 28. General-Purpose Register, R254 GPR FEh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: R = Read, W= Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-0 | Stack | R/W | 0 | General-Purpose Register |

**Table 29. Stack Pointer Low, R255 SPL FFh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: R = Read, W= Write

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-0 | Stack | R/W | 0 | Stack Pointer Lower Byte (SP0-SP7) |

# Package Information
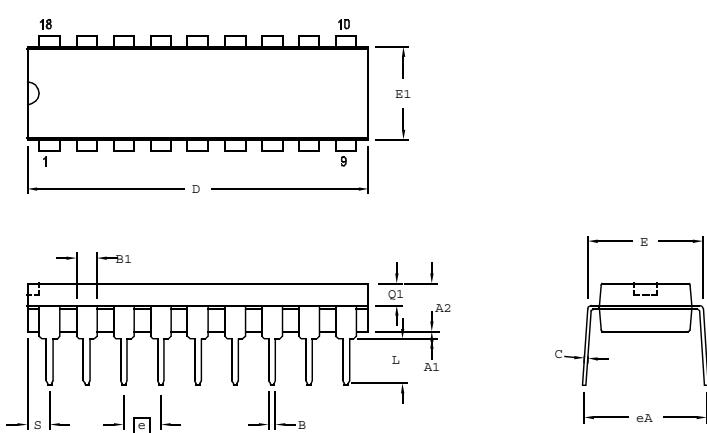


| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | .020 | .032 |
| A2 | 3.25 | 3.43 | .128 | .135 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.14 | 1.65 | .045 | .065 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 22.35 | 23.37 | .880 | .920 |
| E | 7.62 | 8.13 | .300 | .320 |
| E1 | 6.22 | 6.48 | .245 | .255 |
| e | 2.54 BSC | | .100 BSC | |
| eA | 7.87 | 9.40 | .310 | 0.370 |
| L | 3.18 | 3.81 | .125 | .150 |
| Q1 | 1.47 | 1.65 | .058 | .065 |
| S | 0.89 | 1.65 | .035 | .065 |

CONTROLLING DIMENSIONS : INCH

**Figure 20.  18-Pin DIP Package Diagram**
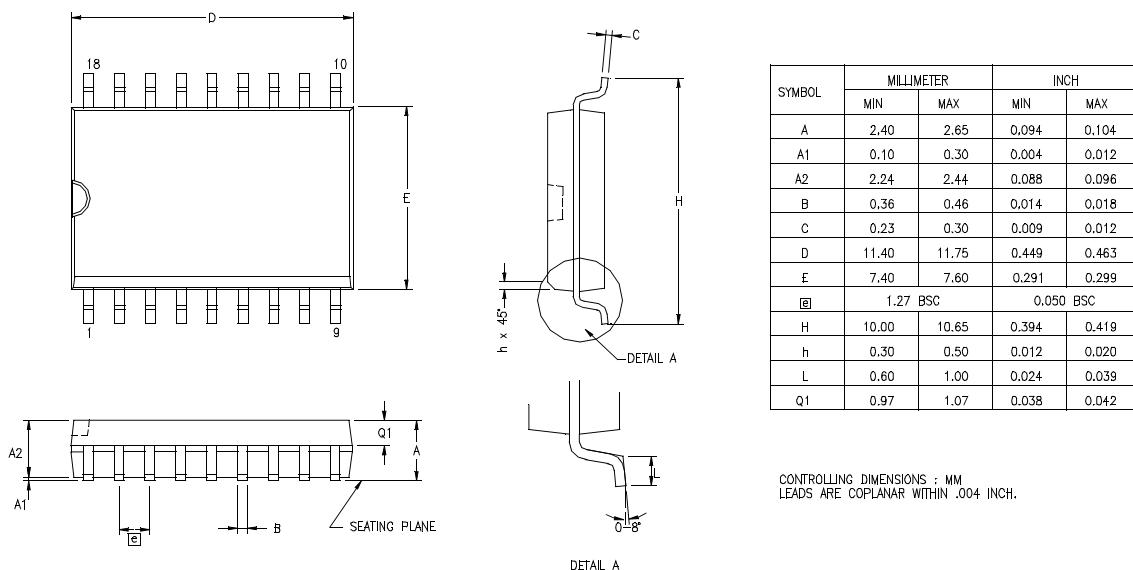


| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | 0.094 | 0.104 |
| A1 | 0.10 | 0.30 | 0.004 | 0.012 |
| A2 | 2.24 | 2.44 | 0.088 | 0.096 |
| B | 0.36 | 0.46 | 0.014 | 0.018 |
| C | 0.23 | 0.30 | 0.009 | 0.012 |
| D | 11.40 | 11.75 | 0.449 | 0.463 |
| E | 7.40 | 7.60 | 0.291 | 0.299 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 10.00 | 10.65 | 0.394 | 0.419 |
| h | 0.30 | 0.50 | 0.012 | 0.020 |
| L | 0.60 | 1.00 | 0.024 | 0.039 |
| Q1 | 0.97 | 1.07 | 0.038 | 0.042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 21.  18-Pin SOIC Package Diagram**
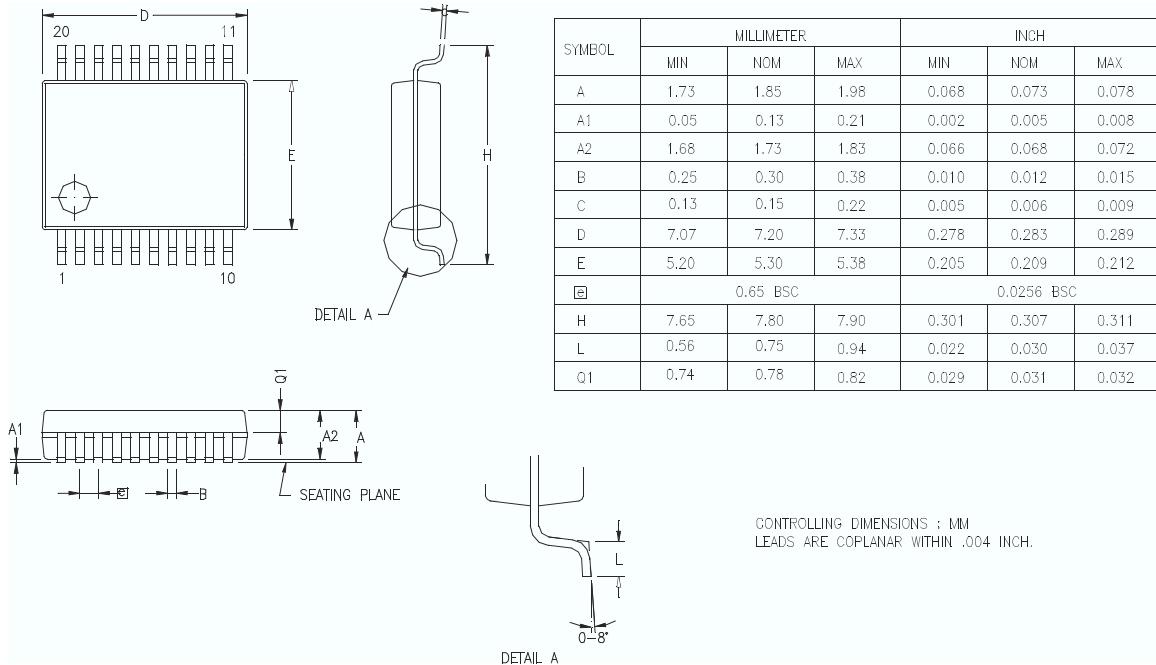
**Figure 22. 20-Pin SSOP Package Diagram**

# Ordering Information

**Table 30. Ordering Information**

| Pin Count | Package | Size (KB) | Description |
|-----------|---------|-----------|-------------|
| 18 | DIP | 0.5 | Z86E0208PSC1925 |
| | | | Z86E0208PEC1925 |
| | SOIC | 0.5 | Z86E0208SSC1925 |
| | | | Z86E0208SEC1925 |
| 20 | SSOP | 0.5 | Z86E0208HSC1925 |
| | | | Z86E0208HEC1925 |

Note: The Standard temperature range is 0°C to 70°C. For parts that operate in the Extended temperature range of -40°C to 105°C, substitute the letter E for the letter S. For example, the PSI number for an 18-pin DIP operating at 8 MHz in the extended temperature range is Z86E0208PEC

For fast results, contact your local ZiLOG Sales offices for assistance in ordering the part(s) required. Contact your local ZiLOG Sales office by navigating to Sales Office on

# Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86E0208PSC1925 is a 8-MHz 18-pin DIP that operates in the -0°C to +70°C temperature range, with Plastic Standard Flow. The Z86E0208PSC1925 part number corresponds to the code segments indicated in the following table.

| | |
|------|---------------------------|
| Z | ZiLOG Prefix |
| 86 | Z8 Product |
| E | OTP Product |
| 02 | Product Number |
| 08 | Speed (MHz) |
| P | Dual In-line Processor |
| S | Standard Temperature |
| C | Environmental Flow |

# Document Information

## Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

| | |
|------|----------------------------|
| PS | Product Specification |
| 0148 | Unique Document Number |
| 02 | Revision Number |
| 0903 | Month and Year Published |

# Customer Feedback Form

## Z86E02 SL1925 Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see Return Information, below). We also welcome your suggestions!

## Customer Information

| | |
|---|---|
| Name | Country |
| Company | Phone |
| Address | Fax |
| City/State/Zip | E-Mail |

## Product Information

| |
|---|
| Serial # or Board Fab #/Rev. # |
| Software Version |
| Document Number |
| Host Computer Description/Type |

## Return Information

ZiLOG
532 Race Street
Campbell, CA 95126-3432
Fax: (408) 558-8536
www.zilog.com

## Problem Description or Suggestion

Please provide a complete description of the problem or suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

# Mouser Electronics

Authorized Distributor


Click to View Pricing, Inventory, Delivery & Lifecycle Information:


[ZiLOG](#):
  [Z86E0208SSC1925](#)  [Z86E0208HSC1925](#)  [Z86E0208HEC1925](#)  [Z86E0208HSG1925](#)  [Z86E0208HEG1925](#)
[Z86E0208SEG1925](#)  [Z86E0208PEG1925](#)  [Z86E0208SSG1925](#)  [Z86E0208PSG1925](#)