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PCI Express x1, x4 Root Complex Lite IP Core

PCI Express is a high performance, fully scalable, well defined standard for a wide variety of computing and communications platforms. It has been defined to provide software compatibility with existing PCI drivers and operating systems. Being a packet based serial technology, PCI Express greatly reduces the number of required pins and simplifies board routing and manufacturing. PCI Express is a point-to-point technology, as opposed to the multidrop bus in PCI. Each PCI Express device has the advantage of full duplex communication with its neighbor to greatly increase overall system bandwidth. The basic data rate for a single lane is double that of the 32 bit/33 MHz PCI bus. A four lane link has eight times the data rate in each direction of a conventional bus.



Lattice's **PCI Express Root Complex (RC) Lite core** provides an x1 or x4 root complex solution from the electrical SERDES interface, physical layer, data link layer and a minimum transaction layer in PCI express protocol stack. This IP is a lighter version of the root complex intended to use in simple bridging application to local bus. This solution supports the high value, low power [LatticeECP3](#) and [LatticeECP2M](#) FPGA device families.

Key Features

Top Level IP Support

125 MHz user interface

x4 supports a 64-bit data path

x1 supports a 16-bit data path

In transmit, user creates TLPs without ECRC, LCRC, or sequence number

In receive, user receives valid TLPs without ECRC, LCRC, or sequence number

Credit interface for transmit and receive for PH, PD, NPH, NPD, CPLH, CPLD credit types

Higher layer control of LTSSM via ports

Transaction Layer

Transmit and Receive Flow control

Malformed and poisoned TLP detection

Optional ECRC generation/checking

INTx message TLP decoding and interrupt signaling to user

Error message TLP decoding and signaling to user.

128, 256, 512, 1k, 2k or 4k bytes maximum payload size

Data Link Layer

Data link control and management state machine

Flow control initialization

Ack/Nak DLLP generation/termination

LCRC generation/checking

Sequence number appending/checking/removing

Retry buffer and management

Receiver buffer

PHY Layer Features

2.5 Gbps CML electrical interface

PCI Express 1.1 electrical compliance

Many options for signal integrity including differential output voltage, transmit pre-emphasis and receiver equalization

Serialization and de-serialization

8b10b symbol encoding/decoding

Link state machine for symbol alignment

Clock tolerance compensation supports +/- 300 ppm

Framing and application of symbols to lanes

Data scrambling and de-scrambling

Lane-to-lane de-skew

Link Training and Status State Machine (LTSSM)

Electrical idle generation

Receiver detection

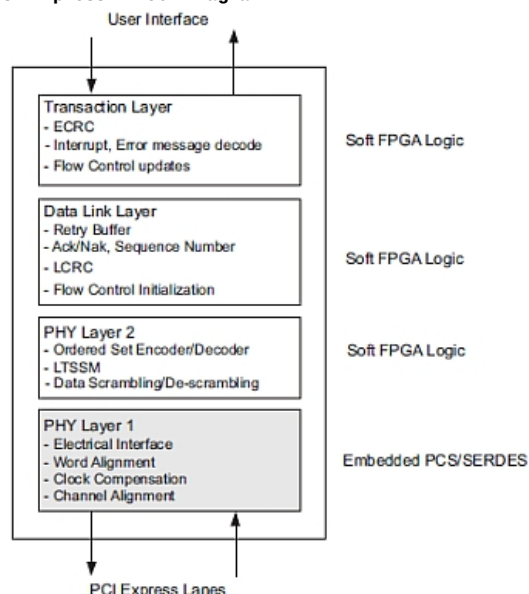
TS1/TS2 generation/detection

Lane polarity inversion

Link width negotiation

Higher layer control to jump to defined states

PCI Express - Block Diagram



Performance and Resource Utilization

PCI Express x1 Root Complex

LatticeECP3¹

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f _{MAX} (MHz)
Config 1 - x1, 128 Bytes, ECRC disabled	3059	4560	3048	3	125

1. Performance and utilization data are generated targeting an LFE3-95E-7FN1156CES using Lattice Diamond 1.0 and Synplify Pro D- 2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M¹

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f _{MAX} (MHz)
Config 1 - x1, 128 Bytes, ECRC disabled	3260	4770	3096	3	125

1. Performance and utilization data are generated targeting an LFE2M-50E-6F900C using Lattice Diamond 1.0 and Synplify Pro D- 2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

PCI Express x4 Root Complex

LatticeECP3¹

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f _{MAX} (MHz)
Config 1 - x4, 128 Bytes, ECRC disabled	7703	10608	8460	9	125

1. Performance and utilization data are generated targeting an LFE3-95E-7FN1156CES using Lattice Diamond 1.0 and Synplify Pro D- 2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M¹

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f _{MAX} (MHz)
Config 1 - x4, 128 Bytes, ECRC disabled	8185	10889	8469	9	125

1. Performance and utilization data are generated targeting an LFE2M-50E-6F900C using Lattice Diamond 1.0 and Synplify Pro D- 2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

Solutions

Download demo bitstream from the [PCI Express Demo](#) page.

Visit the [PCI Express Solutions](#) page for other demos, boards and development kits.

Ordering Information

Family	x1 Part Numbers	x4 Part Numbers
LatticeECP3	PCI-ERC1-E3-U1	PCI-ERC4-E3-U1
LatticeECP2M	PCI-ERC1-PM-U1	PCI-ERC4-PM-U1

IP Version: 1.1

Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the [IP Express Quick Start Guide](#).

Purchase: To find out how to purchase the IP Core, please contact your [local Lattice Sales Office](#).