MAX15009/MAX15011

300mA LDO Regulators with Switched Output and Overvoltage Protector

General Description

The MAX15009 includes a 300mA LDO regulator, a switched output, and an overvoltage protection (OVP) controller to protect downstream circuits from high-|voltage load dump. The MAX15011 includes only the 300mA LDO regulator and switched output. Both devices operate over a wide supply voltage range from 5V to 40V and are able to withstand load-dump transients up to 45V. The MAX15009/MAX15011 feature short-circuit and thermal-shutdown protection.

The 300mA LDO regulator consumes 67µA quiescent current at light loads and is well suited to power battery applications. The LDO features independent enable and hold inputs, as well as a microprocessor (µP) reset output with adjustable reset timeout period.

The switched output of the MAX15009/MAX15011 incorporates a low $R_{DS(ON)}$ (0.28Ω, typ) pass transistor switch internally connected to the output of the LDO regulator. This switch features accurate current-limit sensing circuitry and is capable of controlling remote loads. The MAX15009/MAX15011 feature an adjustable current limit and a programmable delay timer to set the overcurrent detection blanking time of the switch and autoretry timeout.

The MAX15009 OVP controller operates with an external enhancement mode n-channel MOSFET. While the monitored voltage remains below the adjustable threshold, the MOSFET stays on. When the monitored voltage exceeds the OVP threshold, the OVP controller quickly turns off the external MOSFET. The OVP controller is configurable as a load-disconnect switch or a voltage limiter.

The MAX15009/MAX15011 are available in a thermally enhanced, 32-pin (5mm x 5mm), TQFN package and are fully specified over the -40°C to +125°C automotive operating temperature range.

Applications

- Multimedia Power Supply

Typical Operating Circuits and Selector Guide appear at end of data sheet.

Features

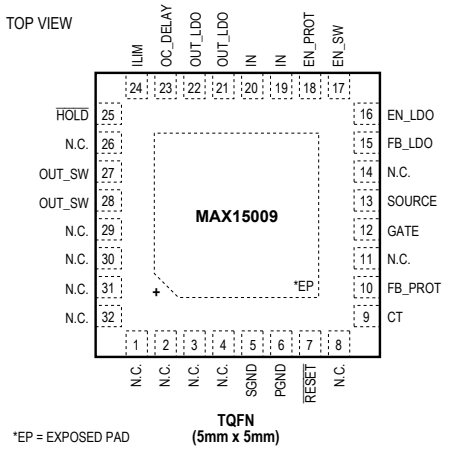
- 300mA LDO Regulator, Switched Output, and OVP Controller (MAX15009)
- 300mA LDO Regulator and Switched Output (MAX15011)
- 5V to 40V Wide Operating Supply Voltage Range
- 45V Load Dump Protection
- 67µA Quiescent Current LDO Regulator
- OVP Controller Disconnects or Limits Output Voltage During Battery Overvoltage Conditions
- LDO Regulator with Enable, Hold, and Reset Features
- Internal 0.28Ω (typ) n-Channel Switch for Switched Output
- 100mA Switched Output with Adjustable Current-Limit Blanking/Autoretry Delay

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX15009ATJ+	-40°C to +125°C	32 TQFN-EP*	T3255-4
MAX15011ATJ+	-40°C to +125°C	32 TQFN-EP*	T3255-4

+Denotes a lead(Pb)-free/RoHS-compliant package.
For tape and reel, add a T after "+."
**EP = Exposed pad.*

Pin Configurations



Pin Configurations continued at end of data sheet.

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Absolute Maximum Ratings

(All pins referenced to SGND, unless otherwise noted.)
IN, GATE.....-0.3V to +45V
EN_LDO, EN_SW, EN_PROT.....-0.3V to (V_{IN} + 0.3V)
SOURCE.....-0.3V to (V_{IN} + 0.3V)
OUT_LDO, FB_LDO, FB_PROT, $\overline{RESET}$, OC_DELAY.....-0.3V to +12V
GATE to SOURCE .....-0.3V to +12V
OUT_SW, ILIM, $\overline{HOLD}$.....-0.3V to (V_{OUT_LDO} + 0.3V)
OUT_SW to OUT_LDO.....-12V to +0.3V
CT to SGND.....-0.3V to +12V
SGND to PGND.....-0.3V to +0.3V
IN, OUT_LDO Current.....700mA
OUT_SW Current.....350mA
Current Sink/Source (all remaining pins) 50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C).....2.7W*
Thermal Resistance
θ_{JA}.....29.0°C/W
θ_{JC}.....1.7°C/W
Operating Temperature Range.....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
**As per JEDEC 51 Standard, Multilayer Board (PCB).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = +14V, V_{SGND} = V_{PGND} = 0V, C_{GATE} = 6000pF, C_{IN} = 10µF (ESR < 1.5Ω), C_{OUT_LDO} = 22µF (ceramic), C_{OUT_SW} = 1µF, V_{OUT_LDO} = 5V, C_T = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	$V_{IN} \geq V_{OUT}$ + 1.5V		5		40	V
Supply Current	I_{IN}	MAX15009	EN_LDO = IN, EN_SW = EN_PROT = 0V, I_{OUT_LDO} = 0µA, LDO on, switch off, protector off, measured from SGND		67	85	µA
			EN_LDO = EN_SW = IN, EN_PROT = 0V, LDO ON, I_{OUT_LDO} = 100µA, switch on, I_{OUT_SW} = 0µA, protector off, measured from SGND		290	360	
			EN_LDO = EN_SW = EN_PROT = IN, LDO ON, I_{OUT_LDO} = 100µA, switch on, I_{OUT_SW} = 0µA, protector on, measured from SGND		360	500	
		MAX15011	EN_LDO = EN_SW = IN, LDO ON, I_{OUT_LDO} = 100µA, switch on, I_{OUT_SW} = 0µA, measured from SGND		268	360	
Shutdown Supply Current	I_{SHDN}	EN_LDO = EN_SW = EN_PROT = SGND, measured from SGND	T_A = -40°C to +85°C		16	30	µA
			T_A = -40°C to +125°C			40	
IN Undervoltage Lockout	V_{UVLO}	V_{IN} falling, GATE disabled		4.10	4.27	4.45	V
IN Undervoltage Lockout Hysteresis	V_{UVLO_HYST}				260		mV

Electrical Characteristics (continued)

(V_{IN} = +14V, V_{SGND} = V_{PGND} = 0V, C_{GATE} = 6000pF, C_{IN} = 10µF (ESR < 1.5Ω), C_{OUT_LDO} = 22µF (ceramic), C_{OUT_SW} = 1µF, V_{OUT_LDO} = 5V, C_T = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Temperature	T_{SHDN}			+160		°C
Thermal Hysteresis	T_{HYST}			20		°C
LDO						
Output Voltage	V_{OUT_LDO}	I_{LOAD} = 1mA, FB_LDO = SGND	4.92	5.00	5.09	V
		I_{LOAD} = 300mA, V_{IN} = 8V, FB_LDO = SGND	4.88	5.00	5.11	
FB_LDO Set-Point Voltage	V_{FB_LDO}	With respect to SGND, I_{LOAD} = 1mA, V_{OUT_LDO} = 5V, adjustable output option	1.21	1.235	1.26	V
Dual ModeK FB_LDO Threshold	$V_{FB_LDO_TH}$	FB_LDO rising		0.125		V
		FB_LDO falling		0.064		
FB_LDO Input Current	I_{FB_LDO}	V_{FB_LDO} = 1V	-100		+100	nA
LDO Output Voltage	V_{LDO_ADJ}	Adjustable output option (Note 2)	1.8		11.0	V
LDO Dropout Voltage	V_{DO}	I_{LOAD} = 300mA (Note 3)		800	1500	mV
		I_{LOAD} = 200mA (Note 3)		520	1000	
LDO Output Current	I_{OUT_LDO}	(Note 4)	300			mA
LDO Output Current Limit	I_{LIM_LDO}	OUT_LDO = SGND, V_{IN} = 6V	330	500	700	mA
OUT_LDO Line Regulation	DV_{OUT}/ DV_{IN}	6V ≤ V_{IN} ≤ 40V, I_{LOAD} = 1mA, V_{OUT}_LDO = 5V		0.03	0.2	mV/V
		6V ≤ V_{IN} ≤ 40V, I_{LOAD} = 1mA, FB_LDO = SGND, V_{OUT_LDO} = 3.3V		0.03	0.1	
		6V ≤ V_{IN} ≤ 40V, I_{LOAD} = 20mA, FB_LDO = SGND, V_{OUT_LDO} = 5V		0.27	1	
		6V ≤ V_{IN} ≤ 40V, I_{LOAD} = 20mA, V_{OUT_LDO} = 3.3V		0.27	0.5	
OUT_LDO Load Regulation	DV_{OUT}/ DI_{OUT}	1mA to 300mA, V_{IN} = 8V, FB_LDO = SGND		0.054	0.15	mV/mA
		1mA to 300mA, V_{IN} = 6.3V, V_{OUT_LDO} = 3.3V		0.038	0.100	
OUT_LDO Power-Supply Rejection Ratio	PSRR	I_{LOAD} = 10mA, f = 100Hz, 500mV_{P-P}, V_{OUT_LDO} = 5V		60		dB
OUT_LDO Startup Delay Time	$t_{STARTUP_DELAY}$	I_{OUT_LDO} = 0mA, from EN_LDO rising to 10% of V_{OUT_LDO} (nominal), FB_LDO = SGND		30		µs

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Electrical Characteristics (continued)

(V_{IN} = +14V, V_{SGND} = V_{PGND} = 0V, C_{GATE} = 6000pF, C_{IN} = 10µF (ESR < 1.5Ω), C_{OUT_LDO} = 22µF (ceramic), C_{OUT_SW} = 1µF, V_{OUT_LDO} = 5V, C_T = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_LDO Overvoltage Protection Threshold	V_{OV_TH}	1mA sink from OUT_LDO		105	110	$\%V_{OUT_LDO}$
OUT_LDO Overvoltage Protection Sink Current	I_{OV}	V_{OUT_LDO} = V_{OUT} (nominal) x 1.15	8	19		mA
ENABLE/HOLD INPUTS						
EN_LDO to EN_PROT Input Threshold Voltage	V_{IH}		2			V
	V_{IL}				0.7	
EN_LDO, EN_PROT, EN_SW Input Pulldown Current	I_{EN_PD}	EN_ is internally pulled low to SGND		1		µA
$\overline{HOLD}$ Input Threshold Voltage	V_{IH}		1.4			V
	V_{IL}				0.4	
$\overline{HOLD}$ Input Pullup	$I_{\overline{HOLD}_PU}$	$\overline{HOLD}$ is internally pulled high to OUT_LDO		0.6		µA
$\overline{RESET}$						
RESET Voltage Threshold HIGH	$V_{\overline{RESET}_H}$	$\overline{RESET}$ goes HIGH when rising V_{OUT_LDO} crosses this threshold, FB_LDO = SGND	90.0	92.5	95.0	$\%V_{OUT_LDO}$
		$\overline{RESET}$ goes HIGH when rising V_{FB_LDO} crosses this threshold	90.0	92.5	95.0	$\%V_{FB_LDO}$
$\overline{RESET}$ Voltage Threshold LOW	$V_{\overline{RESET}_L}$	$\overline{RESET}$ goes LOW when falling V_{OUT_LDO} crosses this threshold, FB_LDO = SGND	88	90	92	$\%V_{OUT_LDO}$
		$\overline{RESET}$ goes LOW when falling V_{FB_LDO} crosses this threshold	88	90	92	$\%V_{FB_LDO}$
V_{OUT_LDO} to $\overline{RESET}$ Delay	t_{RESET_FALL}	V_{OUT_LDO} falling, 0.1V/µs		19		µs
CT Ramp Current	I_{CT}	V_{CT} = 0V	1.50	2	2.35	µA
CT Ramp Threshold	V_{CT_TH}	V_{CT} rising	1.190	1.235	1.270	V
$\overline{RESET}$ Output-Voltage Low	V_{OL}	I_{SINK} = 1mA, output asserted			0.1	V
$\overline{RESET}$ Open-Drain Leakage Current	$I_{LEAK_\overline{RESET}}$	Output not asserted			150	nA
LOAD DUMP PROTECTOR (MAX15009 only)						
FB_PROT Threshold Voltage	V_{TH_PROT}	FB_PROT rising	1.20	1.235	1.27	V
FB_PROT Threshold Hysteresis	V_{HYST}			4		$\%V_{TH_PROT}$
FB_PROT Input Current	I_{FB_PROT}	V_{FB_PROT} = 1.4V	-100		+100	nA
Startup Response Time	t_{START}	EN_PROT rising, EN_LDO = IN, to V_{GATE} = 0.5V		20		µs
GATE Rise Time	t_{GATE}	GATE rising to +8V, V_{SOURCE} = 0V		1		ms

Electrical Characteristics (continued)

(V_{IN} = +14V, V_{SGND} = V_{PGND} = 0V, C_{GATE} = 6000pF, C_{IN} = 10µF (ESR < 1.5Ω), C_{OUT_LDO} = 22µF (ceramic), C_{OUT_SW} = 1µF, V_{OUT_LDO} = 5V, C_T = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

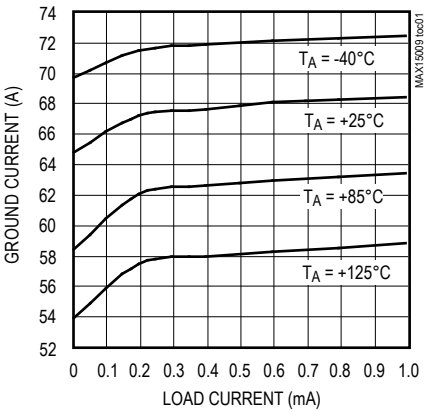
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB_PROT to GATE Turn-Off Propagation Delay	t_{OV}	FB_PROT rising from V_{TH_PROT} -250mV to V_{TH_PROT} + 250mV			0.6	µs
GATE Output High Voltage	V_{GATE} - V_{IN}	V_{SOURCE} = V_{IN} = 5.5V, R_{GATE} to IN = 1MΩ	V_{IN} + 3.2	V_{IN} + 3.5	V_{IN} + 3.8	V
		V_{SOURCE} = V_{IN}; V_{IN} ≥ 14V, RGATE to IN = 1MΩ	V_{IN} + 7.0	V_{IN} + 8.1	V_{IN} + 9.5	
GATE Output Pulldown Current	I_{GATEPD}	V_{GATE} = 5V, V_{EN_PROT} = 0V		63	100	mA
GATE Charge-Pump Current	I_{GATE}	GATE = SGND		45		µA
GATE-to-SOURCE Clamp Voltage	V_{CLMP}		12	16	18	V
SWITCH						
Switch Dropout	DV_{SW}	DV_{SW} = V_{OUT_LDO} - V_{OUT_SW}, I_{OUT_SW} = 100mA, V_{OUT_LDO} = 5V, no external MOSFET		36	70	mV
Switch Current Limit	I_{SW_LIM}	ILIM = OUT_LDO, V_{IN} = 8V	170	200	240	mA
		R_{LIM} = 100kΩ to SGND, V_{OUT_LDO} = 5V, V_{IN} = 8V	85	100	120	
		R_{LIM} = 39kΩ to SGND, V_{OUT_LDO} = 5V, V_{IN} = 8V	30	40	50	
Current-Limit Selector ILIM Voltage	V_{ILIM}	R_{LIM} = 100kΩ		0.395		V
OC_DELAY Timeout Threshold	V_{OC_DELAY}		1.194	1.235	1.270	V
OC_DELAY Timeout Pullup Current	$I_{OC_DELAY_UP}$	V_{OC_DELAY} = 0.5V rising	12.5	16.0	21.3	µA
OC_DELAY Timeout Pulldown Current	$I_{OC_DELAY_DOWN}$	V_{OC_DELAY} = 0.5V, falling	0.75	1.00	1.40	µA
Minimum OC_DELAY Timeout	$t_{OC_DELAY_MIN}$	C_{OC_DELAY} is unconnected		12		µs
EN_SW to OUT_SW Turn-On Time		OUT_SW rising to +0.5V, R_{OUT_SW} = 1kΩ		38		µs
EN_SW to OUT_SW Turn-Off Propagation Delay	t_{OV_SW}	EN_SW falling, V_{OUT_LDO} - V_{OUT_SW} rising to +1V, R_{OUT_SW} = 1kΩ, V_{OUT_LDO} = 5V		18		µs

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: 1.8V is the minimum limit for proper $\overline{HOLD}$ functionality.
Note 3: Dropout is defined as V_{IN} - V_{OUT_LDO} when V_{OUT_LDO} is 98% of the value of V_{OUT_LDO} for V_{IN} = V_{OUT_LDO} + 1.5V.
Note 4: Maximum output current may be limited by the power dissipation of the package.

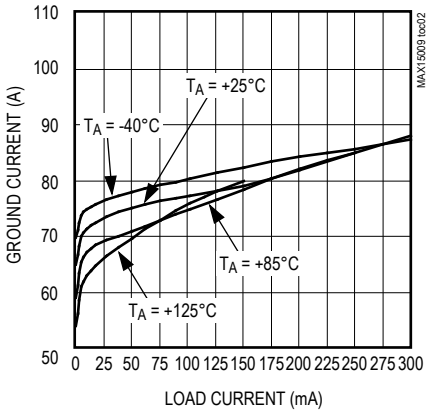
Typical Operating Characteristics

(V_{IN} = V_{EN_LDO} = V_{EN_PROT} = V_{EN_SW} = +14V, C_{IN} = 10µF, C_{OUT_LDO} = 22µF, C_{OUT_SW} = 1µF, V_{OUT_LDO} = +5V, FB_LDO = SGND, T_A = +25°C, unless otherwise specified.)

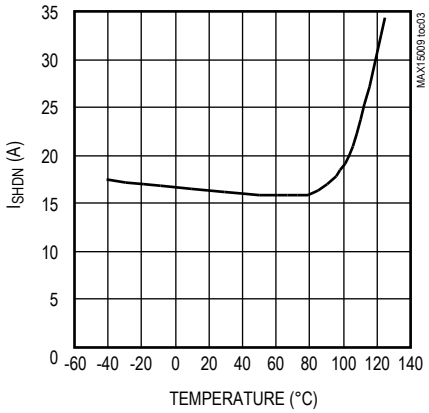
LDO GROUND CURRENT vs. LOAD CURRENT



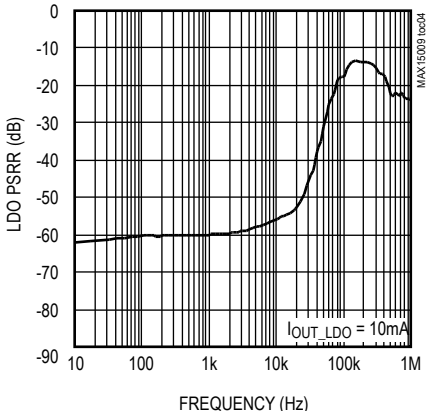
LDO GROUND CURRENT vs. LOAD CURRENT



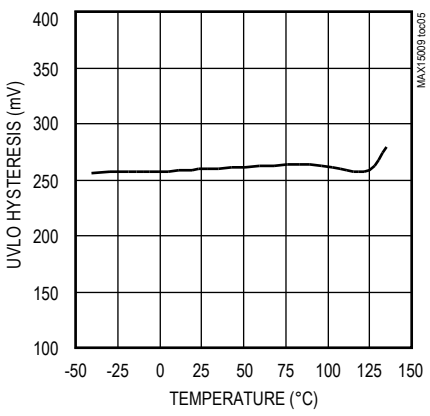
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



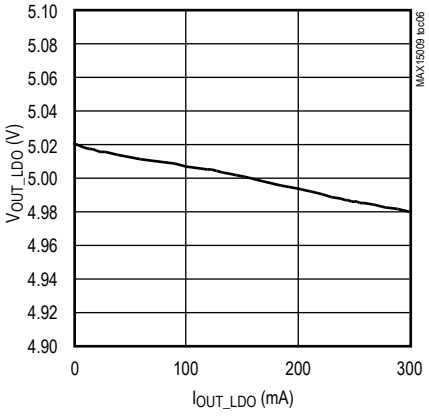
LDO POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



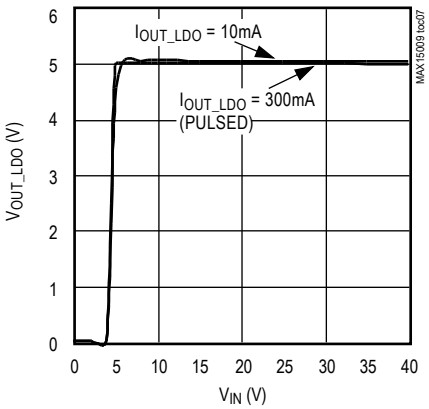
VIN UVLO HYSTERESIS vs. TEMPERATURE



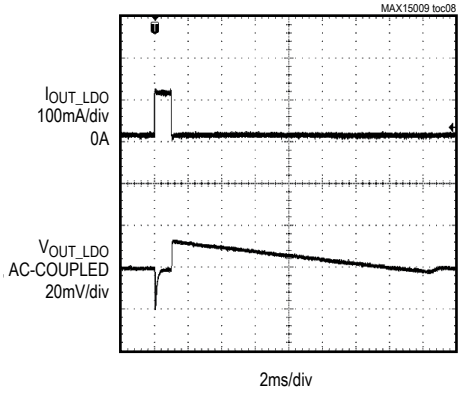
LDO LOAD REGULATION



LDO OUTPUT VOLTAGE vs. INPUT VOLTAGE



LDO LOAD-TRANSIENT RESPONSE



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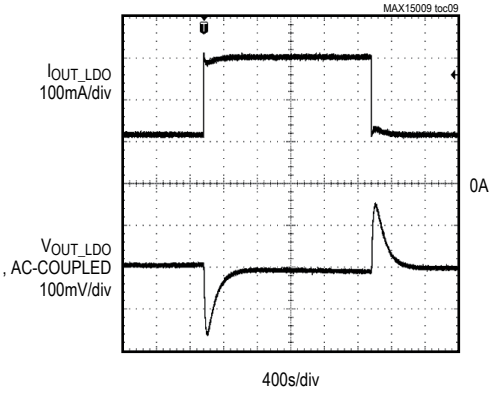
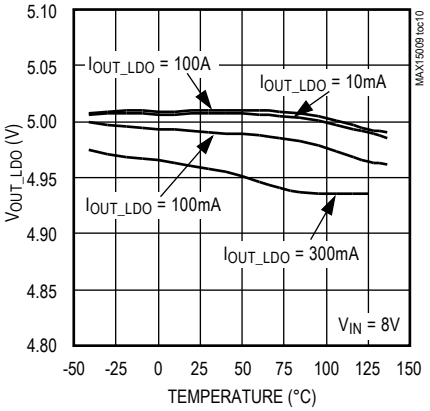


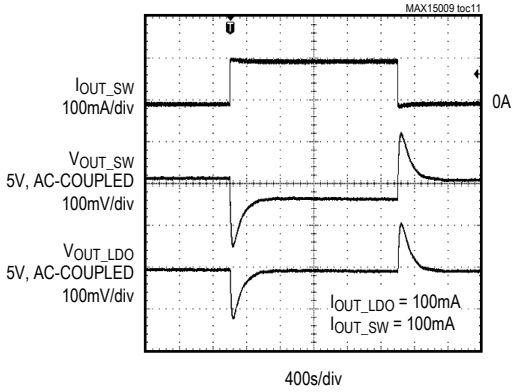
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN_LDO} = V_{EN_PROT} = V_{EN_SW} = +14V, C_{IN} = 10µF, C_{OUT_LDO} = 22µF, C_{OUT_SW} = 1µF, V_{OUT_LDO} = +5V, FB_LDO = SGND, T_A = +25°C, unless otherwise specified.)

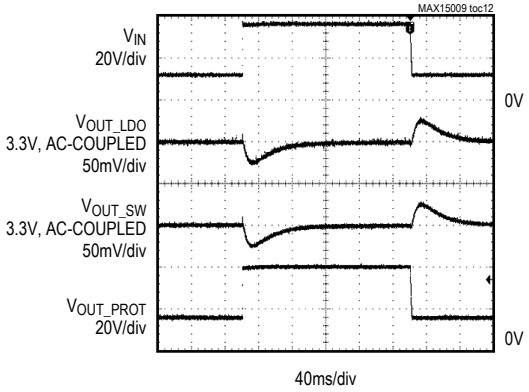
LDO OUTPUT VOLTAGE vs. TEMPERATURE



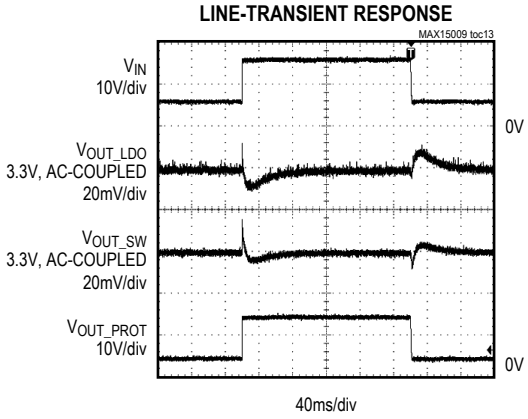
SWITCH LOAD-TRANSIENT RESPONSE



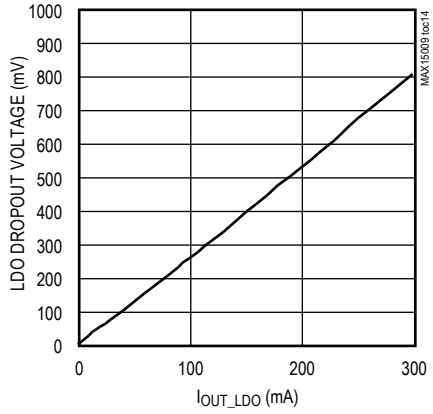
LINE-TRANSIENT RESPONSE



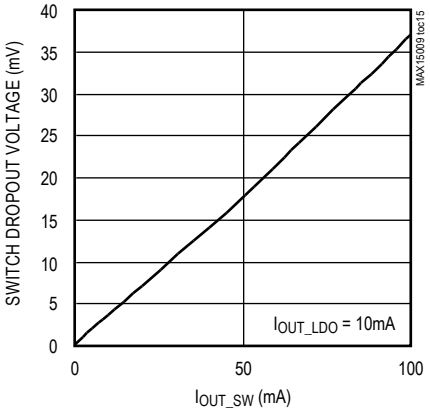
LINE-TRANSIENT RESPONSE



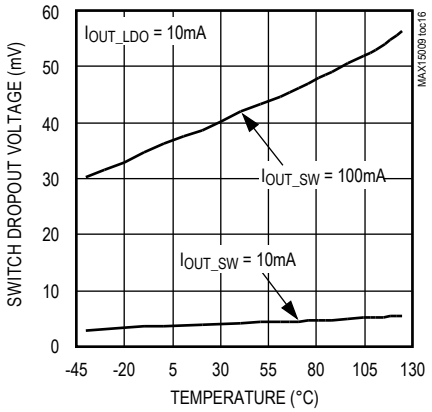
LDO DROPOUT VOLTAGE vs. LOAD CURRENT



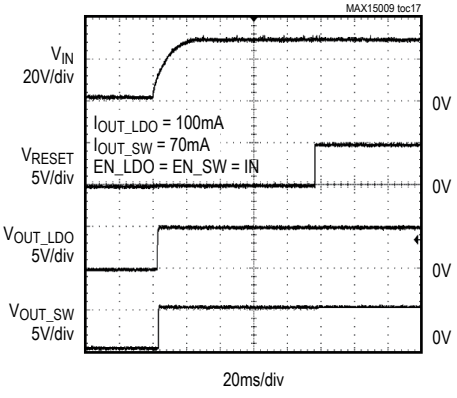
SWITCH DROPOUT VOLTAGE vs. LOAD CURRENT



SWITCH DROPOUT VOLTAGE vs. TEMPERATURE



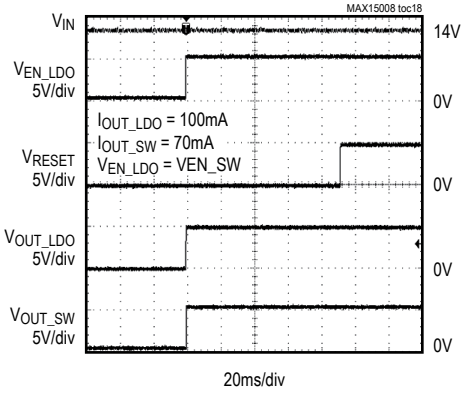
STARTUP RESPONSE THROUGH V_{IN}



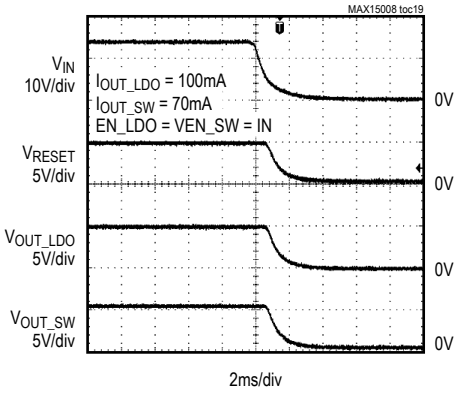
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN_LDO} = V_{EN_PROT} = V_{EN_SW} = +14V, C_{IN} = 10µF, C_{OUT_LDO} = 22µF, C_{OUT_SW} = 1µF, V_{OUT_LDO} = +5V, FB_LDO = SGND, T_A = +25°C, unless otherwise specified.)

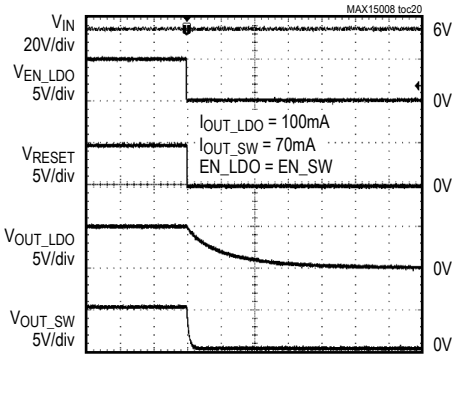
STARTUP RESPONSE THROUGH EN



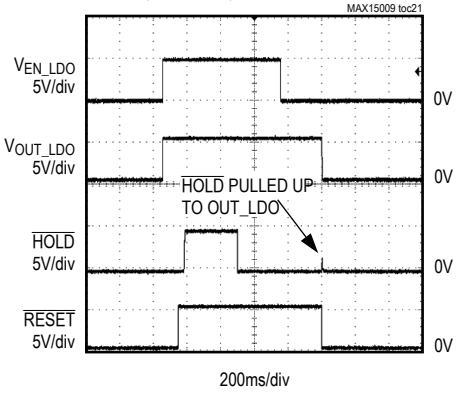
SHUTDOWN RESPONSE THROUGH V_{IN}



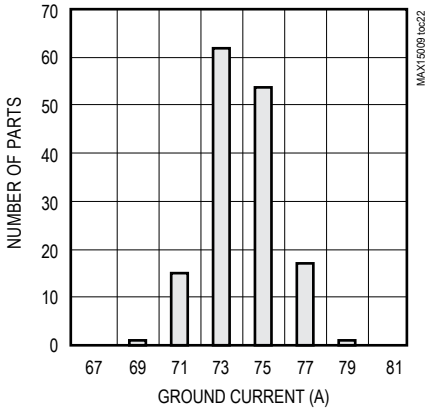
SHUTDOWN RESPONSE THROUGH EN



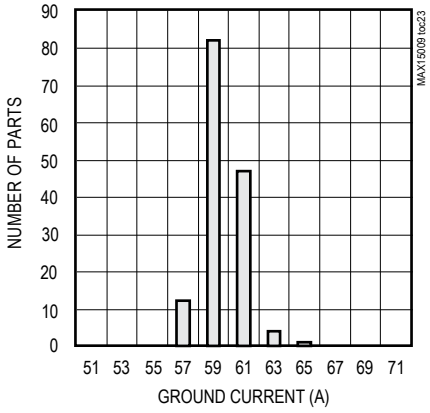
LDO, EN_LDO, AND $\overline{HOLD}$ TIMING



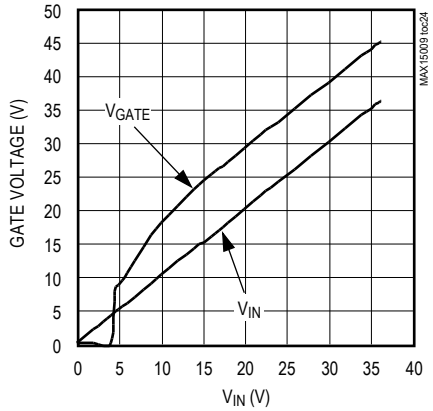
GROUND CURRENT DISTRIBUTION HISTOGRAM (T_A = -40°C)



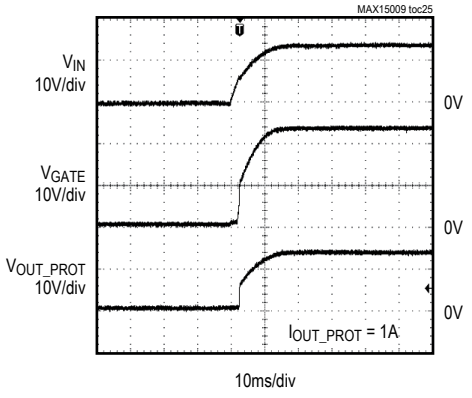
GROUND CURRENT DISTRIBUTION HISTOGRAM (T_A = +125C)



PROTECTOR GATE VOLTAGE vs. INPUT VOLTAGE (MAX15009 ONLY)



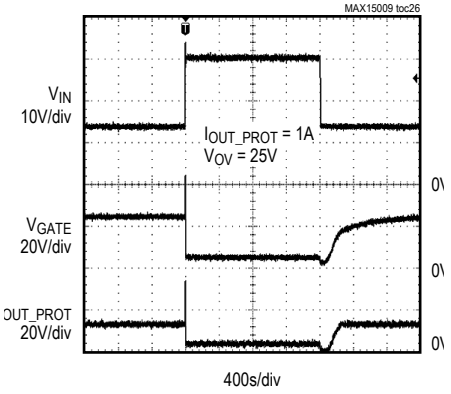
PROTECTOR STARTUP RESPONSE



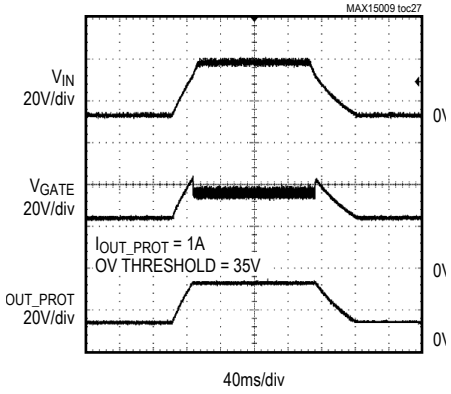
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN_LDO} = V_{EN_PROT} = V_{EN_SW} = +14V, C_{IN} = 10µF, C_{OUT_LDO} = 22µF, C_{OUT_SW} = 1µF, V_{OUT_LDO} = +5V, FB_LDO = SGND, T_A = +25°C, unless otherwise specified.)

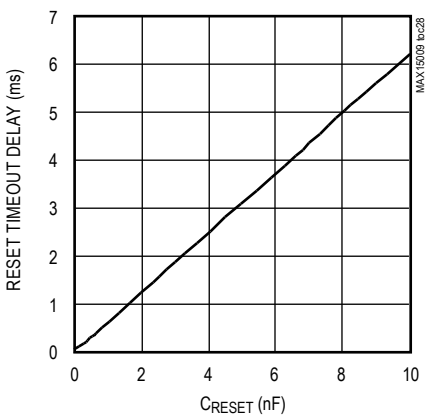
OVERVOLTAGE SWITCH FAULT



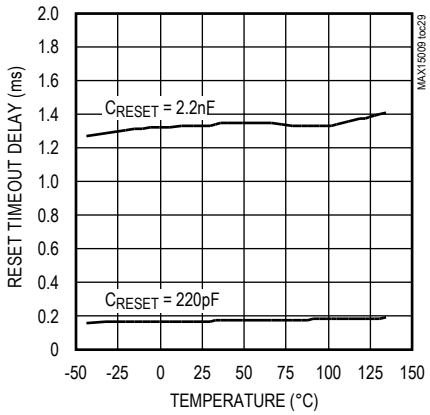
OVERVOLTAGE LIMIT FAULT



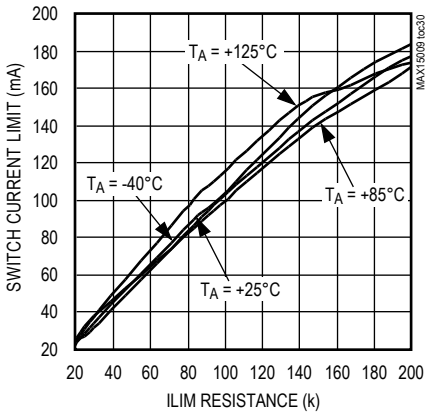
RESET TIMEOUT DELAY vs. CRESET



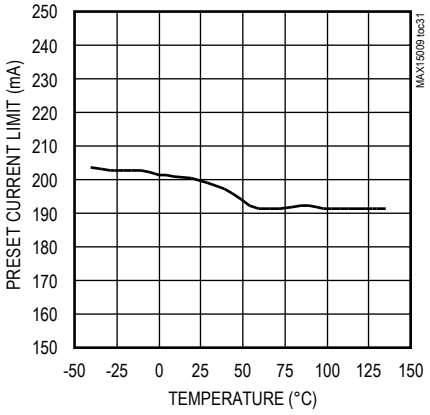
RESET TIMEOUT DELAY vs. TEMPERATURE



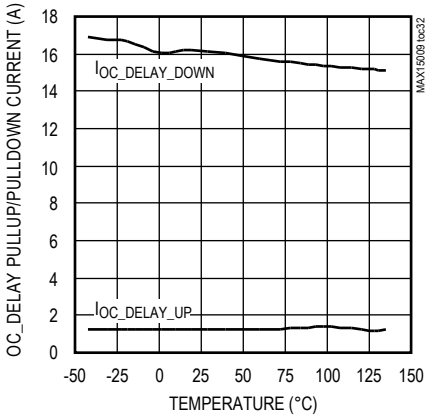
SWITCH CURRENT LIMIT vs. ILIM RESISTANCE



INTERNAL PRESET SWITCH CURRENT LIMIT vs. TEMPERATURE



IOC_DELAY_UP AND IOC_DELAY_DOWN vs. TEMPERATURE



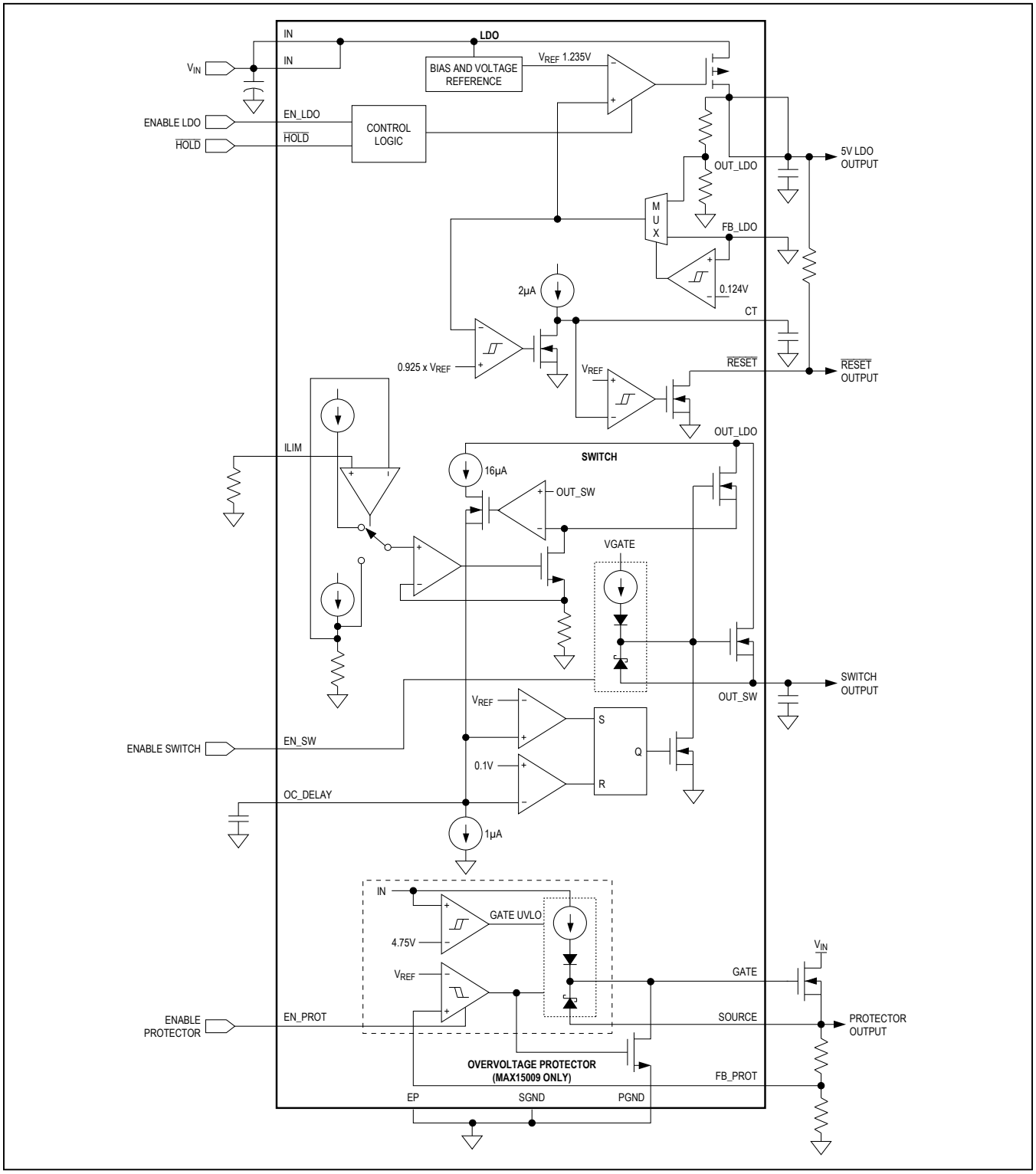
Pin Description

PIN	NAME		FUNCTION
	MAX15009	MAX15011	
1–4, 8, 11, 14, 26, 29–32	N.C.	—	No Connection. Not internally connected.
1–4, 8, 10–14, 18, 26, 29–32	—	N.C.	
5	SGND	SGND	Signal Ground
6	PGND	PGND	Ground. PGND is also the return path for the overvoltage protector pulldown current for the MAX15009. In this case, connect PGND to SGND at the negative terminal of the bypass capacitor connected to the source of the external MOSFET. For the MAX15011, connect PGND to SGND together to the local ground plane.
7	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Active-Low Open-Drain Reset Output. $\overline{\text{RESET}}$ is low while OUT_LDO is below the reset threshold. Once OUT_LDO has exceeded the reset threshold, $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period then goes high.
9	CT	CT	Reset Timeout Adjust Input. Connect a capacitor ($C_{\overline{\text{RESET}}}$) from CT to ground to adjust the reset timeout period. See the *Setting the $\overline{\text{RESET}}$ Timeout Period* section.
10	FB_PROT	—	Overvoltage-Threshold Adjustment Input. Connect FB_PROT to an external resistive voltage-divider network to adjust the desired overvoltage threshold. Use FB_PROT to monitor a system input or output voltage. See the *Setting the Overvoltage Threshold (MAX15009 Only)* section.
12	GATE	—	Protector Gate Drive Output. Connect GATE to the gate of an external n-channel MOSFET. GATE is the output of a charge pump with a 45µA pullup current to 8.1V (typ) above IN during normal operation. GATE is quickly turned off through a 63mA internal pulldown during an overvoltage condition. GATE then remains low until FB_PROT has decreased below 96% of the overvoltage threshold. GATE pulls low when EN_PROT is low.
13	SOURCE	—	Output-Voltage Sense Input. Connect SOURCE to the source of the external n-channel MOSFET.

Pin Description (continued)

PIN	NAME		FUNCTION
	MAX15009	MAX15011	
15	FB_LDO	FB_LDO	LDO Voltage Feedback Input. Connect FB_LDO to SGND to select the preset +5V output voltage. Connect FB_LDO to an external resistive voltage-divider for adjustable output operation. See the *Setting the Output Voltage* section.
16	EN_LDO	EN_LDO	Active-High LDO Enable Input. Connect EN_LDO to IN or to a logic-high voltage to turn on the regulator. To place the LDO in shutdown, pull EN_LDO low or leave unconnected and leave $\overline{HOLD}$ unconnected. EN_LDO is internally pulled to SGND through a 1FA current sink. See the *Control Logic* section.
17	EN_SW	EN_SW	Active-High Switch Enable Input. Connect EN_SW to IN or to a logic-high voltage to turn on the switch. Pull EN_SW low or leave unconnected to place the switch in shutdown. EN_SW is internally pulled to SGND through a 1µA current sink.
18	EN_PROT	—	Protector Enable Input. Drive EN_PROT low to force GATE low and turn off the external n-channel MOSFET. EN_PROT is internally pulled to SGND by a 1µA sink current. Connect EN_PROT to IN for normal operation.
19, 20	IN	IN	Regulator Input. Bypass IN to SGND with a 10µF capacitor with an ESR < 1.5Ω.
21, 22	OUT_LDO	OUT_LDO	LDO Regulator Output. Bypass OUT_LDO to SGND with a ceramic capacitor with a minimum value of 22µF. OUT_LDO has a fixed 5V output or can be adjusted from 1.8V to 11V. See the *Setting the Output Voltage* section.
23	OC_DELAY	OC_DELAY	Switch Overcurrent Blanking Time Programming Input. Leave OC_DELAY unconnected to select the minimum delay timeout before turning the switch off. OC_DELAY is internally pulled to SGND through a 1µA current source. See the *Programming the Switch Overcurrent Blanking Time* section.
24	ILIM	ILIM	Switch Current-Limit Set Input. Connect a 10kΩ to 200kΩ resistor from ILIM to SGND to select the current limit for the internal switch. Connect ILIM to OUT_LDO to select the internal 170mA (min) current-limit threshold. Do not leave ILIM unconnected. See the *Setting the Switch Current Limit* section.
25	$\overline{HOLD}$	$\overline{HOLD}$	Active-Low Hold Input. If EN_LDO is high when $\overline{HOLD}$ is forced low, the regulator latches the state of the EN_LDO input and allows the regulator to remain turned on when EN_LDO is subsequently pulled low. To shut down the regulator, release $\overline{HOLD}$ after EN_LDO is pulled low. If $\overline{HOLD}$ functionality is unused, connect $\overline{HOLD}$ to OUT_LDO or leave unconnected. $\overline{HOLD}$ is internally pulled up to OUT_LDO through a 0.6µA current source. See the *Control Logic* sectio
27, 28	OUT_SW	OUT_SW	Switch Output. Bypass OUT_SW to SGND with a minimum 0.1µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect EP to SGND plane. EP also functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

Functional Diagram



Detailed Description

The MAX15009/MAX15011 integrate a 300mA LDO voltage regulator, a current-limited switched output, and an OVP controller (MAX15009 only). These devices operate over a wide supply voltage range from 5V to 40V and are able to withstand load-dump transients up to 45V.

The MAX15009/MAX15011 feature a 300mA LDO regulator that consumes 70µA of current under light-load conditions and feature a fixed 5V or an adjustable output voltage (1.8V to 11V). Connect FB_LDO to ground to select a fixed 5V output voltage, or select the LDO output voltage by connecting an external resistive voltage-divider at FB_LDO. The regulator sources at least 300mA of current and includes a current limit of 330mA (min). Enable the LDO by pulling EN_LDO high.

The switch features accurate current-limit-sensing circuitry and is capable of controlling remote loads. Once enabled, an internal charge pump generates the overdrive voltage for an internal MOSFET. The switch then starts to conduct and OUT_SW is charged up to V_{OUT_LDO}. The switch is enabled when the output voltage of the LDO is above the $\overline{RESET}$ threshold voltage (92.5% of the LDO nominal output value).

An overcurrent condition exists when the current at OUT_SW (I_{OUT_SW}) exceeds the 200mA (typ) internal factory-set current-limit threshold or the externally adjustable current-limit threshold. During a continuous overcurrent event, the capacitor connected at OC_DELAY (C_{OC_DELAY}) is charged up to a voltage of 1.235V with a current ($I_{OC_DELAY_UP}$). When this voltage is reached, an overcurrent latch is set and the gate of the internal MOSFET is discharged, reducing I_{OUT_SW}. C_{OC_DELAY} is then discharged through a pulldown current, $I_{OC_DELAY_DOWN}$ ($I_{OC_DELAY_UP}$/16) and the internal MOSFET remains off until C_{OC_DELAY} has been discharged to 0.1V. After this user-programmable turnoff delay, the switch turns back on. This charge/discharge is repeated if the overcurrent condition persists. The switch returns to normal operation once the overcurrent condition has been removed.

The OVP controller (MAX15009 only) relies on an external MOSFET with adequate voltage rating (V_{DSS}) to protect downstream circuitry from overvoltage transients. The OVP controller drives the gate of the external n-channel MOSFET, and is configurable to operate as an overvoltage protection switch or as a closed-loop voltage limiter.

GATE Voltage (MAX15009 Only)

The MAX15009 uses a high-efficiency charge pump to generate the GATE voltage for the external n-channel MOSFET. Once the input voltage (V_{IN}) exceeds the undervoltage-lockout (UVLO) threshold, the internal charge pump fully enhances the external n-channel MOSFET. An overvoltage condition occurs when the voltage at FB_PROT goes above the threshold voltage (V_{TH_PROT}). After V_{TH_PROT} is exceeded, GATE is quickly pulled to PGND with a 63mA pulldown current. The MAX15009 includes an internal clamp from GATE to SOURCE that ensures that the voltage at GATE never exceeds one diode drop below SOURCE during gate discharge. The voltage clamp also prevents the GATE-to-SOURCE voltage from exceeding the absolute maximum rating for the V_{GS} of the external MOSFET in case the source terminal is accidentally shorted to 0V.

Overvoltage Monitoring (MAX15009 Only)

The OVP controller monitors the voltage at FB_PROT and controls an external n-channel MOSFET, isolating, or limiting the load during an overvoltage condition. Operation in OVP switch mode or limiter mode depends on the connection between FB_PROT and the external MOSFET.

Overvoltage Switch Mode

When operating in OVP switch mode, the FB_PROT divider is connected to the drain of the external MOSFET. The feedback path consists of the voltage-divider tapped at FB_PROT, FB_PROT's internal comparator, the internal gate-charge pump/gate pulldown, and the external n-channel MOSFET (Figure 1). When the programmed overvoltage threshold is exceeded, the internal comparator quickly pulls GATE to ground and turns off the

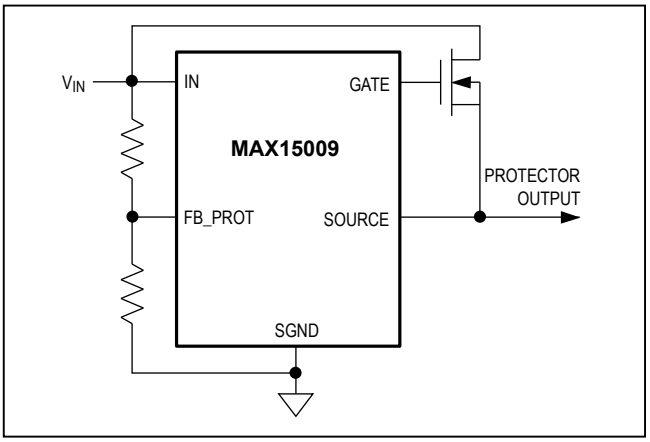


Figure 1. Overvoltage-Limiter Switch Configuration (MAX15009)

external MOSFET, disconnecting the power source from the load. In this configuration, the voltage at the source of the MOSFET is not monitored. When the voltage at FB_PROT decreases below the overvoltage threshold, the MAX15009 raises the voltage at GATE, reconnecting the load to the power source.

Overvoltage-Limiter Mode (MAX15009 Only)

When operating in overvoltage-limiter mode, the feedback path consists of SOURCE, FB_PROT's internal comparator, the internal gate-charge pump/gate pulldown, and the external n-channel MOSFET (Figure 2). This configuration results in the external MOSFET operating as a hysteretic voltage regulator.

During normal operation, GATE is enhanced 8.1V above V_{IN}. The external MOSFET source voltage is monitored through a resistive voltage-divider between SOURCE and FB_PROT. When V_{SOURCE} exceeds the adjustable overvoltage threshold, an internal pulldown switch discharges the gate voltage and quickly turns the MOSFET off. Consequently, the source voltage begins to fall. The V_{SOURCE} fall time is dependent on the MOSFET's gate charge, the internal charge-pump current, the output load, and any load capacitance at SOURCE. When the voltage at FB_PROT is below the overvoltage threshold by an amount equal to the hysteresis, the charge pump restarts and turns the MOSFET back on. In this way, the OVP controller attempts to regulate V_{SOURCE} around the overvoltage threshold. SOURCE remains high during overvoltage transients and the MOSFET continues to conduct during an overvoltage event. The hysteresis of the FB_PROT comparator and the gate turn-on delay force the external MOSFET to operate in a switched on/off sequence during an overvoltage event.

Exercise caution when operating the MAX15009 in voltage-limiting mode for long durations. Care must be taken against prolonged or repeated exposure to overvoltage events while delivering large amounts of load current, as the power dissipation in the external MOSFET may be high under these conditions. To prevent damage to the MOSFET, implement proper heatsinking. The capacitor tied between SOURCE and ground may also be damaged if the ripple current rating for the capacitor is exceeded.

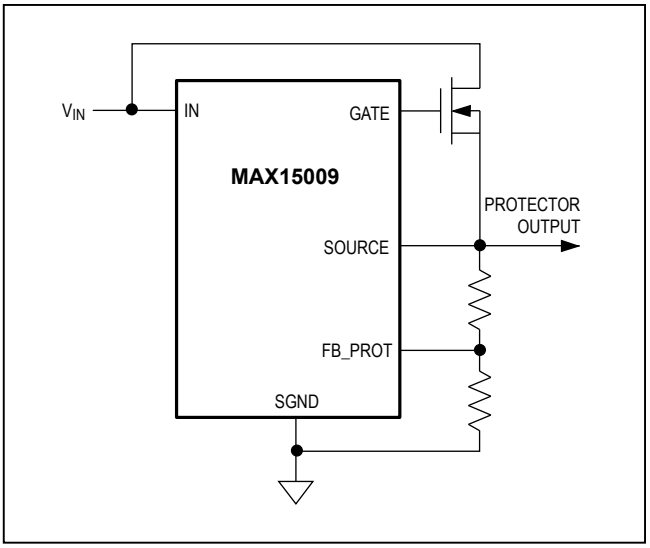


Figure 2. Overvoltage Limiter (MAX15009)

As the transient voltage decreases, the voltage at SOURCE falls. For fast-rising transients and very large MOSFETs, connect an additional capacitor from GATE to PGND. This capacitor acts as a voltage-divider working against the MOSFET's drain-to-gate capacitance. If using a very low gate-charge MOSFET, additional capacitance from GATE to ground might be required to reduce the switching frequency.

Control Logic

The MAX15009/MAX15011 LDO features two logic inputs, EN_LDO and $\overline{HOLD}$. For example, when the ignition key signal drives EN_LDO high, the regulator turns on and remains on even if EN_LDO goes low, as long as $\overline{HOLD}$ is forced low and stays low after initial regulator power-up. In this state, releasing $\overline{HOLD}$ turns the regulator output (OUT_LDO) off. This feature makes it possible to implement a self-holding circuit without external components. Forcing EN_LDO low and $\overline{HOLD}$ high (or unconnected) places the regulator into shutdown mode, reducing the supply current to less than 16µA. Table 1 shows the state of OUT_LDO with respect to EN_LDO and $\overline{HOLD}$. Leave $\overline{HOLD}$ unconnected or connect directly to OUT_LDO to allow the EN_LDO input to act as a standard on/off logic input for the regulator.

Table 1. EN_LDO/HOLD Truth/State Table

OPERATION STATE	EN_LDO	$\overline{HOLD}$	OUT_LDO	COMMENT
Initial State	Low	Don't care	OFF	EN_LDO is pulled to SGND through an internal pulldown. $\overline{HOLD}$ is unconnected and is internally pulled up to OUT_LDO. The regulator is disabled.
Turn-On State	High	Don't care	ON	EN_LDO is externally driven high turning regulator on. $\overline{HOLD}$ is pulled up to OUT_LDO.
Hold Setup State	High	Low	ON	$\overline{HOLD}$ is externally pulled low while EN_LDO remains high (latches EN_LDO state).
Hold State	Low	Low	ON	EN_LDO is driven low or left unconnected. $\overline{HOLD}$ remains externally pulled low keeping the regulator on.
Off State	Low	High or unconnected	OFF	$\overline{HOLD}$ is driven high or left unconnected while EN_LDO is low. The regulator is turned off and EN_LDO/$\overline{HOLD}$ logic returns to the initial state.

Applications Information

Setting the Output Voltage

The MAX15009/MAX15011 feature dual-mode operation: these devices operate in either a preset voltage mode or an adjustable mode. In preset-voltage mode, internal feedback resistors set the linear regulator output voltage (V_{OUT_LDO}) to 5V. To select the preset 5V output voltage, connect FB_LDO to SGND.

To select an adjustable output voltage between 1.8V and 11V, use two external resistors connected as a voltage-divider to FB_LDO (Figure 3). Set the output voltage using the following equation:

$$V_{OUT_LDO} = V_{FB_LDO} \times (R_1 + R_2) / R_2$$

where V_{FB_LDO} = 1.235V and $R_2 \le 50k\Omega$.

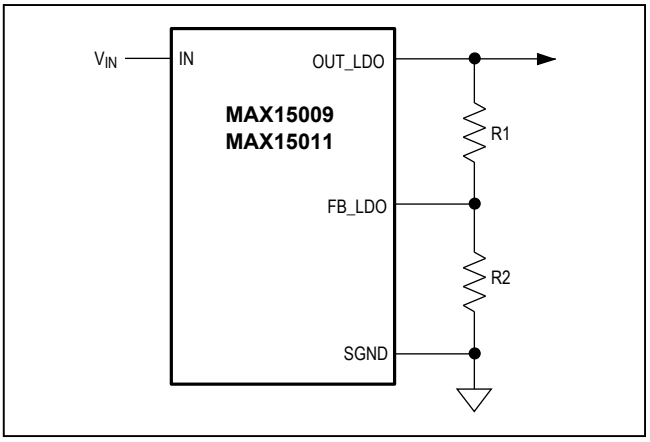


Figure 3. Setting the LDO Output Voltage

Setting the $\overline{RESET}$ Timeout Period

The reset-timeout period is adjustable to accommodate a variety of applications. Set the reset-timeout period by connecting a capacitor (CRESET) between CT and SGND. Use the following formula to select the reset-timeout period (t_{RESET}):

$$t_{RESET} = C_{RESET} \times V_{CT_TH}/I_{CT}$$

where t_{RESET} is in seconds and C_{RESET} is in µF. V_{CT_TH} is the CT ramp threshold in volts and I_{CT} is the CT ramp current in µA, as described in the *Electrical Characteristics* table.

Leave CT open to select a typical reset timeout of 19µs. To maintain reset accuracy, use a low-leakage type of capacitor.

Setting the Switch Current Limit

The switch block features accurate current-limit-sensing circuitry. A resistor connected from ILIM to SGND can be used to select the current-limit threshold using the following relationship:

$$I_{SW_LIM}\ (mA) = R_{ILIM}\ (k\Omega) \times 1mA/k\Omega$$

where $20k\Omega \le R_{ILIM} \le 200k\Omega$.

Connect ILIM to OUT_LDO to select the default current limit of 200mA (typ).

Programming the Switch Overcurrent Blanking Time

The switch provides an adjustable overcurrent blanking time to allow the safe charge of large capacitive loads. When an overcurrent event is detected, a delay period elapses before the condition is latched and the internal MOSFET is turned off. This period is the overcurrent delay (t_{OC_DELAY}). Set the overcurrent delay using the following equation:

$$t_{OC_DELAY} = C_{OC_DELAY} \times V_{OC_DELAY}/I_{OC_DELAY_UP}$$

where t_{OC_DELAY} is in seconds and C_{OC_DELAY} is in µF. V_{OC_DELAY} is the overcurrent-delay timeout threshold voltage in volts and $I_{OC_DELAY_UP}$ is the overcurrent-delay timeout pullup current in µA, as seen in the *Electrical Characteristics* table.

Ensure that the switch is not disabled due to a large startup inrush current by selecting a large enough value for overcurrent blanking time. Assume that the current available for charging the total switch output capacitance (C_{OUT_SW}) is the difference between the current-limit threshold value (I_{SW_LIM}), and the nominal DC load current at OUT_SW ($I_{OUT_SW_NOM}$), and select the C_{OC_DELAY} using the following relationship:

$$C_{OC_DELAY} \geq \frac{I_{OC_DELAY_UP} \times V_{OUT_LDO} \times C_{OUT_SW}}{V_{OC_DELAY} \times (I_{SW_LIM} - I_{OUT_SW_NOM})}$$

C_{OC_DELAY} also affects the length of time before the MAX15009/MAX15011 attempt to turn the switch back on. Set the autoretry delay using the following equation:

$$t_{OC_RETRY} = C_{OC_DELAY} \times V_{OC_DELAY}/I_{OC_DELAY_DOWN}$$

where t_{OC_RETRY} is in seconds, C_{OC_DELAY} is in µF, V_{OC_DELAY} is in volts, and $I_{OC_DELAY_DOWN}$ is in µA.

C_{OC_DELAY} should be a low-leakage type of capacitor with a minimum value of 100pF.

Setting the Overvoltage Threshold (MAX15009 Only)

The MAX15009 provides an accurate means to set the overvoltage threshold for the OVP controller using FB_PROT. Use a resistive voltage-divider to set the desired overvoltage threshold (Figure 4). FB_PROT has a rising 1.235V threshold with a 4% falling hysteresis.

Begin by selecting the total end-to-end resistance, $R_{TOTAL} = R_3 + R_4$. Choose R_{TOTAL} to yield a total current equivalent to a minimum of 100 x I_{FB_PROT} (FB_PROT's input maximum bias current) at the desired overvoltage threshold. See the *Electrical Characteristics* table.

For example:

With an overvoltage threshold (V_{OV}) set to 20V, R_{TOTAL} < 20V/(100 x I_{FB_PROT}), where I_{FB_PROT} is FB_PROT's maximum 100nA bias current:

$$R_{TOTAL} < 2M\Omega$$

Use the following formula to calculate R_4:

$$R_4 = V_{TH_PROT} \times R_{TOTAL} / V_{OV}$$

where V_{TH_PROT} is the 1.235V FB_PROT rising threshold and V_{OV} is the desired overvoltage threshold. R_4 = 124kΩ:

$$R_{TOTAL} = R_3 + R_4$$

where R_3 = 1.88MΩ. Use a standard 1.87MΩ resistor.

A lower value for total resistance dissipates more power, but provides better accuracy and robustness against external disturbances.

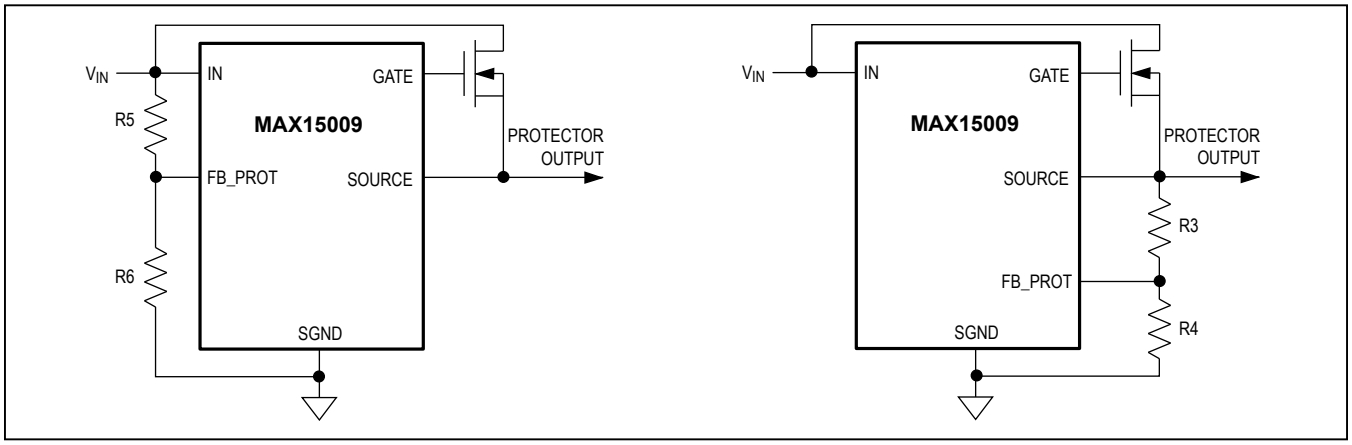


Figure 4. Setting the Overvoltage Threshold (MAX15009)

Input Transients Clamping

When the external MOSFET is turned off during an overvoltage event, stray inductance in the power path may cause additional input-voltage spikes that exceed the V_{DSS} rating of the external MOSFET, or the absolute maximum rating for the MAX15009. Minimize stray inductance in the power path using wide traces and minimize the loop area included by the power traces and the return ground path.

For further protection, add a zener diode or transient voltage suppressor (TVS) rated below the absolute maximum rating limits (Figure 5).

External MOSFET Selection

Select the external MOSFET with adequate voltage rating (V_{DSS}) to withstand the maximum expected load-dump input voltage. The on-resistance of the MOSFET ($R_{DS(ON)}$) should be low enough to maintain a minimal voltage drop at full load, limiting the power dissipation of the MOSFET.

During regular operation, the power dissipated by the MOSFET is:

$$P_{NORMAL} = I_{LOAD}^2 \times R_{DS(ON)}$$

Normally, this power loss is small and is safely handled by the MOSFET; however, when operating the MAX15009 in overvoltage-limiter mode under prolonged or frequent overvoltage events, select an external MOSFET with an appropriate power rating.

During an overvoltage event, the power dissipation in the external MOSFET is proportional to both load current and to the drain-source voltage, resulting in high power dissipated in the MOSFET (Figure 6). The power dissipated across the MOSFET is:

$$P_{OV_LIMITER} = V_{Q1} \times I_{LOAD}$$

where V_{Q1} is the voltage across the MOSFET's drain and source during overvoltage-limiter operation, and I_{LOAD} is the load current.

Overvoltage-Limiter Mode Switching Frequency

When the MAX15009 is configured in overvoltage-limiter mode, the external n-channel MOSFET is subsequently switched on and off during an overvoltage event. The output voltage at OUT_PROT resembles a periodic sawtooth waveform. Calculate the period of the waveform (t_{OVP}) by summing three time intervals (Figure 7):

$$t_{OVP} = t_1 + t_2 + t_3$$

where t_1 is the V_{SOURCE} output discharge time, t_2 is the GATE delay time, and t3 is the V_{SOURCE} output charge time.

During an overvoltage event, the power dissipated inside the MAX15009 is due to the gate pulldown current

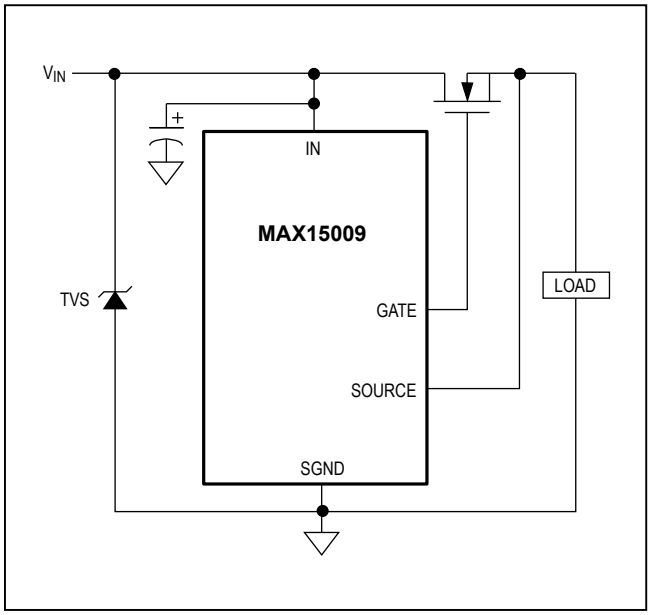


Figure 5. Protecting the MAX15009 Input from High-Voltage Transients

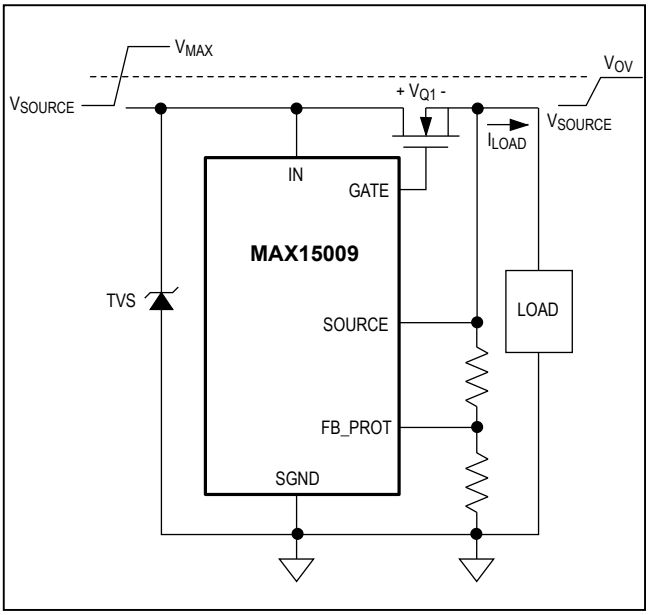


Figure 6. Power Dissipated Across MOSFETs During an Overvoltage Fault (Overvoltage Limiter Mode)

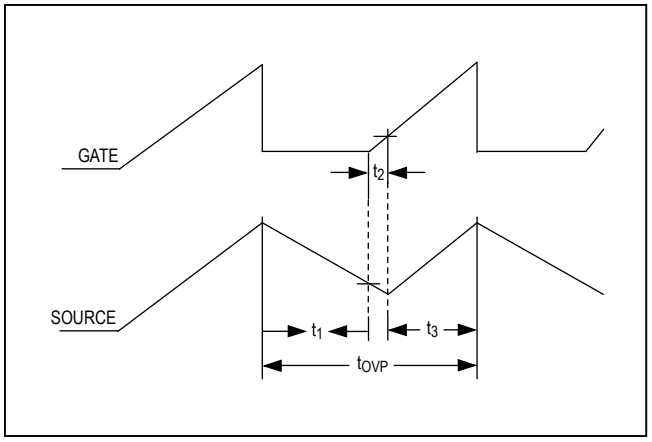


Figure 7. MAX15009 Timing Diagram

(I_{GATEPD}) . This amount of power dissipation is worse when I_{SOURCE} = 0 (C_{SOURCE} is discharged only by the internal current sink).

The worst-case internal power dissipation contribution in overvoltage limiter mode (P_{OVP}) in watts can be approximated using the following equation:

$$P_{OVP} = V_{OV} \times 0.98 \times I_{GATEPD} \times \frac{t_1}{t_{OVP}}$$

where V_{OV} is the overvoltage threshold voltage in volts and I_{GATEPD} is 100mA (max) GATE pulldown current.

Output Discharge Time (t_1)

When the voltage at SOURCE exceeds the adjusted overvoltage threshold, GATE's internal pulldown is enabled until V_{SOURCE} drops by 4%. The internal current sink (I_{GATEPD}) and the external load current (I_{LOAD}) discharge the external capacitance from SOURCE to ground.

Calculate the discharge time (t_1) using the following equation:

$$t_1 = C_{SOURCE} \times \frac{0.04 \times V_{OV}}{I_{LOAD} + I_{GATEPD}}$$

where t_1 is in ms, V_{OV} is the adjusted overvoltage threshold in volts, I_{LOAD} is the external load current in mA, and I_{GATEPD} is the 100mA (max) internal pulldown current of GATE. C_{SOURCE} is the value of the capacitor connected between the source of the MOSFET and PGND in µF.

GATE Delay Time (t_2)

When SOURCE falls 4% below the overvoltage-threshold voltage, the internal current sink is disabled and the internal charge pump begins recharging the external GATE voltage. Due to the external load, the SOURCE voltage continues to drop until the gate of the MOSFET is recharged. The time needed to recharge GATE and reenhance the external MOSFET is approximately:

$$t_2 = C_{iss} \times \frac{V_{GS(TH)} + V_F}{I_{GATE}}$$

where t_2 is in µs, C_{iss} is the input capacitance of the MOSFET in pF, and $V_{GS(TH)}$ is the GATE-to-SOURCE threshold voltage of the MOSFET in volts. V_F is the 0.7V (typ) internal clamp-diode forward voltage of the MOSFET in volts, and I_{GATE} is the charge-pump current 45µA (typ). Any external capacitance between GATE and PGND adds up to C_{iss}.

During t_2, the SOURCE capacitance (C_{SOURCE}) loses charge through the output load. The voltage across C_{SOURCE}, ΔV_2, decreases until the MOSFET reaches its $V_{GS(TH)}$ threshold. Approximate ΔV_2 using the following formula:

$$\Delta V_2 = \frac{I_{LOAD} \times t_2}{C_{SOURCE}}$$

SOURCE Output Charge Time (t_3)

Once the GATE voltage exceeds the GATE-to-SOURCE threshold ($V_{GS(TH)}$) of the external MOSFET, the MOSFET turns on and the charge through the internal charge pump with respect to the drain potential (Q_G) determines the slope of the output voltage rise. The time required for the SOURCE voltage to rise again to the overvoltage threshold is:

$$t_3 = \frac{C_{rss} \times \Delta V_{SOURCE}}{I_{GATE}}$$

where V_{SOURCE} = (V_{OV} x 0.04) + V_2 in volts, and C_{rss} is the MOSFET's reverse transfer capacitance in pF. Any external capacitance between GATE and PGND adds up to C_{rss}.

Power Dissipation/Junction Temperature

During normal operation, the MAX15009/MAX15011 have two main sources of internal power dissipation: the LDO and the switched output.

The internal power dissipation due to the LDO can be calculated as:

$$P_{LDO} = (V_{IN} - V_{OUT_LDO}) \times (I_{OUT_LDO} + I_{OUT_SW})$$

where V_{IN} is the LDO input supply voltage in volts, V_{OUT_LDO} is the output voltage of the LDO in volts, I_{OUT_LDO} is the LDO total load current in mA, and I_{OUT_SW} is the switch load current in mA.

Calculate the power dissipation due to the switch as:

$$P_{SW} = \Delta V_{SW} \times I_{OUT_SW}$$

where ΔV_{SW} is the switch dropout voltage in volts for the given I_{OUT_SW} current in mA.

The total power dissipation (P_{DISS}) in mW as:

$$P_{DISS} = P_{LDO} + P_{SW}$$

For prolonged exposure to overvoltage events, use the V_{IN} voltage expected during overvoltage conditions. Under these circumstances the corresponding internal power dissipation contribution (P_{OVP}) calculated in the previous section should also be included in the total power dissipation (P_{DISS}).

For a given ambient temperature (T_A) calculate the junction temperature (T_J) as follows:

$$T_J = T_A + P_{DISS} \times \theta_{JA}$$

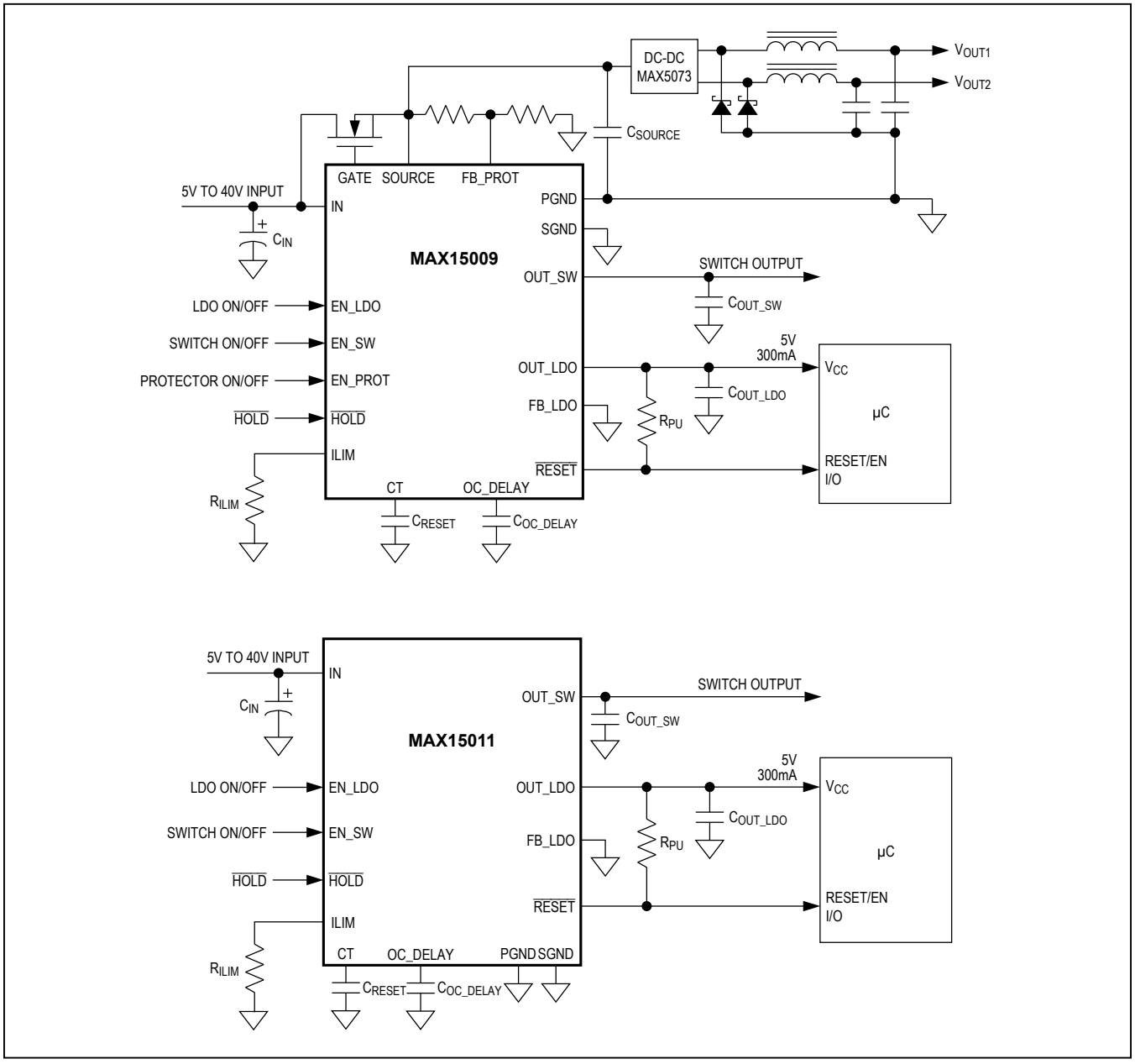
where T_J and T_A are in °C and θ_{JA} is the junction-to-ambient thermal resistance in °C/W, as listed in the *Absolute Maximum Ratings* section.

The junction temperature should never exceed +150°C during normal operation.

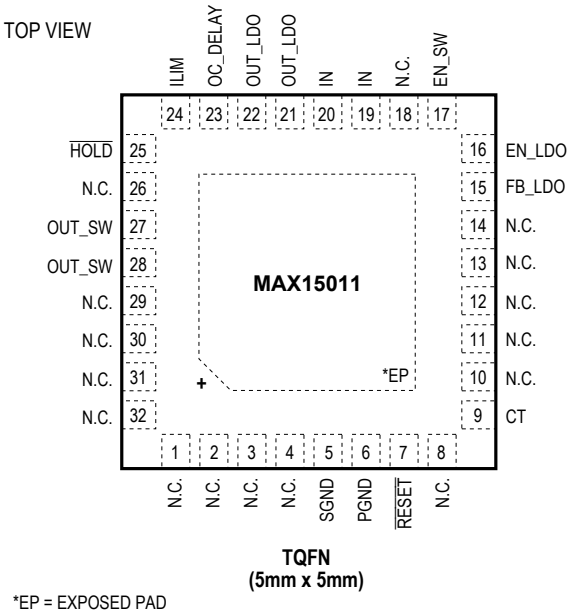
Thermal Protection

When the junction temperature exceeds T_J = +160°C, the MAX15009/MAX15011 shut down to allow the device to cool. When the junction temperature drops to +140°C, the thermal sensor turns all enabled blocks on again, resulting in a cycled output during continuous thermal-overload conditions. Thermal protection protects the MAX15009/MAX15011 from excessive power dissipation. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Typical Operating Circuits



Pin Configurations (continued)



Selector Guide

PART	LDO	SWITCHED OUTPUT	OVP CONTROLLER
MAX15009	√	√	√
MAX15011	√	√	—

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/07	Initial release	—
1	1/08	Removed future product asterisks, updated *Electrical Characteristics* table and *Typical Operating Characteristics* section.	1, 2, 6, 8
2	11/14	No /V OPN in *Ordering Information*; removed automotive references and deleted *Load-Dump* section	1, 14, 15

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