19-3979; Rev 0; 2/06

Overvoltage-Protection Controllers with Status FLAG

General Description

The MAX4838A/MAX4840A/MAX4842A are overvoltage-protection ICs that protect low-voltage systems against voltages of up to +28V. If the input voltage exceeds the overvoltage trip level, the MAX4838A/MAX4840A/MAX4842A turn off the low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the FET gate for a simple, robust solution.

The MAX4838A has a 7.4V overvoltage threshold, and the MAX4840A has a 5.8V overvoltage threshold. The MAX4842A has a 4.7V overvoltage threshold. The MAX4838A/MAX4840A have an undervoltage-lockout (UVLO) threshold of 3.25V, while the MAX4842A has a UVLO of 2.5V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter.

On power-up, the device waits for 50ms before driving GATE high. $\overline{FLAG}$ is held low for an additional 50ms after GATE goes high before deasserting. The MAX4838A/MAX4840A/MAX4842A have an open-drain $\overline{FLAG}$ output. The $\overline{FLAG}$ output asserts immediately to an overvoltage fault.

Additional features include a ±15kV (HBM) ESD-protected input (when bypassed with a 1µF capacitor) and a shutdown pin ($\overline{EN}$) to turn off the device.

All devices are offered in a small 6-pin SC70 and 6-pin 1.5mm x 1.0mm µDFN packages and are specified over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

Digital Still Cameras

PDAs and Palmtop Devices

MP3 Players

Selector Guide

PART	UVLO THRESHOLD (V)	OV TRIP LEVEL (V)	$\overline{EN}$ INPUT	$\overline{FLAG}$ OUTPUT
MAX4838A	3.25	7.4	Yes	Open-Drain
MAX4840A	3.25	5.8	Yes	Open-Drain
MAX4842A	2.50	4.7	Yes	Open-Drain

Features

- ♦ **Overvoltage Protection Up to +28V**
- ♦ **Preset 7.4V, 5.8V, or 4.7V Overvoltage Trip Level**
- ♦ **Drives Low-Cost nMOS FET**
- ♦ **Internal 50ms Startup Delay**
- ♦ **Internal Charge Pump**
- ♦ **Undervoltage Lockout**
- ♦ **±15kV ESD-Protected Input**
- ♦ **Voltage Fault $\overline{FLAG}$ Indicator**
- ♦ **6-Pin SC70 and µDFN Packages**
- ♦ **Lead Free**

Ordering Information

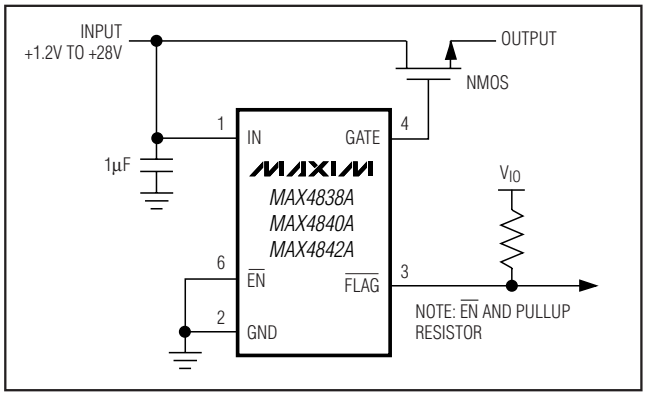
PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX4838AEXT+T	6 SC70	ACY	X6S-1
MAX4838AELT+	6 µDFN	KU	L611-1
MAX4840AEXT+T	6 SC70	ACZ	X6S-1
MAX4840AELT+	6 µDFN	KV	L611-1
MAX4842AEXT+T	6 SC70	ADA	X6S-1
MAX4842AELT+*	6 µDFN	KW	L611-1

Note: *All devices specified for the -40°C to +85°C extended temperature range.*

**Future product—contact factory for availability.*

+Denotes lead-free package.

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

Overvoltage-Protection Controllers with Status $\overline{\text{FLAG}}$

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
GATE to GND .....-0.3V to +12V
$\overline{\text{EN}}$, $\overline{\text{FLAG}}$ to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
6-Pin µDFN (derate 2.1mW/°C above +70°C) 477mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V (MAX4838A/MAX4840A), V_{IN} = +4V (MAX4842A), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			1.2		28.0	V
Undervoltage-Lockout Threshold	UVLO	V_{IN} falling	MAX4838A/MAX4840A	3.0	3.25	3.5	V
			MAX4842A	2.3	2.5	2.7	
Undervoltage-Lockout Hysteresis					50		mV
Overvoltage Trip Level	OVLO	V_{IN} rising	MAX4838A	7.0	7.4	7.8	V
		V_{IN} rising	MAX4840A	5.5	5.8	6.1	
		V_{IN} rising	MAX4842A	4.4	4.7	5.0	
Overvoltage Trip Level Hysteresis		MAX4838A			100		mV
		MAX4840A			80		
		MAX4842A			50		
IN Supply Current	I_{IN}	No load, $\overline{\text{EN}}$ = GND or 5V, V_{IN} = 5V (MAX4838A/MAX4840A)			80	200	µA
		No load, $\overline{\text{EN}}$ = GND or 4.0V, V_{IN} = 4V (MAX4842A)			75	160	
UVLO Supply Current	I_{UVLO}	V_{IN} = 2.9V (MAX4838A/MAX4840A)				30	µA
		V_{IN} = 2.2V (MAX4842A)				22	
GATE Voltage	V_{GATE}	I_{GATE} sourcing 1µA	MAX4838A/MAX4840A	9		10	V
			MAX4842A	7.5		8.0	
GATE Pulldown Current	I_{PD}	$V_{IN} > V_{OVLO}$, V_{GATE} = 5.5V			27		mA
$\overline{\text{FLAG}}$ Output Low Voltage	V_{OL}	$\overline{\text{FLAG}}$ asserted	1.2V ≤ V_{IN} < UVLO, I_{SINK} = 50µA			0.4	V
			V_{IN} ≥ OVLO, I_{SINK} = 1mA			0.4	
$\overline{\text{FLAG}}$ Output High Leakage	I_{OH}	$V_{\overline{\text{FLAG}}}$ = 5.5V, $\overline{\text{FLAG}}$ deasserted				1	µA
$\overline{\text{EN}}$ Input High Voltage	V_{IH}			1.5			V
$\overline{\text{EN}}$ Input Low Voltage	V_{IL}					0.4	V
$\overline{\text{EN}}$ Input Leakage	I_{LKG}	$\overline{\text{EN}}$ = GND or 5.5V				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +5V (MAX4838A/MAX4840A), V_{IN} = +4V (MAX4842A), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

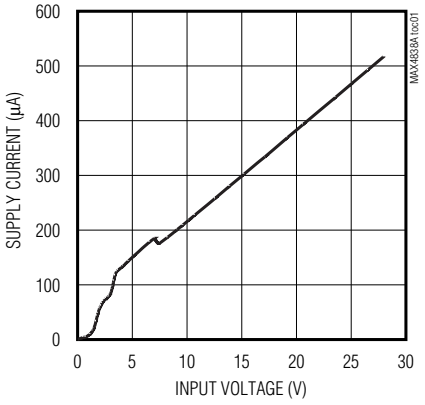
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
Startup Delay	t_{START}	$V_{IN} > V_{UVLO}$, V_{GATE} > 0.3V, Figure 1	20	50	80	ms
$\overline{FLAG}$ Blanking Time	t_{BLANK}	V_{GATE} > 0.3V, $V_{\overline{FLAG}}$ > 2.4V, Figure 1	20	50	80	ms
GATE Turn-On Time	t_{GON}	V_{GATE} = 0.3V to 8V (MAX4838A/MAX4840A), V_{GATE} = 0.3V to 6V (MAX4842A), C_{GATE} = 1500pF, Figure 1		10		ms
GATE Turn-Off Time	t_{GOFF}	V_{IN} increasing from 5V to 8V at 3V/µs (MAX4838A/MAX4840A), V_{IN} increasing from 4V to 6V at 3V/µs (MAX4842A), V_{GATE} = 0.3V, C_{GATE} = 1500pF, Figure 2		6	20	µs
$\overline{FLAG}$ Assertion Delay	$t_{\overline{FLAG}}$	V_{IN} increasing from 5V to 8V at 3V/µs (MAX4838A/MAX4840A), V_{IN} increasing from 4V to 6V at 3V/µs (MAX4842A), V_{FLAG} = 0.4V, Figure 2		5.8		µs
Initial Overvoltage Fault Delay	t_{OVP}	V_{IN} increasing from 0 to 8V (MAX4838A/MAX4840A), V_{IN} increasing from 0V to 6V (MAX4842A), I_{GATE} = 80% of I_{PD}, Figure 3		1.5		µs
Disable Time	t_{DIS}	$V_{\overline{EN}}$ = 2.4V, V_{GATE} = 0.3V, Figure 4		2		µs

Note 1: All parts are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and correlation.

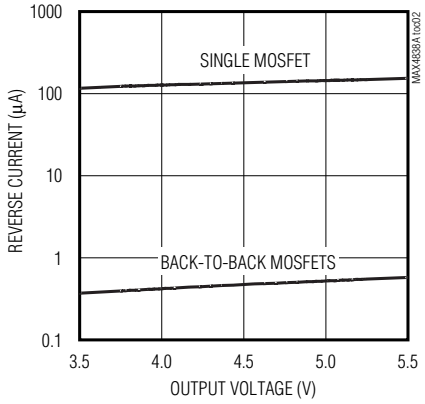
Typical Operating Characteristics

(V_{IN} = +5V (MAX4838A/MAX4840A), V_{IN} = +4V (MAX4842A); Si9936DY external MOSFET in back-to-back configuration; T_A = +25°C, unless otherwise noted.)

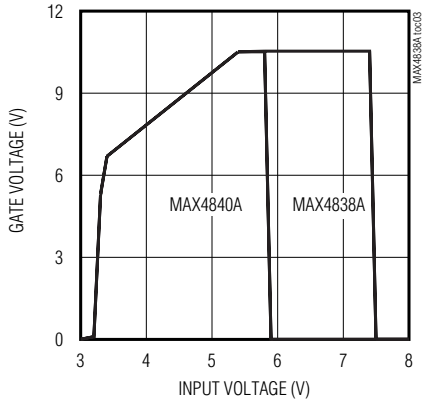
SUPPLY CURRENT vs. INPUT VOLTAGE



REVERSE CURRENT vs. OUTPUT VOLTAGE



MAX4838A/MAX4840A GATE VOLTAGE vs. INPUT VOLTAGE

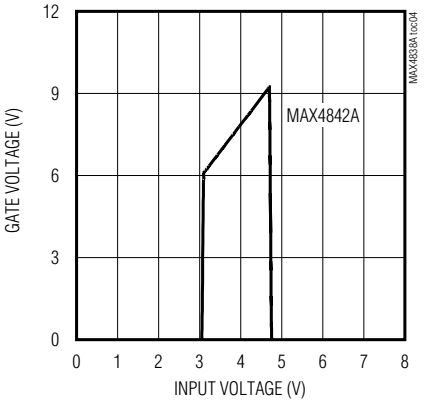


Overvoltage-Protection Controllers with Status $\overline{FLAG}$

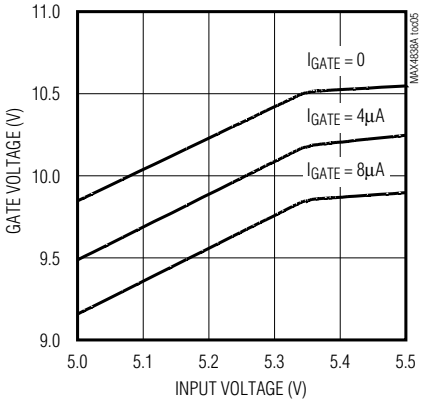
Typical Operating Characteristics (continued)

(V_{IN} = +5V (MAX4838A/MAX4840A), V_{IN} = +4V (MAX4842A); Si9936DY external MOSFET in back-to-back configuration; T_A = +25°C, unless otherwise noted.)

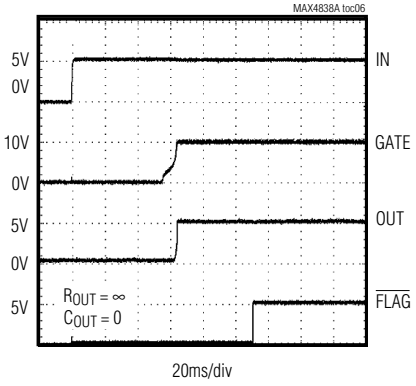
MAX4842A
GATE VOLTAGE vs. INPUT VOLTAGE



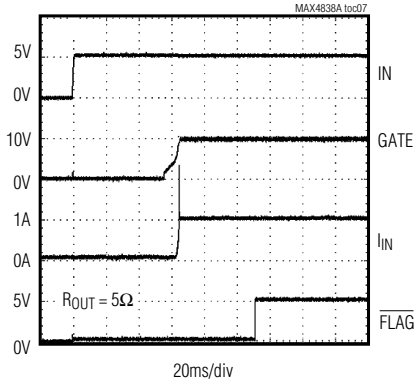
GATE VOLTAGE vs. INPUT VOLTAGE



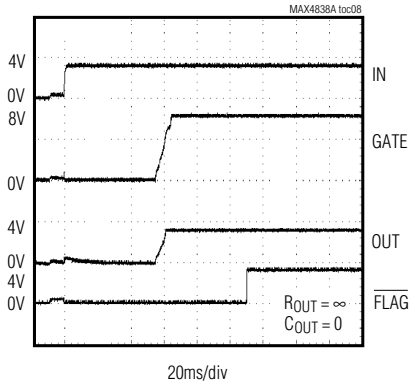
MAX4838A/MAX4840A
POWER-UP RESPONSE



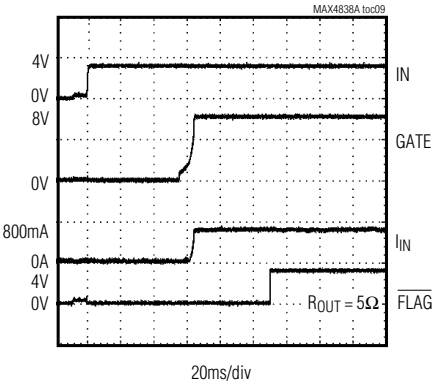
MAX4838A/MAX4840A
POWER-UP RESPONSE



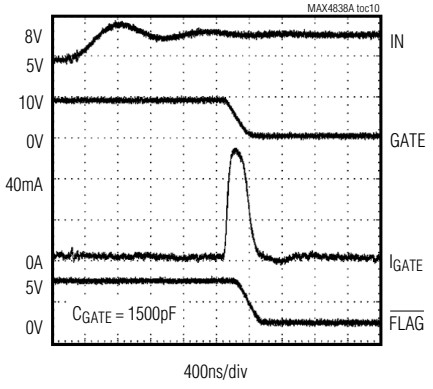
MAX4842A
POWER-UP RESPONSE



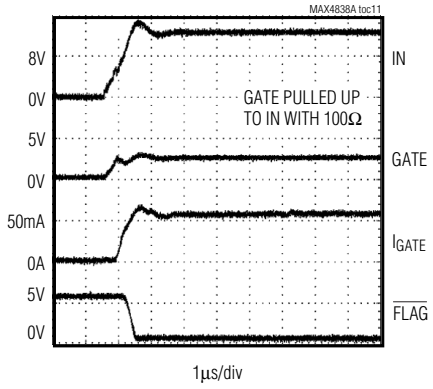
MAX4842A
POWER-UP RESPONSE



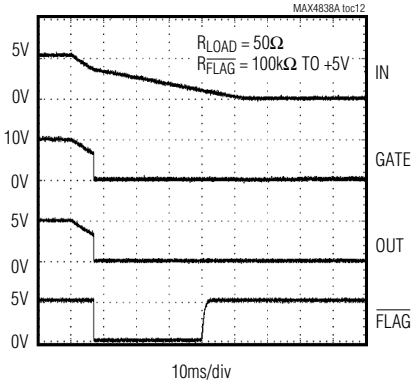
OVERVOLTAGE RESPONSE



POWER-UP OVERVOLTAGE RESPONSE



POWER-DOWN RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	IN	Input. IN is both the power-supply input and the overvoltage sense input. Bypass IN to GND with a 1µF capacitor or larger.
2	GND	Ground
3	$\overline{FLAG}$	Fault Indication Output, Open-Drain, Active Low. $\overline{FLAG}$ is asserted low during undervoltage-lockout and overvoltage-lockout conditions. $\overline{FLAG}$ is deasserted during normal operation.
4	GATE	Gate-Drive Output. GATE is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$, GATE is driven high to turn on the external n-channel MOSFET(s).
5	N.C.	No Connection. Not internally connected for µDFN package. Connected to ground for SC70 6-pin package; connect to ground or leave unconnected.
6	$\overline{EN}$	Device Enable Input, Active Low. Drive $\overline{EN}$ low or connect to ground to allow normal device operation. Drive $\overline{EN}$ high to turn off the external MOSFET.

Timing Diagrams

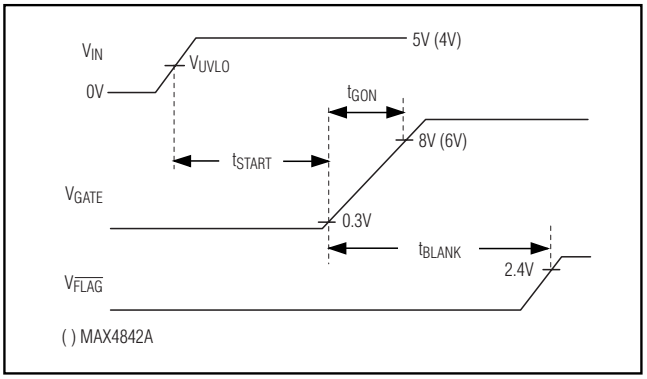


Figure 1. Startup Timing Diagram

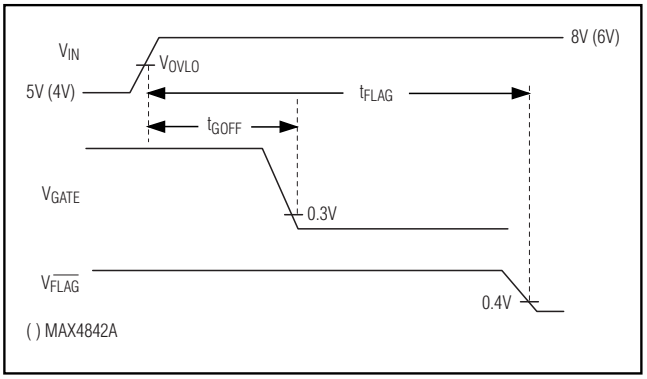


Figure 2. Shutdown Timing Diagram

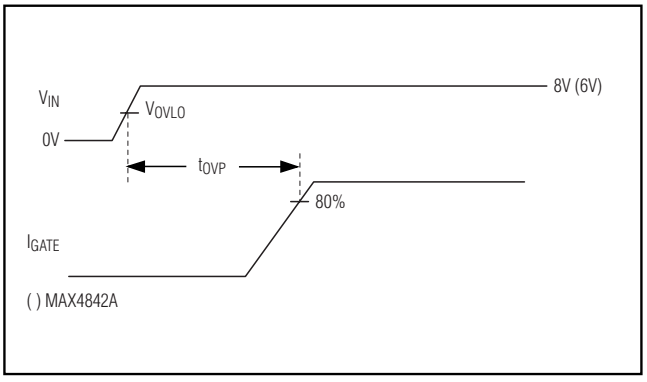


Figure 3. Power-Up Overvoltage Timing Diagram

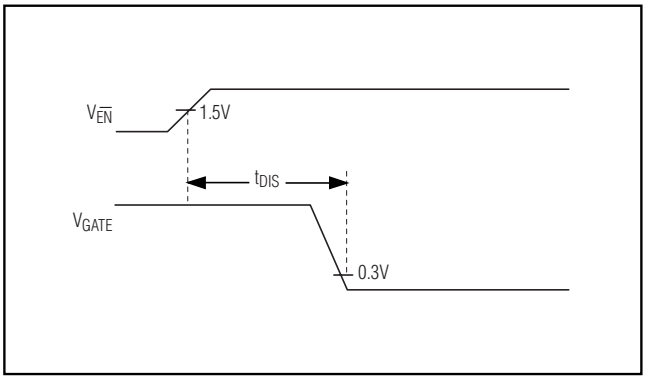


Figure 4. Disable Timing Diagram

Overvoltage-Protection Controllers with Status $\overline{\text{FLAG}}$

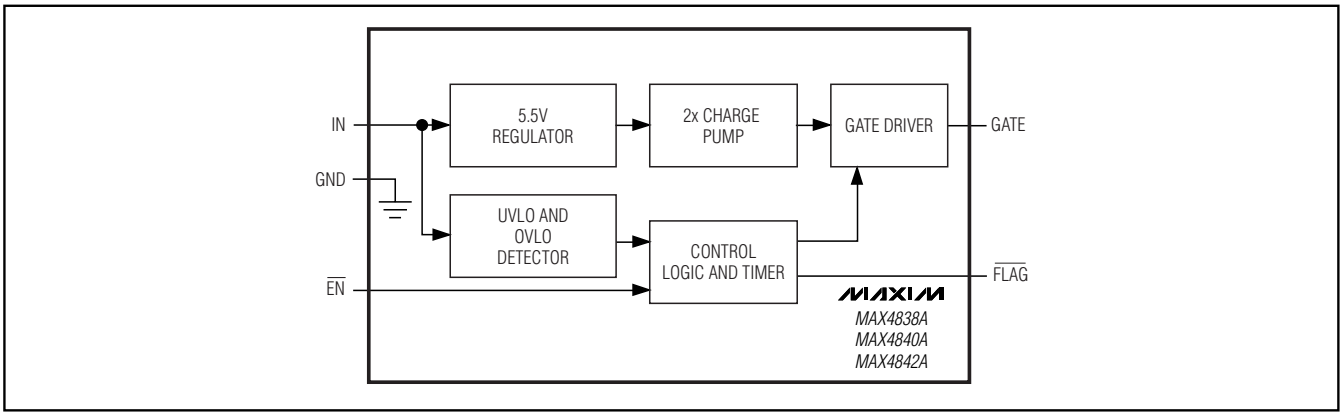


Figure 5. Functional Diagram

Detailed Description

The MAX4838A/MAX4840A/MAX4842A provide up to +28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4838A/MAX4840A/MAX4842A turn off a low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump (Figure 5) drives the FET gate for a simple, robust solution.

Undervoltage Lockout (UVLO)

The MAX4838A/MAX4840A have a fixed 3.25V typical undervoltage-lockout level (UVLO) while the MAX4842A has a 2.5V typical UVLO. When V_{IN} is less than the UVLO, the GATE driver is held low and $\overline{\text{FLAG}}$ is asserted.

Overvoltage Lockout (OVLO)

The MAX4838A has a 7.4V typical overvoltage threshold (OVLO), and the MAX4840A has a 5.8V typical overvoltage threshold. The MAX4842A has a 4.7V typical overvoltage threshold. When V_{IN} is greater than OVLO, the GATE driver is held low and $\overline{\text{FLAG}}$ is asserted.

$\overline{\text{FLAG}}$ Output

The $\overline{\text{FLAG}}$ output is used to signal the host system there is a fault with the input voltage. $\overline{\text{FLAG}}$ asserts immediately to an overvoltage fault. $\overline{\text{FLAG}}$ is held low for 50ms after GATE turns on before deasserting.

All devices have an open-drain $\overline{\text{FLAG}}$ output. Connect a pullup resistor from $\overline{\text{FLAG}}$ to the logic I/O voltage of the host system.

$\overline{\text{EN}}$ Enable Input

$\overline{\text{EN}}$ is an active-low enable input. Drive $\overline{\text{EN}}$ low or connect to ground to enable normal device operation. Drive $\overline{\text{EN}}$ high to force the external MOSFET(s) off. $\overline{\text{EN}}$ does not override an OVLO or UVLO fault.

GATE Driver

An on-chip charge pump is used to drive GATE above IN, allowing the use of low-cost n-channel MOSFETS. The charge pump operates from the internal 5.5V regulator.

The actual GATE output voltage tracks approximately two times V_{IN} until V_{IN} exceeds 5.5V or the OVLO trip level is exceeded, whichever comes first. The MAX4838A has a 7.4V typical OVLO; therefore GATE remains relatively constant at approximately 10.5V for $5.5V < V_{IN} < 7.4V$. The MAX4840A has a 5.8V typical OVLO, but this can be as low as 5.5V. The MAX4840A in practice may never actually achieve the full 10.5V GATE output. The MAX4842A has a 4.7V (typ) OVLO, and the GATE output voltage is 2x the input voltage. The GATE output voltage as a function of input voltage is shown in the *Typical Operating Characteristics*.

Device Operation

The MAX4838A/MAX4840A/MAX4842A have an on-board state machine to control device operation. A flowchart is shown in Figure 6. On initial power-up, if $V_{IN} <$ UVLO or if $V_{IN} >$ OVLO, GATE is held at 0V, and $\overline{\text{FLAG}}$ is low.

If UVLO $< V_{IN} <$ OVLO and $\overline{\text{EN}}$ is low, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATE begins to be driven above V_{IN} by the internal charge pump. $\overline{\text{FLAG}}$ is held low during startup until the $\overline{\text{FLAG}}$ blanking period expires, typically 50ms after the GATE starts going high. At this point the device is in its on state.

At any time if V_{IN} drops below UVLO, $\overline{\text{FLAG}}$ is driven low and GATE is driven to ground.

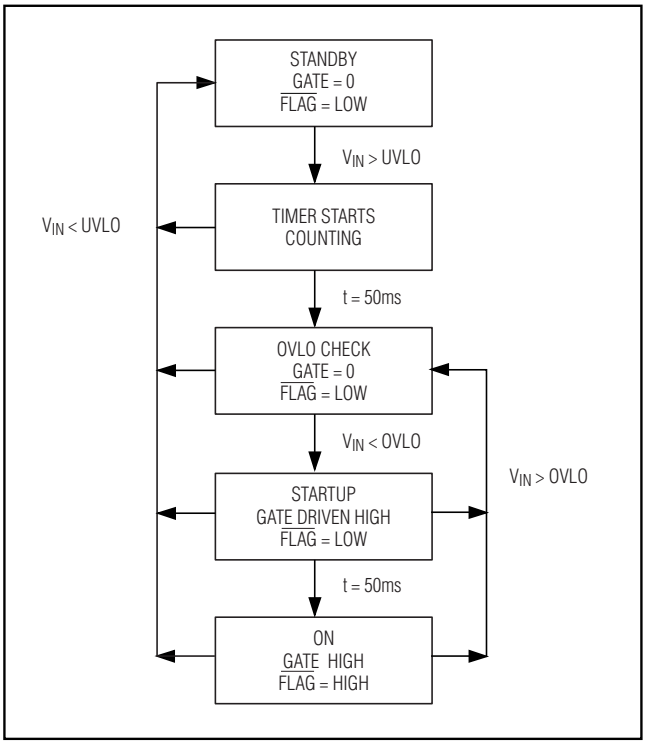


Figure 6. State Diagram

Applications Information

MOSFET Configuration

The MAX4838A/MAX4840A/MAX4842A can be used with either a single MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a back-to-back MOSFET as shown in Figure 7. The back-to-back configuration has almost zero reverse current when the input supply is below the output.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types, and is a lower cost solution. Note that if the input is actually pulled low, the output is pulled low as well due to the parasitic body diode in the MOSFET. If this is a concern, then the back-to-back configuration should be used.

MOSFET Selection

The MAX4838A/MAX4840A/MAX4842A are designed for use with either a single n-channel MOSFET or dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with $R_{DS(ON)}$ specified for a V_{GS} of 4.5V work well. If the input supply is near the UVLO maximum of 3.5V, consider using a MOSFET specified for a lower V_{GS} voltage. Also, the V_{DS} should be 30V for the MOSFET to withstand the full 28V IN range of all devices. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4838A/MAX4840A/MAX4842A.

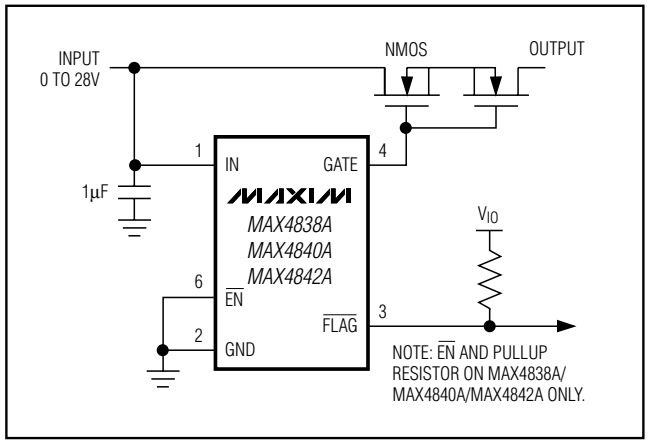


Figure 7. Back-to-Back External MOSFET Configuration

IN Bypass Considerations

For most applications, bypass IN to GND with a 1µF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4838A/MAX4840A/MAX4842A provide protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4838A/MAX4840A/MAX4842A are specified for ±15kV typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Overvoltage-Protection Controllers with Status $\overline{\text{FLAG}}$

Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V_{DS} MAX (V)	R_{ON} AT 4.5V (mΩ)	MANUFACTURER
Si5902DC	Dual/1206-8	30	143	Vishay Silconix www.vishay.com 402-563-6866
Si1426DH	Single/SC70-6	30	115	
FDC6305N	Dual/SSOT-6	20	80	Fairchild Semiconductor www.fairchildsemi.com 207-775-8100
FDC6561AN	Dual/ SSOT-6	30	145	
FDG315N	Single/SC70-6	30	160	

IEC 61000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 61000-4-2 specification. The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4838A/MAX4840A/MAX4842A help users design equipment that meets Level 3 of IEC 61000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±8kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

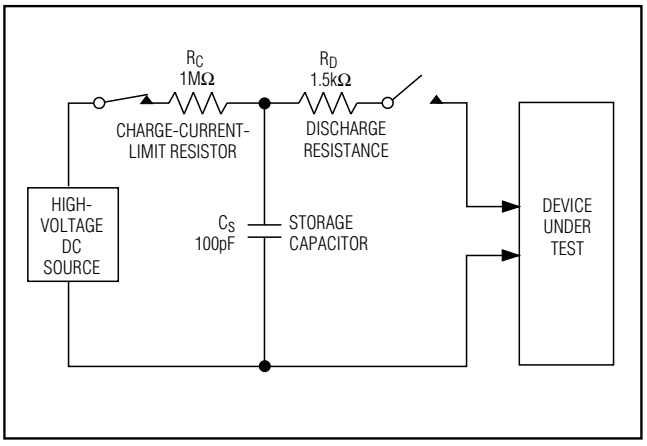


Figure 8. Human Body ESD Test Model

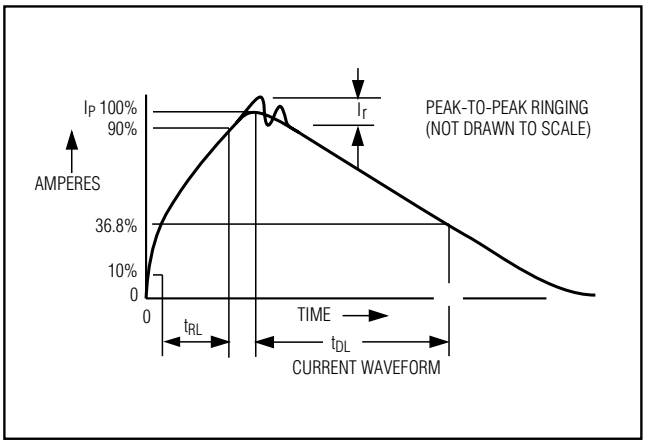


Figure 9. Human Body Model Current Waveform

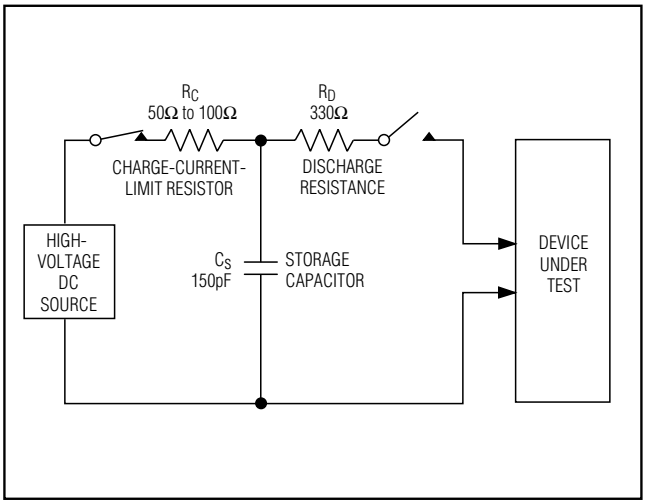


Figure 10. IEC 61000-4-2 ESD Test Model

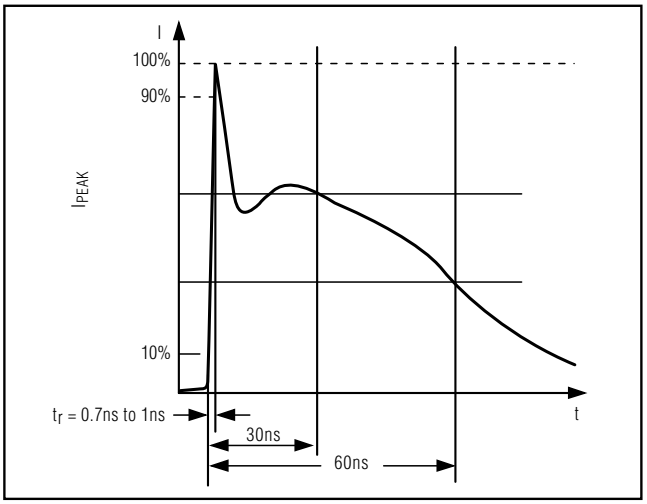
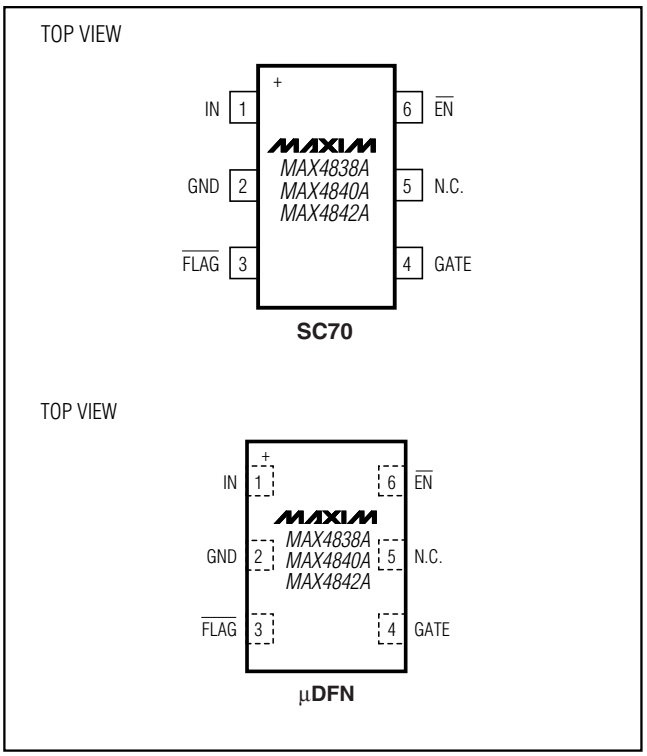


Figure 11. IEC 61000-4-2 ESD Generator Current

Pin Configurations



Chip Information

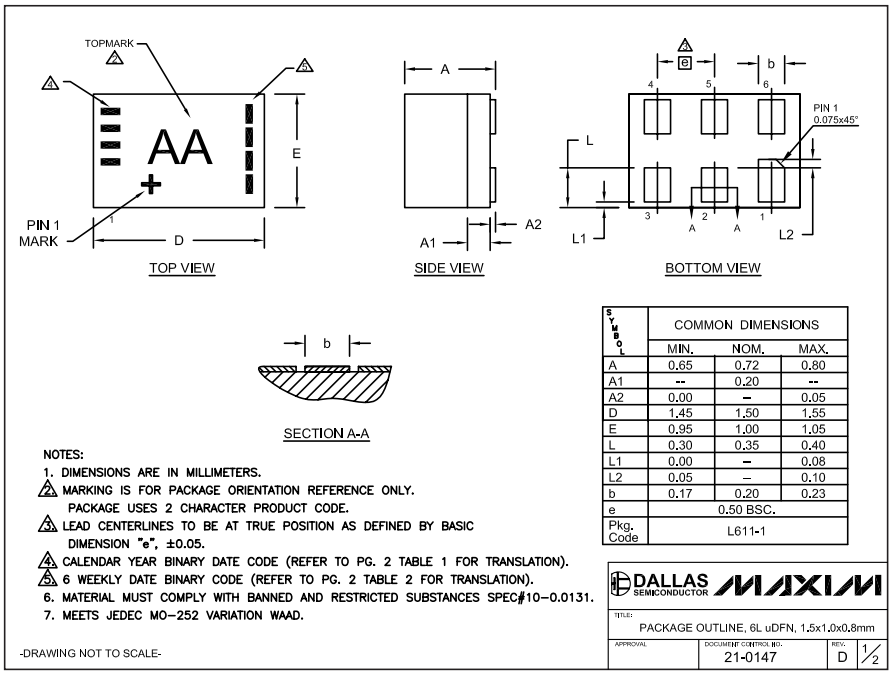
PROCESS: BiCMOS

Overvoltage-Protection Controllers with Status FLAG

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6L UDFN.EPS



SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.65	0.72	0.80
A1	--	0.20	--
A2	0.00	--	0.05
D	1.45	1.50	1.55
E	0.95	1.00	1.05
L	0.30	0.35	0.40
L1	0.00	--	0.08
L2	0.05	--	0.10
b	0.17	0.20	0.23
e	0.50 BSC.		
Pkg. Code	L611-1		

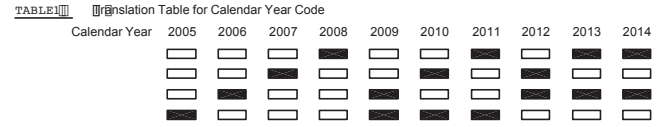
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY. PACKAGE USES 2 CHARACTER PRODUCT CODE.
3. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
4. CALENDAR YEAR BINARY DATE CODE (REFER TO PG. 2 TABLE 1 FOR TRANSLATION).
5. 6 WEEKLY DATE BINARY CODE (REFER TO PG. 2 TABLE 2 FOR TRANSLATION).
6. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC#10-0.0131.
7. MEETS JEDEC MO-252 VARIATION WAAD.

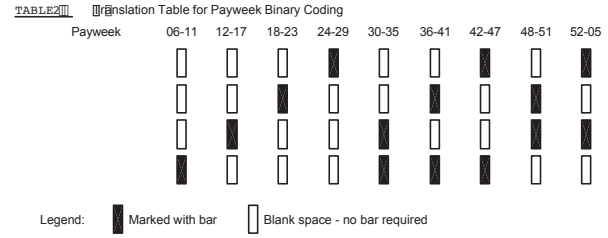
-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L uDFN, 1.5x1.0x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0147 | REV. D | 1/2





-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

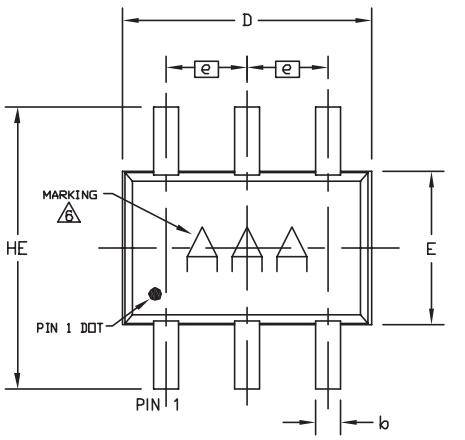
TITLE: PACKAGE OUTLINE, 6L uDFN, 1.5x1.0x0.8mm

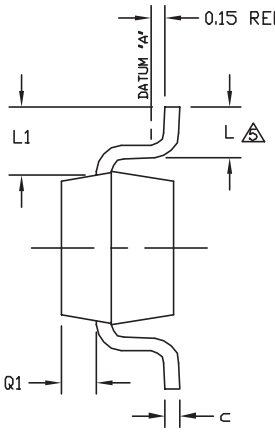
APPROVAL | DOCUMENT CONTROL NO. 21-0147 | REV. D | 2/2

Package Information (continued)

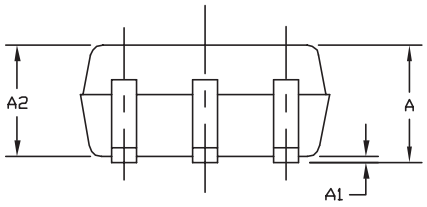
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 6L.EPS





COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.30
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.41
L1	0.425 TYP.	
Q1	0.10	0.40



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0077	C	1/1

-DRAWING NOT TO SCALE-