



4-Pin μ P Voltage Monitors with Manual Reset Input

MAX811/MAX812

General Description

The MAX811/MAX812 are low-power microprocessor (μ P) supervisory circuits used to monitor power supplies in μ P and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits. The MAX811/MAX812 also provide a debounced manual reset input.

These devices perform a single function: They assert a reset signal whenever the V_{CC} supply voltage falls below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the MAX811 has an active-low RESET output (which is guaranteed to be in the correct state for V_{CC} down to 1V), while the MAX812 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC} . Reset thresholds are available for operation with a variety of supply voltages.

Low supply current makes the MAX811/MAX812 ideal for use in portable equipment. The devices come in a 4-pin SOT143 package.

Applications

Computers
Controllers
Intelligent Instruments
Critical μ P and μ C Power Monitoring
Portable/Battery-Powered Equipment

Features

- ◆ Precision Monitoring of 3V, 3.3V, and 5V Power-Supply Voltages
- ◆ 6 μ A Supply Current
- ◆ 140ms Min Power-On Reset Pulse Width; RESET Output (MAX811), RESET Output (MAX812)
- ◆ Guaranteed Over Temperature
- ◆ Guaranteed RESET Valid to $V_{CC} = 1V$ (MAX811)
- ◆ Power-Supply Transient Immunity
- ◆ No External Components
- ◆ 4-Pin SOT143 Package

Ordering Information

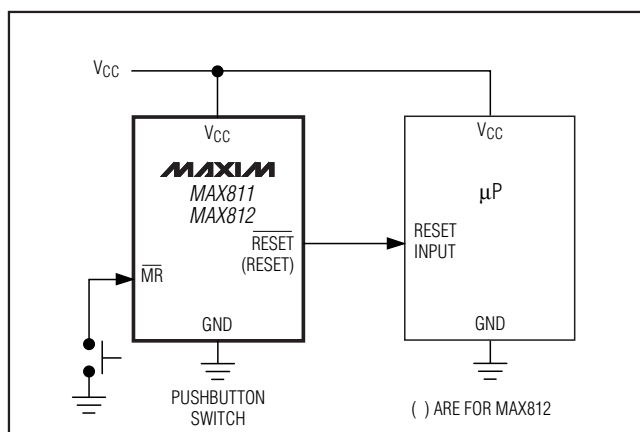
PART*	TEMP RANGE	PIN-PACKAGE
MAX811_EUS-T	-40°C to +85°C	4 SOT143
MAX812_EUS-T	-40°C to +85°C	4 SOT143

*This part offers a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage, and insert it into the blank to complete the part number.

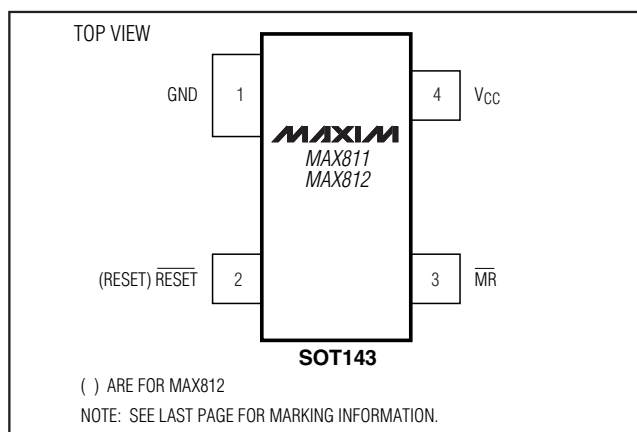
Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

RESET THRESHOLD	
SUFFIX	VOLTAGE (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

Typical Operating Circuit



Pin Configuration



4-Pin μ P Voltage Monitors with Manual Reset Input

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

VCC-0.3V to 6.0V

All Other Inputs.....-0.3V to (VCC + 0.3V)

Input Current, VCC, $\overline{\text{MR}}$ 20mA

Output Current, RESET or $\overline{\text{RESET}}$ 20mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

SOT143 (derate 4mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 320mW

Operating Temperature Range-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$

Storage Temperature Range-65 $^\circ\text{C}$ to +160 $^\circ\text{C}$

Lead Temperature (soldering, 10sec).....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = 5V for L/M versions, VCC = 3.3V for T/S versions, VCC = 3V for R version, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted.

Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	VCC	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	1.0		5.5	V
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.2			
Supply Current	ICC	MAX81_L/M, VCC = 5.5V, IOUT = 0		6	15	μA
		MAX81_R/S/T, VCC = 3.6V, IOUT = 0		2.7	10	
Reset Threshold	VTH	MAX81_L	$T_A = +25^\circ\text{C}$	4.54	4.63	V
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.50		
		MAX81_M	$T_A = +25^\circ\text{C}$	4.30	4.38	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.25		
		MAX81_T	$T_A = +25^\circ\text{C}$	3.03	3.08	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.00		
		MAX81_S	$T_A = +25^\circ\text{C}$	2.88	2.93	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2.85		
		MAX81_R	$T_A = +25^\circ\text{C}$	2.58	2.63	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2.55		
Reset Threshold Tempco				30		ppm/ $^\circ\text{C}$
VCC to Reset Delay (Note 2)		VOD = 125mV, MAX81_L/M		40		μs
		VOD = 125mV, MAX81_R/S/T		20		
Reset Active Timeout Period	tRP	VCC = VTH(MAX)	140		560	ms
$\overline{\text{MR}}$ Minimum Pulse Width	tMR		10			μs
$\overline{\text{MR}}$ Glitch Immunity (Note 3)				100		ns
$\overline{\text{MR}}$ to Reset Propagation Delay (Note 2)	tMD			0.5		μs
$\overline{\text{MR}}$ Input Threshold	VIH	VCC > VTH(MAX), MAX81_L/M	2.3			V
	VIL			0.8		
	VIH	VCC > VTH(MAX), MAX81_R/S/T	0.7 x VCC			
	VIL			0.25 x VCC		
$\overline{\text{MR}}$ Pull-Up Resistance			10	20	30	k Ω
RESET Output Voltage (MAX812)	VOH	ISOURCE = 150 μA , 1.8V < VCC < VTH(MIN)	0.8VCC			V
	VOL	MAX812R/S/T only, ISINK = 1.2mA, VCC = VTH(MAX)		0.3		
		MAX812L/M only, ISINK = 3.2mA, VCC = VTH(MAX)		0.4		

4-Pin μ P Voltage Monitors with Manual Reset Input

MAX811/MAX812

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V for L/M versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{RESET}}$ Output Voltage (MAX811)	V_{OL}	MAX811R/S/T only, $I_{SINK} = 1.2\text{mA}$, $V_{CC} = V_{TH(MIN)}$			0.3	V
		MAX811L/M only, $I_{SINK} = 3.2\text{mA}$, $V_{CC} = V_{TH(MIN)}$			0.4	
		$I_{SINK} = 50\mu\text{A}$, $V_{CC} > 1.0\text{V}$			0.3	
	V_{OH}	MAX811R/S/T only, $I_{SOURCE} = 500\mu\text{A}$, $V_{CC} > V_{TH(MAX)}$	$0.8V_{CC}$			
		MAX811L/M only, $I_{SOURCE} = 800\mu\text{A}$, $V_{CC} > V_{TH(MAX)}$	$V_{CC} - 1.5$			

Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by design using six sigma design limits.

Note 2: $\overline{\text{RESET}}$ output for MAX811, RESET output for MAX812.

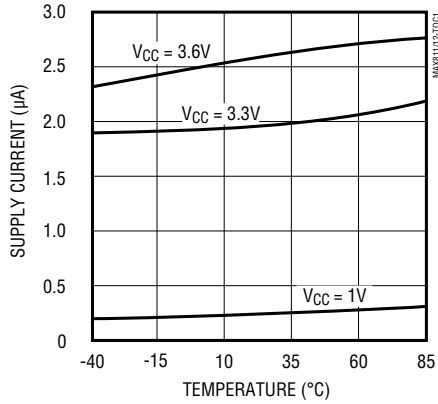
Note 3: "Glitches" of 100ns or less typically will not generate a reset pulse.

4-Pin μ P Voltage Monitors with Manual Reset Input

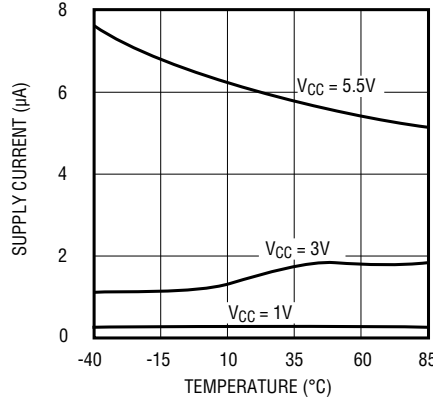
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

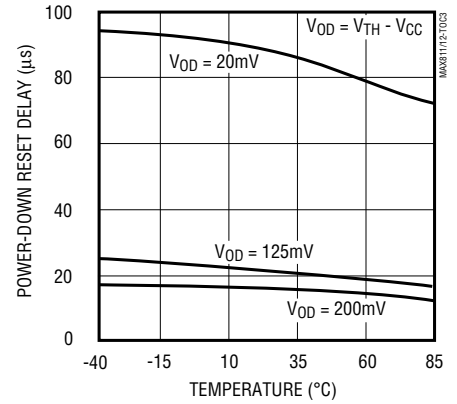
**SUPPLY CURRENT vs. TEMPERATURE
(MAX81_R/S/T)**



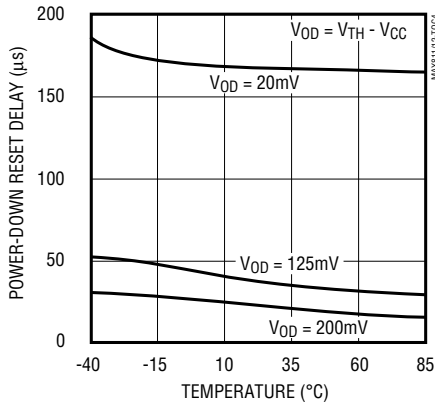
**SUPPLY CURRENT vs. TEMPERATURE
(MAX81_L/M)**



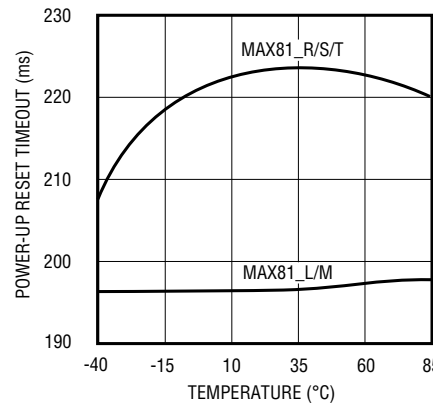
**POWER-DOWN RESET DELAY vs. TEMPERATURE
(MAX81_R/S/T)**



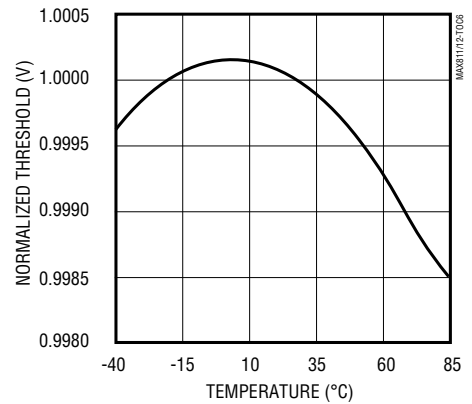
**POWER-DOWN RESET DELAY vs. TEMPERATURE
(MAX81_L/M)**



**POWER-UP RESET TIMEOUT
vs. TEMPERATURE**



**RESET THRESHOLD DEVIATION
vs. TEMPERATURE**



4-Pin μ P Voltage Monitors with Manual Reset Input

Pin Description

PIN		NAME	FUNCTION
MAX811	MAX812		
1	1	GND	Ground
2	—	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. $\overline{\text{RESET}}$ remains low for the Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
—	2	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. RESET remains high for Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
3	3	$\overline{\text{MR}}$	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for 180ms after $\overline{\text{MR}}$ returns high. This active-low input has an internal 20k Ω pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	4	V_{CC}	+5V, +3.3V, or +3V Supply Voltage

MAX811/MAX812

Detailed Description

Reset Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. These μ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for $V_{CC} > 1V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer starts after V_{CC} returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

The manual reset input ($\overline{\text{MR}}$) can also initiate a reset. See the *Manual Reset Input* section.

The MAX812 has an active-high RESET output that is the inverse of the MAX811's $\overline{\text{RESET}}$ output.

Manual Reset Input

Many μ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for the Reset Active Timeout Period (t_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 20k Ω pull-up resistor, so it can be left open if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μ F capacitor from $\overline{\text{MR}}$ to ground provides additional noise immunity.

Reset Threshold Accuracy

The MAX811/MAX812 are ideal for systems using a 5V $\pm 5\%$ or 3V $\pm 5\%$ power supply with ICs specified for 5V $\pm 10\%$ or 3V $\pm 10\%$, respectively. They are designed to meet worst-case specifications over temperature. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range for the system ICs. The thresholds are pre-trimmed and exhibit tight distribution, reducing the range over which an undesirable reset may occur.

4-Pin μ P Voltage Monitors with Manual Reset Input

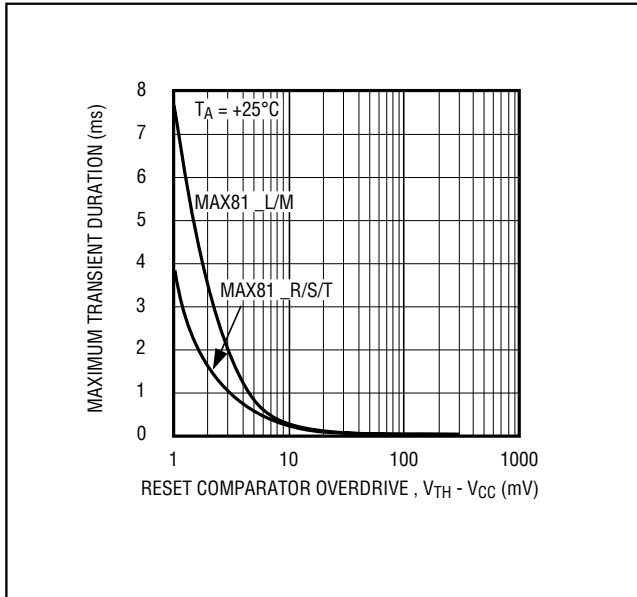


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Comparator Overdrive

Applications Information

Negative-Going VCC Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, the MAX811/MAX812 are relatively immune to short duration negative-going VCC transients (glitches).

Figure 1 shows typical transient durations vs. reset comparator overdrive, for which the MAX811/MAX812 do not generate a reset pulse. This graph was generated using a negative-going pulse applied to VCC, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going VCC transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 125mV below the reset threshold and lasts 40 μ s or less (MAX81_L/M) or 20 μ s or less (MAX81_T/S/R) will not cause a reset pulse to be issued. A 0.1 μ F capacitor mounted as close as possible to VCC provides additional transient immunity.

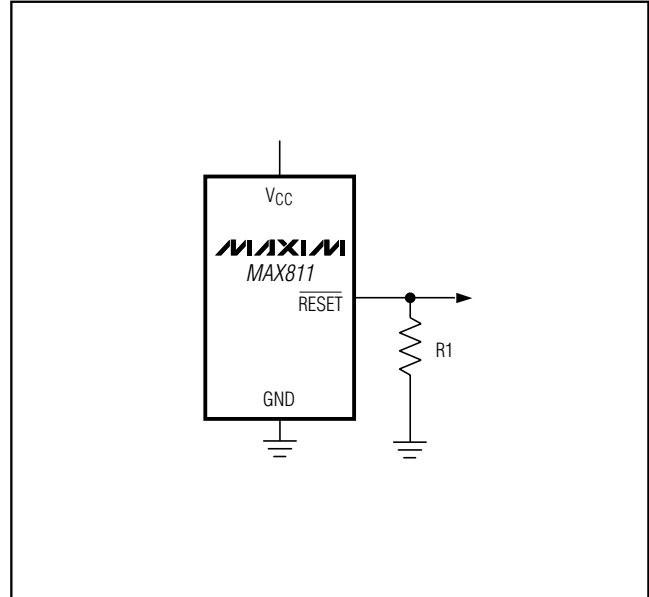


Figure 2. RESET Valid to VCC = Ground Circuit

Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX811 RESET output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to the RESET output can drift to undetermined voltages. This presents no problem in most applications, since most μ P and other circuitry is inoperative with VCC below 1V. However, in applications where the RESET output must be valid down to 0V, adding a pull-down resistor to the RESET pin will cause any stray leakage currents to flow to ground, holding RESET low (Figure 2). R1's value is not critical; 100k Ω is large enough not to load RESET and small enough to pull RESET to ground.

A 100k Ω pull-up resistor to VCC is also recommended for the MAX812 if RESET is required to remain valid for VCC < 1V.

4-Pin μ P Voltage Monitors with Manual Reset Input

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX811/MAX812 reset outputs. If, for example, the MAX811 $\overline{\text{RESET}}$ output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a 4.7k Ω resistor between the MAX811 $\overline{\text{RESET}}$ (or MAX812 $\overline{\text{RESET}}$) output and the μ P reset I/O (Figure 3). Buffer the reset output to other system components.

Chip Information

TRANSISTOR COUNT: 341

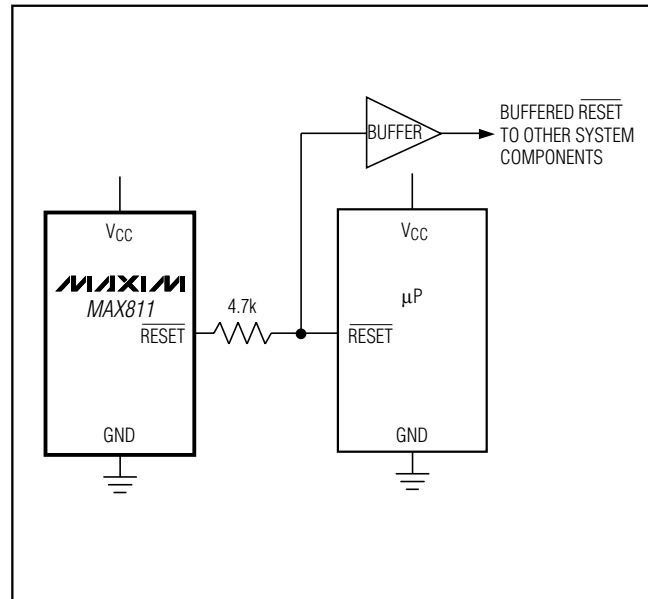


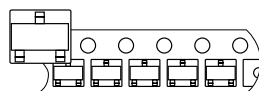
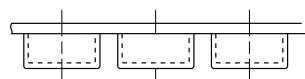
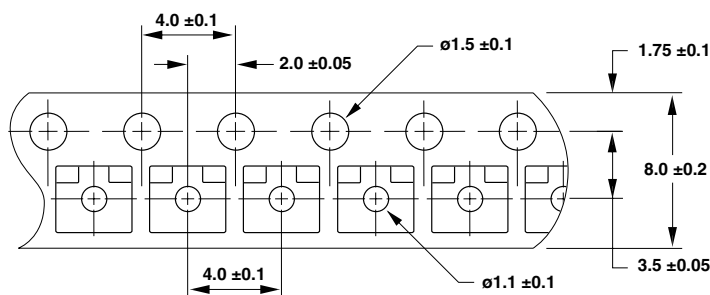
Figure 3. Interfacing to μ Ps with Bidirectional Reset I/O

MAX811/MAX812

4-Pin μ P Voltage Monitors with Manual Reset Input

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

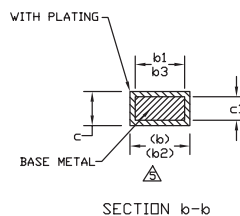
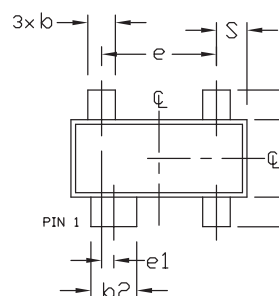
† ICs MAY ALSO BE MARKED WITH FULL PART NAME: 811L, 811M...

MARKING INFORMATION†

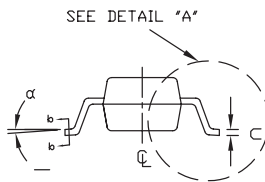
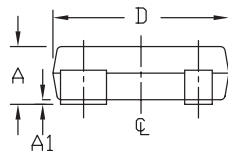
LOT SPECIFIC
CODE

XX'XX'

AMAA or KABB = MAX811L
ANAA or KABC = MAX811M
APAA or KABD = MAX811T
AQAA or KABE = MAX811S
ARAA or KABF = MAX811R
ASAA or KABG = MAX812L
ATAA or KABH = MAX812M
AVAA or KABI = MAX812T
AWAA or KABJ = MAX812S
AXAA or KABK = MAX812R



SECTION b-b

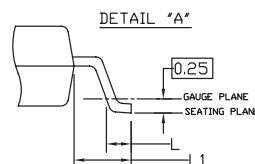


NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC TO253.

THESE DIMENSIONS APPLY TO THE FLAT SECTION OF
THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.048	0.80	1.22
A1	0.000	0.006	0.01	0.15
b	0.014	0.020	0.35	0.50
b1	0.012	0.018	0.30	0.45
b2	0.030	0.035	0.76	0.89
b3	0.012	0.033	0.76	0.84
c	0.003	0.008	0.08	0.20
c1	0.003	0.006	0.08	0.16
D	0.110	0.120	2.80	3.04
E	0.083	0.104	2.10	2.64
E1	0.047	0.055	1.20	1.40
e	0.076	BSC.	1.92	BSC.
e1	0.008	BSC.	0.20	BSC.
L	0.016	0.024	0.40	0.60
L1	0.021	REF.	0.54	REF.
S	0.018	0.024	0.45	0.60
α	0°	8°	0°	8°



 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE			
PACKAGE OUTLINE, SOT-143, 4L			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0052	E	

SOT-143 4LEPS

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