19-2045; Rev. 2; 1/07

MAXIM

25ns, Dual/Quad/Single, Low-Power, TTL Comparators

General Description

The MAX9107/MAX9108/MAX9109 dual/quad/single, high-speed, low-power voltage comparators are designed for use in systems powered from a single +5V supply. Their 25ns propagation delay (with 10mV input overdrive) is achieved with a power consumption of only 1.75mW per comparator. The wide input common-mode range extends from 200mV below ground to within 1.5V of the positive supply rail.

The MAX9107/MAX9108/MAX9109 outputs are TTL-compatible, requiring no external pullup circuitry. These easy-to-use comparators incorporate internal hysteresis to ensure clean output switching even when the devices are driven by a slow-moving input signal.

The MAX9107/MAX9108/MAX9109 are higher-speed, lower-power, lower-cost upgrades to industry-standard comparators MAX907/MAX908/MAX909. The MAX9109 features an output latch but does not have complementary outputs.

The dual MAX9107 is available in both 8-pin SO and SOT23 packages. The quad MAX9108 is available in 14-pin TSSOP and SO packages while the single MAX9109 is available in an ultra-small 6-pin SC70 package, a space-saving 6-pin SOT23 package and an 8-pin SO package.

Applications

Battery-Powered Systems

A/D Converters

Line Receivers

Threshold Detectors/ Discriminators

Sampling Circuits

Zero-Crossing Detectors

Features

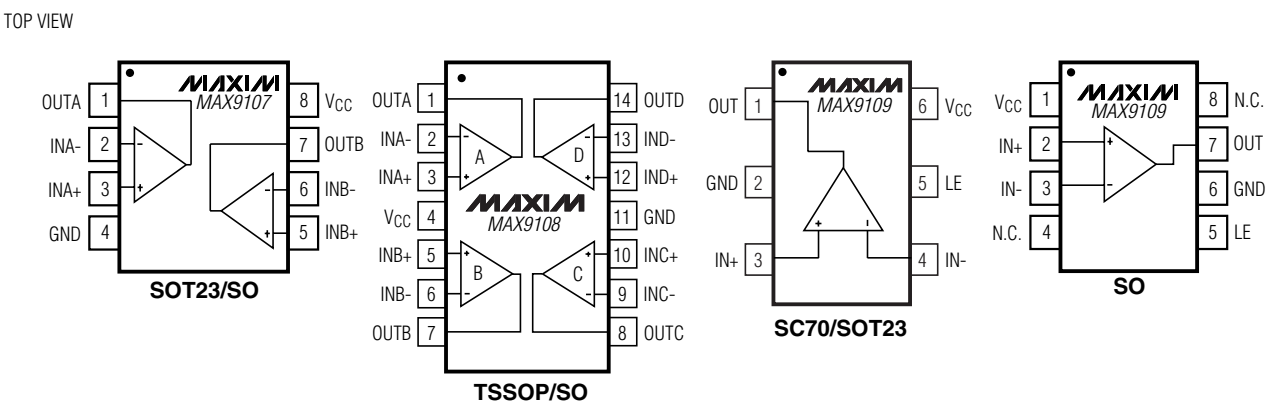
- **25ns Propagation Delay**
- **350µA (1.75mW) Supply Current Per Comparator**
- **Single 4.5V to 5.5V Supply Operation**
- **Wide Input Range Includes Ground**
- **Low 500µV Offset Voltage**
- **Internal Hysteresis Provides Clean Switching (2mV)**
- **TTL-Compatible Outputs**
- **Internal Latch (MAX9109 only)**
- **Space-Saving Packages:**
  - **6-Pin SC70 (MAX9109)**
  - **8-Pin SOT23 (MAX9107)**
  - **14-Pin TSSOP (MAX9108)**

Ordering Information

PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX9107EKA-T	8 SOT23-8	AAIB	K8-5
MAX9107ESA	8 SO	—	S8-2
MAX9108EUD	14 TSSOP	—	U14-1
MAX9108ESD	14 SO	—	S14-1
MAX9109EXT-T	6 SC70-6	AAU	X6S-1
MAX9109EUT-T	6 SOT23-6	AARU	U6-1
MAX9109ESA	8 SO	—	S8-2

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

Pin Configurations



25ns, Dual/Quad/Single, Low-Power, TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage (V_{CC} to GND).....6V
- Differential Input Voltage.....-0.3V to (V_{CC} + 0.3V)
- Common-Mode Input Voltage to GND...-0.3V to (V_{CC} + 0.3V)
- Latch-Enable Input Voltage (MAX9109 only).....-0.3V to (V_{CC} + 0.3V)

Current into Input Pins.....±20mA
Output Short-Circuit Duration to V_{CC} or GND 10s
Continuous Power Dissipation (T_A = +70°C)
- 6-Pin SC70 (derate 3.1mW/°C above +70°C).....245mW
- 6-Pin SOT23 (derate 8.7mW/°C above +70°C)696mW 8-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
- 8-Pin SO (derate 5.9mW/°C above +70°C).....470mW
- 14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
- 14-Pin SO (derate 8.33mW/°C above +70°C).....666mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{CM} = 0, V_{LE} = 0 (MAX9109 only), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	Guaranteed by PSRR		4.5		5.5	V
Input Offset Voltage	V_{OS}	(Note 2)	T_A = +25°C		0.5	1.6	mV
			T_A = T_{MIN} to T_{MAX}			4.0	
Input Hysteresis	V_{HYST}	(Note 3)			2		mV
Input Bias Current	I_B				125	350	nA
Input Offset Current	I_{OS}				25	80	nA
Input Voltage Range	V_{CMR}	(Note 4)		-0.2		V_{CC} - 1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5.5V (Note 5)			50	1000	µV/V
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{CC} ≤ 5.5V			50	1000	µV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 100µA		3.0	3.5		V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA			0.35	0.6	V
		I_{SINK} = 8mA			0.4		
Supply Current Per Comparator	I_{CC}	V_{CC} = +5.5V, all outputs low			0.35	0.7	mA
Output Rise Time	t_r	V_{OUT} = 0.4V to 2.4V, C_L = 10pF			12		ns
Output Fall Time	t_f	V_{OUT} = 2.4V to 0.4V, C_L = 10pF			6		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{CM} = 0, V_{LE} = 0 (MAX9109 only), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay	t_{PD+}, t_{PD-}	V_{IN} = 100mV, V_{OD} = 10mV		25		ns
Differential Propagation Delay	Δt_{PD}	V_{IN} = 100mV, V_{OD} = 10mV (Note 6)		1		ns
Propagation Delay Skew	t_{PD}skew	V_{IN} = 100mV, V_{OD} = 10mV (Note 7)		5		ns
Latch Input Voltage High	V_{IH}	(Note 8)	2.0			V
Latch Input Voltage Low	V_{IL}	(Note 8)			0.8	V
Latch Input Current	I_{IH}, I_{IL}	(Note 8)		0.4	1	µA
Latch Setup Time	t_s	(Note 8)		2		ns
Latch Hold Time	t_h	(Note 8)		2		ns

Note 1: Devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

Note 2: Input Offset Voltage is defined as the center of the input-referred hysteresis zone. Specified for V_{CM} = 0. See Figure 1.

Note 3: Trip Point is defined as the input voltage required to make the comparator output change state. The difference between upper (V_{TRIP}+) and lower (V_{TRIP}-) trip points is equal to the width of the input-referred hysteresis zone (V_{HYST}). Specified for an input common-mode voltage (V_{CM}) of 0. See Figure 1.

Note 4: Inferred from the CMRR test. Note that a correct logic result is obtained at the output, provided that at least one input is within the V_{CMR} limits. Note also that either or both inputs can be driven to the upper or lower absolute maximum limit without damage to the part.

Note 5: Tested over the full-input voltage range (V_{CMR}).

Note 6: Differential Propagation Delay is specified as the difference between any two channels in the MAX9107/MAX9108 (both outputs making either a low-to-high or a high-to-low transition).

Note 7: Propagation Delay Skew is specified as the difference between any single channel's output low-to-high transition (t_{PD}+) and high-to-low transition (t_{PD}-).

Note 8: Latch specifications apply to MAX9109 only. See Figure 2.

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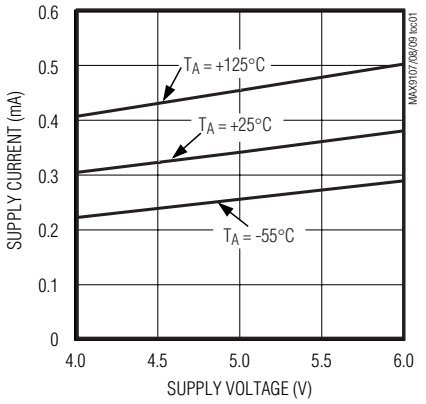
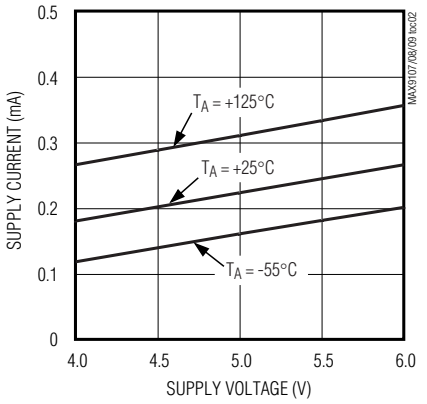
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

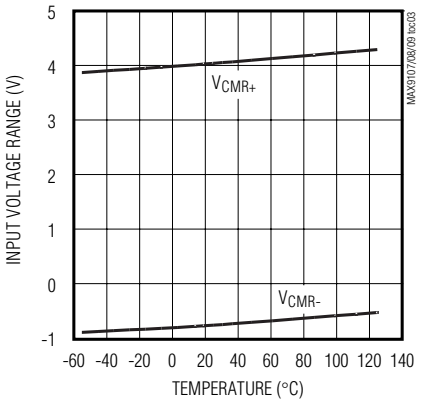
SUPPLY CURRENT vs. SUPPLY VOLTAGE (OUTPUTS AT V_{OL})



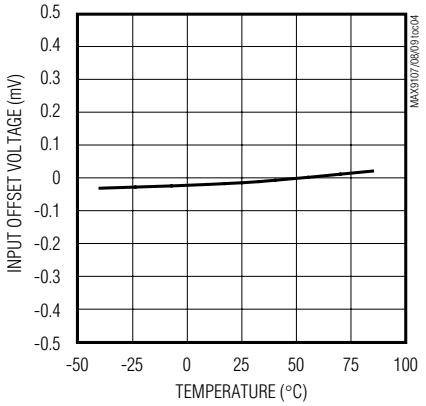
SUPPLY CURRENT vs. SUPPLY VOLTAGE (OUTPUTS AT V_{OH})



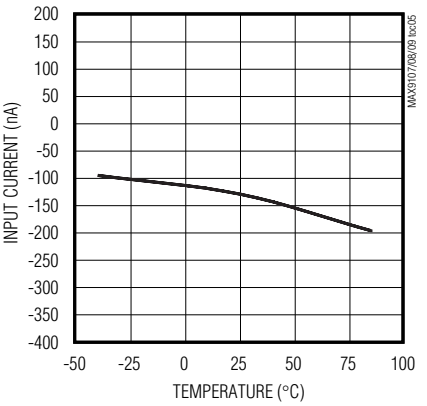
INPUT VOLTAGE RANGE vs. TEMPERATURE



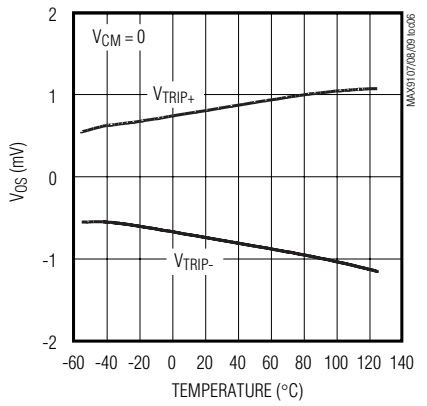
INPUT OFFSET VOLTAGE vs. TEMPERATURE



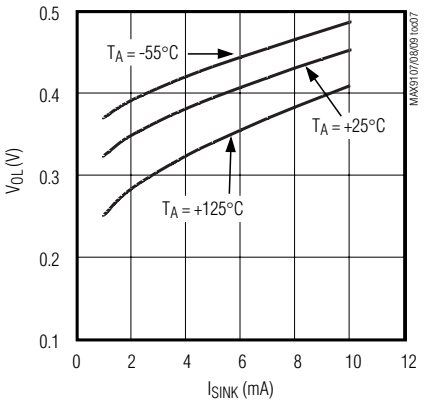
INPUT BIAS CURRENT vs. TEMPERATURE



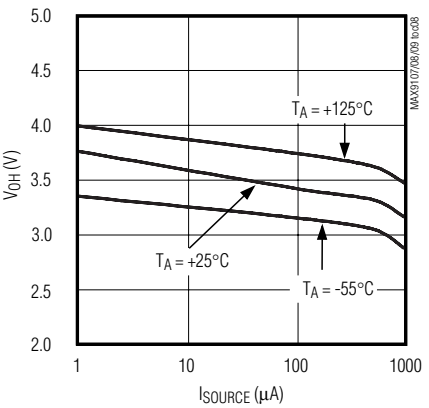
TRIP POINT vs. TEMPERATURE



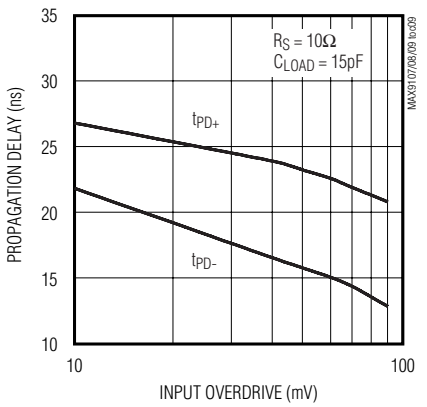
OUTPUT LOW VOLTAGE vs. SINK CURRENT



OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



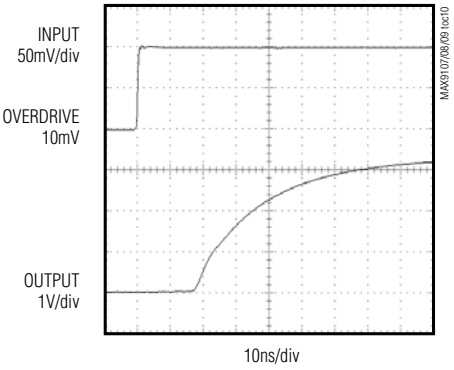
PROPAGATION DELAY vs. INPUT OVERDRIVE



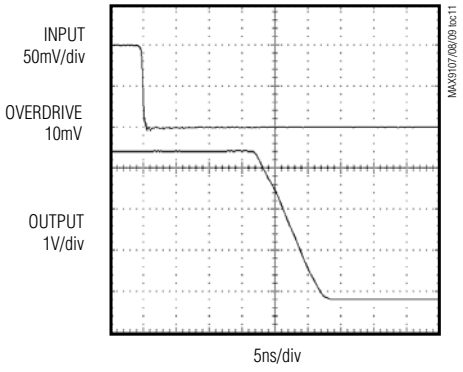
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

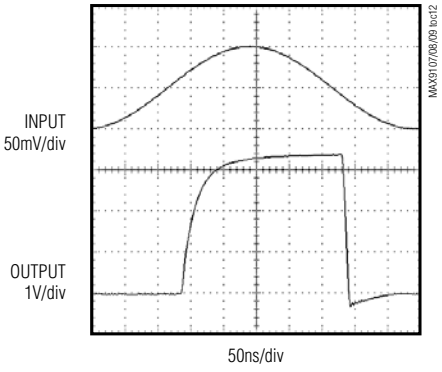
PROPAGATION DELAY (t_{PD+})



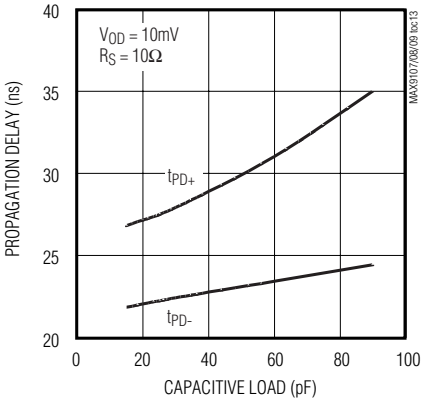
PROPAGATION DELAY (t_{PD-})



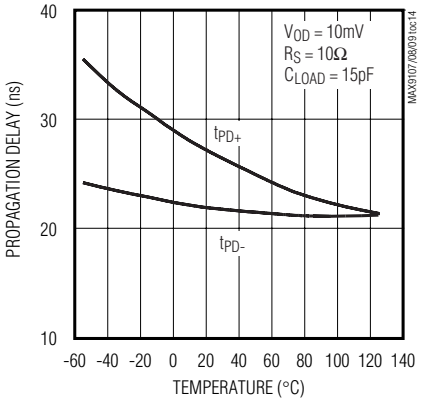
SINUSOID 2MHz RESPONSE



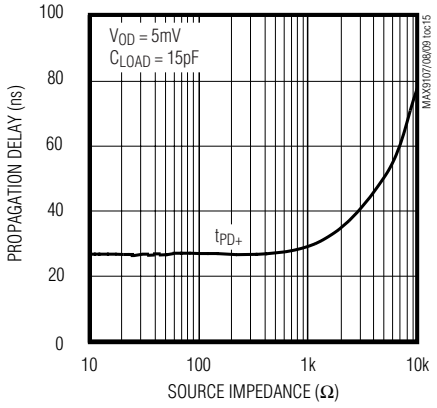
PROPAGATION DELAY vs. CAPACITIVE LOAD



PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. SOURCE IMPEDANCE



Pin Description

PIN				NAME	FUNCTION
MAX9107	MAX9108	MAX9109			
		SC70/SOT23	SO		
1	1	—	—	OUTA	Channel A Output
2	2	—	—	INA-	Channel A Inverting Input
3	3	—	—	INA+	Channel A Noninverting Input
7	7	—	—	OUTB	Channel B Output
6	6	—	—	INB-	Channel B Inverting Input
5	5	—	—	INB+	Channel B Noninverting Input
—	8	—	—	OUTC	Channel C Output
—	9	—	—	INC-	Channel C Inverting Input
—	10	—	—	INC+	Channel C Noninverting Input
—	14	—	—	OUTD	Channel D Output
—	13	—	—	IND-	Channel D Inverting Input
—	12	—	—	IND+	Channel D Noninverting Input
—	—	1	7	OUT	Output
—	—	3	2	IN+	Noninverting Input
—	—	4	3	IN-	Inverting Input
8	4	6	1	V_{CC}	Positive Supply
4	11	2	6	GND	Ground
—	—	5	5	LE	Latch Enable. The latch is transparent when LE is low.
—	—	—	4, 8	N.C.	No Connection. Not internally connected.

Detailed Description

Timing

Noise or undesired parasitic AC feedback cause most high-speed comparators to oscillate in the linear region (i.e., when the voltage on one input is at or near the voltage on the other input). The MAX9107/MAX9108/MAX9109 eliminate this problem by incorporating an internal hysteresis of 2mV. When the two comparator input voltages are equal, hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require that hysteresis be added through the use of external resistors. The MAX9107/MAX9108/MAX9109's fixed internal hysteresis eliminates these resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the noninverting input.

Adding hysteresis to a comparator creates two trip points: one for the input voltage rising and one for the input voltage falling (Figure 1). The difference between these two input-referred trip points is the hysteresis. The average of the trip points is the offset voltage.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX9109 includes an internal latch, allowing the result of a comparison to be stored. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The state of the comparator output is latched when LE is high (Figure 2).

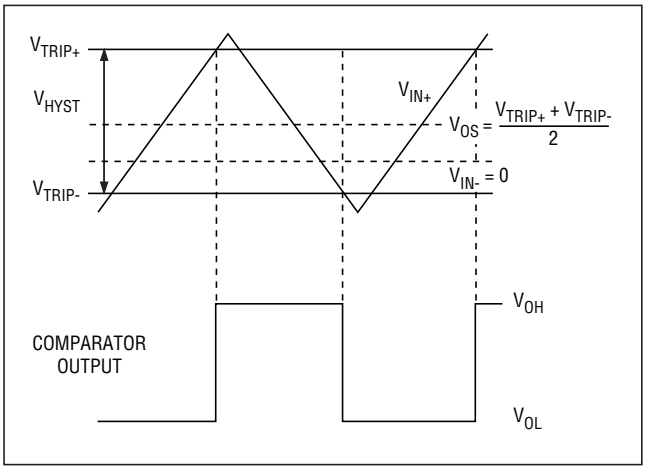


Figure 1. Input and Output Waveforms, Noninverting Input Varied

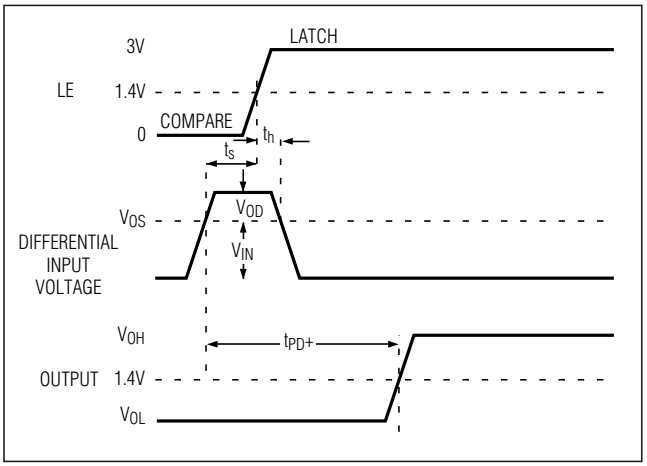


Figure 2. MAX9109 Timing Diagram

Applications Information

Circuit Layout

Because of the MAX9107/MAX9108/MAX9109's high gain bandwidth, special precautions must be taken to realize the full high-speed capability. A printed circuit board with a good, low-inductance ground plane is mandatory. Place the decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V_{CC} as possible. Pay close attention to the decoupling capacitor's bandwidth, keeping leads short. Short lead lengths on the inputs and outputs are also essential to avoid unwanted parasitic feedback around the comparators. Solder the device directly to the printed circuit board instead of using a socket.

Overdriving the Inputs

The inputs to the MAX9107/MAX9108/MAX9109 may be driven beyond the voltage limits given in the *Absolute Maximum Ratings*, as long as the current flowing into the device is limited to 25mA. However, if the inputs are overdriven, the output may be inverted. The addition of an external diode prevents this inversion by limiting the input voltage to 200mV to 300mV below ground (see Figure 3).

Battery-Operated Infrared Data Link

In Figure 4, the circuit allows reception of infrared data. The MAX4400 converts the photodiode current to a voltage, and the MAX9109 determines whether the amplifier output is high enough to be called a "1." The current consumption of this circuit is minimal: the MAX4400 and MAX9109 require typically 410µA and 350µA, respectively.

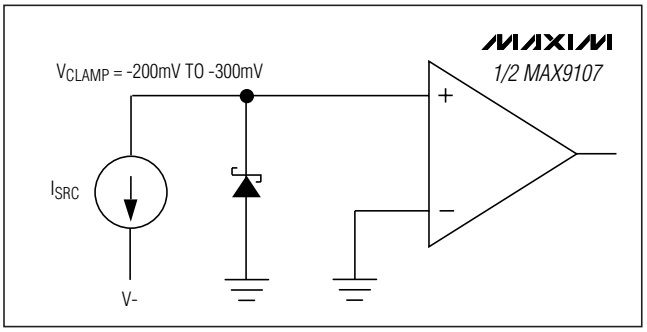


Figure 3. Schottky Clamp for Input Driven Below Ground

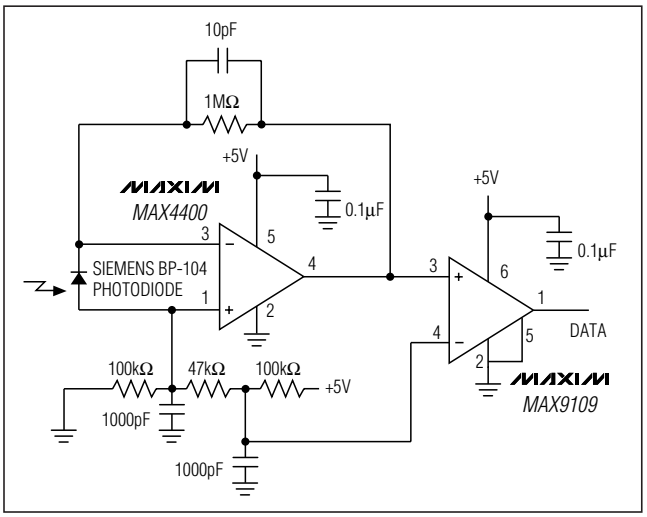


Figure 4. Battery-Operated Infrared Data Link Consumes Only 760µA

25ns, Dual/Quad/Single, Low-Power, TTL Comparators

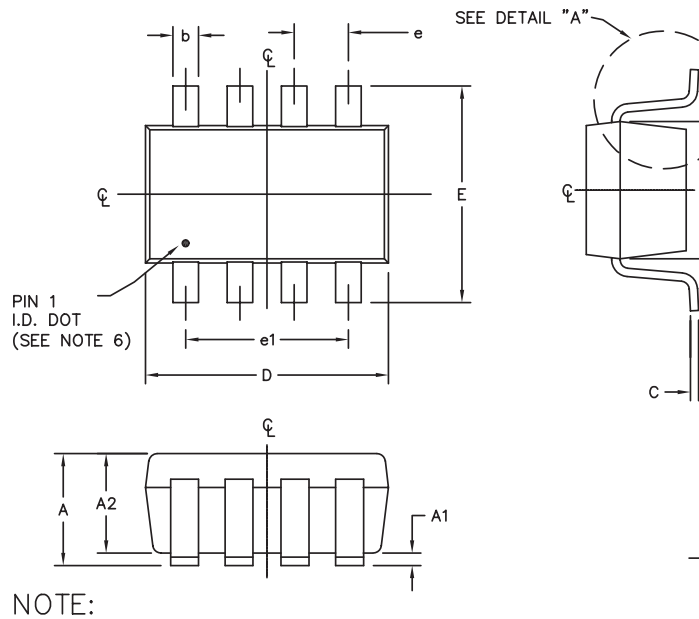
Chip Information

MAX9107 TRANSISTOR COUNT: 262
MAX9108 TRANSISTOR COUNT: 536
MAX9109 TRANSISTOR COUNT: 140
PROCESS: Bipolar

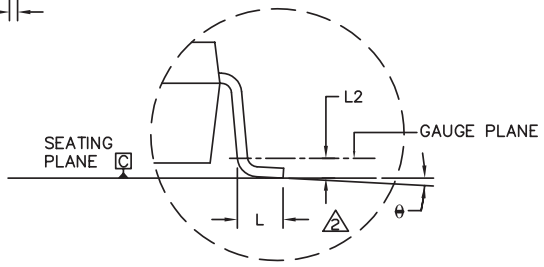
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°
PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6			



DETAIL "A"

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

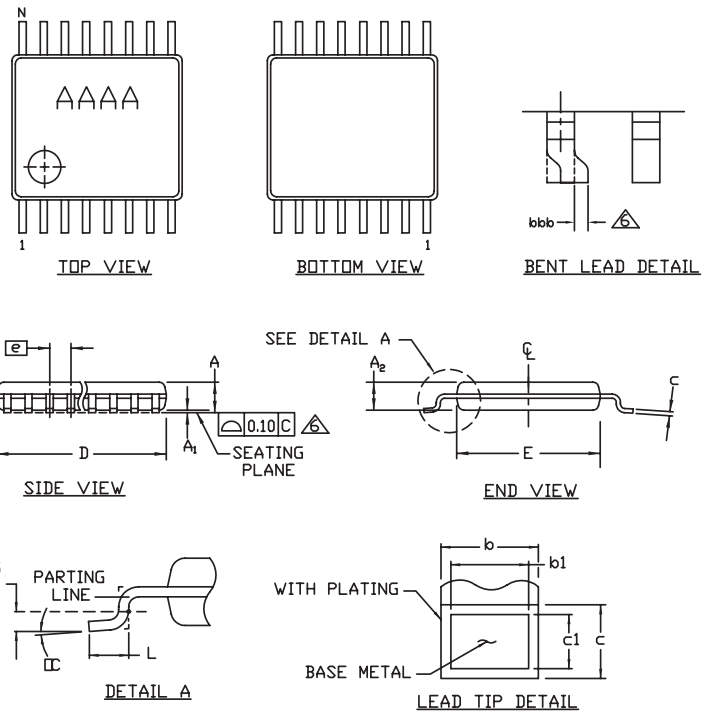
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2; U20-3	6.40	5.10	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

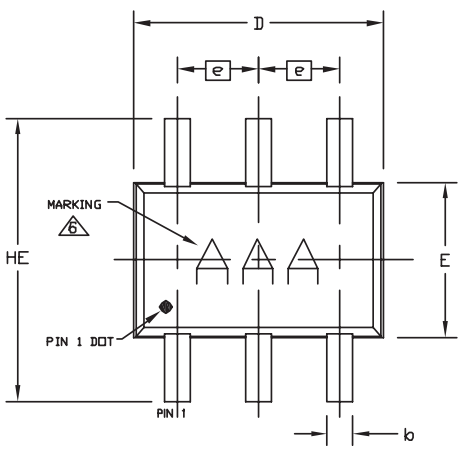
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	H	1/1

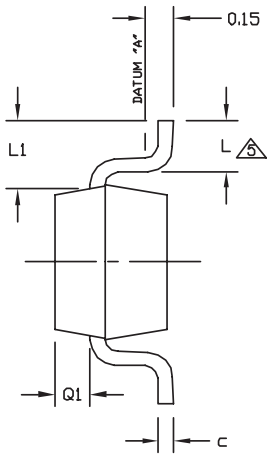
25ns, Dual/Quad/Single, Low-Power, TTL Comparators

Package Information (continued)

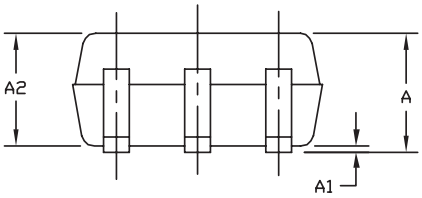
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 6L.EPS





COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X6S-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

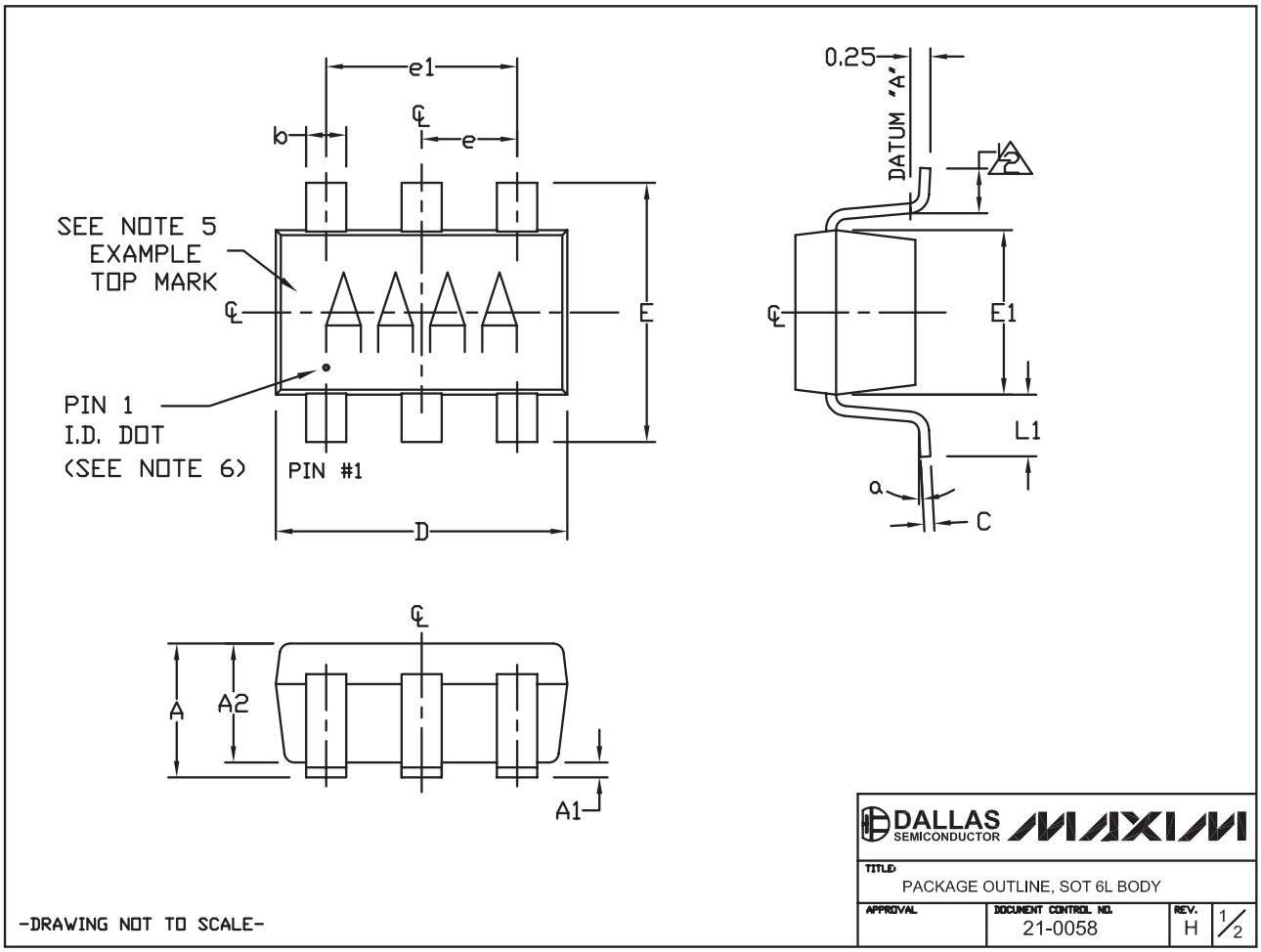
TITLE: PACKAGE OUTLINE, 6L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0077	E	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6LSOT.EPS



25ns, Dual/Quad/Single, Low-Power, TTL Comparators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°
PKG CODES: U6-1, U6-2, U6-4, U6C-8, U6CN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6			

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

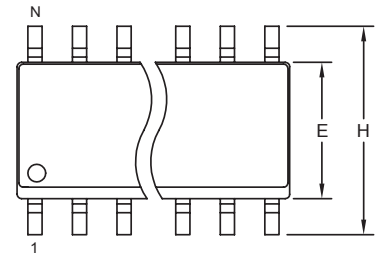
TITLE: PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	H	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

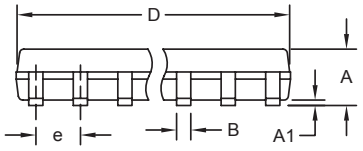


TOP VIEW

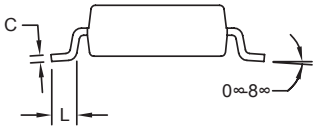
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Revision History

Pages revised at Rev 2: 1, 2, 9–13