TECHNICAL DATA SHEET

6 Lake Street, Lawrence, MA 01841
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Gort Road Business Park, Ennis, Co. Clare, Ireland
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RADIATION HARDENED
NPN LOW POWER SILICON TRANSISTOR
Qualified per MIL-PRF-19500/368

DEVICES

2N3439 **2N3440**
2N3439L **2N3440L**
2N3439UA **2N3440UA**

LEVELS

JANSM – 3K Rads (Si)
JANSD – 10K Rads (Si)
JANSP – 30K Rads (Si)
JANSL – 50K Rads (Si)
JANSR – 100K Rads (Si)

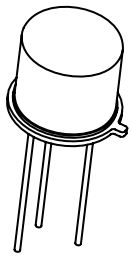
ABSOLUTE MAXIMUM RATINGS ***(T_C = +25°C unless otherwise noted)***

Parameters / Test Conditions	Symbol	2N3439	2N3440	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CBO}	450	300	Vdc
Emitter-Base Voltage	V_{EBO}	7.0		Vdc
Collector Current	I_C	1.0		Adc
Total Power Dissipation @ T_A = +25°C (1) @ T_C = +25°C (2) UA @ T_{SP} = +25°C (3)	P_T	0.8 5.0 2.0		W
Operating & Storage Temperature Range	T_{op} , T_{stg}	-65 to +200		°C

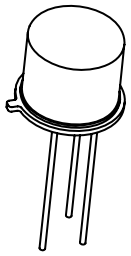
NOTES:
1) Derate linearly @ 4.57mW/°C for T_A > +25°C
2) Derate linearly @ 28.5mW/°C for T_C > +25°C
3) Derate linearly @ 14mW/°C for T_{SP} > +25°C

ELECTRICAL CHARACTERISTICS ***(T_A = +25°C, unless otherwise noted)***

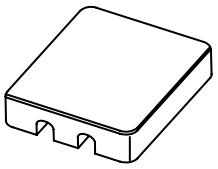
Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERTICS					
Collector-Emitter Breakdown Voltage I_C = 10mAdc R_{BB1} = 470Ω;V_{BB1} = 6V L = 25mH (min); f = 30 – 60Hz	2N3439 / L / UA 2N3440 / L / UA	$V_{(BR)CEO}$	350 250		Vdc
Collector-Emitter Cutoff Current V_{CE} = 300Vdc V_{CE} = 200Vdc	2N3439 / L / UA 2N3440 / L / UA	I_{CEO}		2.0 2.0	µAdc
Emitter-Base Cutoff Current V_{EB} = 7.0Vdc		I_{EBO}		10	µAdc
Collector-Emitter Cutoff Current V_{CE} = 450Vdc, V_{BE} = -1.5Vdc V_{CE} = 300Vdc, V_{BE} = -1.5Vdc	2N3439 / L / UA 2N3440 / L / UA	I_{CEX}		5.0 5.0	µAdc
Collector-Base Cutoff Current V_{CB} = 360Vdc V_{CB} = 250Vdc V_{CB} = 450Vdc V_{CB} = 300Vdc	2N3439 / L / UA 2N3440 / L / UA 2N3439 / L / UA 2N3440 / L / UA	I_{CBO}		2.0 2.0 5.0 5.0	µAdc



TO-5
2N3439L, 2N3440L



TO-39 (TO-205AD)
2N3439, 2N3440



UA
2N3439UA, 2N3440UA

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ELECTRICAL CHARACTERISTICS ***(T_A = +25°C, unless otherwise noted)*** **(CONT.)**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
ON CHARACTERISTICS [3]				
Forward-Current Transfer Ratio I_C = 20mAdc, V_{CE} = 10Vdc I_C = 2.0mAdc, V_{CE} = 10Vdc I_C = 0.2mAdc, V_{CE} = 10Vdc	h_{FE}	40 30 10	160	
Collector-Emitter Saturation Voltage I_C = 50mAdc, I_B = 4.0mAdc	$V_{CE(sat)}$		0.5	Vdc
Base-Emitter Saturation Voltage I_C = 50mAdc, I_B = 4.0mAdc	$V_{BE(sat)}$		1.3	Vdc

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 10mAdc, V_{CE} = 10Vdc, f = 5.0MHz	$\|h_{fe}\|$	3.0	15	
Forward Current Transfer Ratio I_C = 5.0mAdc, V_{CE} = 10V, f = 1.0kHz	h_{fe}	25		
Output Capacitance V_{CB} = 10Vdc, I_E = 0, 100kHz ≤ f ≤ 1.0MHz	C_{obo}		10	pF
Input Capacitance V_{CB} = 5.0Vdc, I_E = 0, 100kHz ≤ f ≤ 1.0MHz	C_{ibo}		75	pF

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time V_{CC} = 200Vdc; I_C = 20mAdc, I_{B1} = 2.0mAdc	t_{on}		1.0	µs
Turn-Off Time V_{CC} = 200Vdc; I_C = 20mAdc, I_{B1} = $-I_{B2}$ = 2.0mAdc	t_{off}		10	µs

SAFE OPERATING AREA

DC Tests
T_C = +25°C, 1 Cycle, t = 1.0s

Test 1
V_{CE} = 5.0Vdc, I_C = 1.0Adc — Both Types

Test 2
V_{CE} = 350Vdc, I_C = 14mAdc — 2N3439 / L / UA

Test 3
V_{CE} = 250Vdc, I_C = 20mAdc — 2N3440 / L / UA

(3) Pulse Test: Pulse Width = 300µs, Duty Cycle ≤ 2.0%

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POST RADIATION ELECTRICAL CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Collector-Emitter Cutoff Current					
V_{CE} = 300Vdc	2N3439 / L / UA	I_{CEO}		4	µAdc
V_{CE} = 200Vdc	2N3440 / L / UA			4	
Emitter-Base Cutoff Current					
V_{EB} = 7.0Vdc		I_{EBO}		20	µAdc
Collector-Emitter Cutoff Current					
V_{CE} = 450Vdc, V_{BE} = -1.5Vdc	2N3439 / L / UA	I_{CEX}		10	µAdc
V_{CE} = 300Vdc, V_{BE} = -1.5Vdc	2N3440 / L / UA			10	
Collector-Base Cutoff Current					
V_{CB} = 360Vdc	2N3439 / L / UA	I_{CBO}		4	µAdc
V_{CB} = 250Vdc	2N3440 / L / UA			4	
V_{CB} = 450Vdc	2N3439 / L / UA			10	
V_{CB} = 300Vdc	2N3440 / L / UA			10	
Forward-Current Transfer Ratio					
I_C = 20mAdc, V_{CE} = 10Vdc		$[h_{FE}]$	[20]	160	
I_C = 2.0mAdc, V_{CE} = 10Vdc			[15]		
I_C = 0.2mAdc, V_{CE} = 10Vdc			[5]		
Collector-Emitter Saturation Voltage					
I_C = 50mAdc, I_B = 4.0mAdc		$V_{CE(sat)}$		0.56	Vdc
Base-Emitter Saturation Voltage					
I_C = 50mAdc, I_B = 4.0mAdc		$V_{BE(sat)}$		1.5	Vdc

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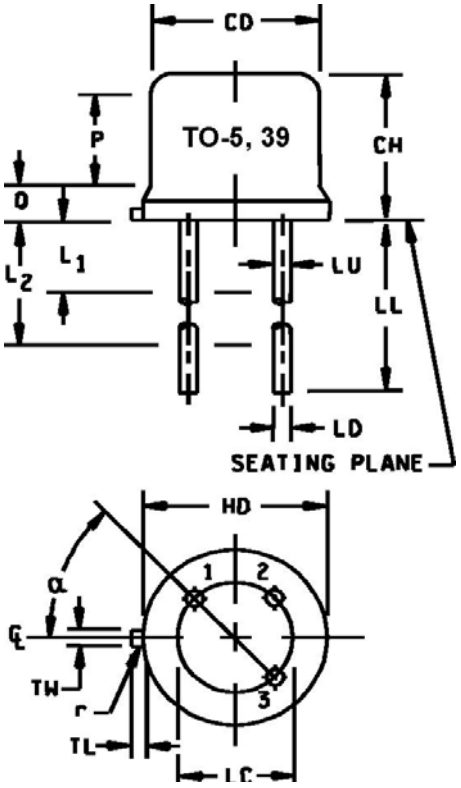
PACKAGE DIMENSIONS



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L1		.050		1.27	8,9
L2	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		7

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
8. Dimension LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For transistor types 2N3439L and 2N3440L (T0-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For transistor types 2N3439 and 2N3440 (T0-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions (similar to TO-5 and TO-39).

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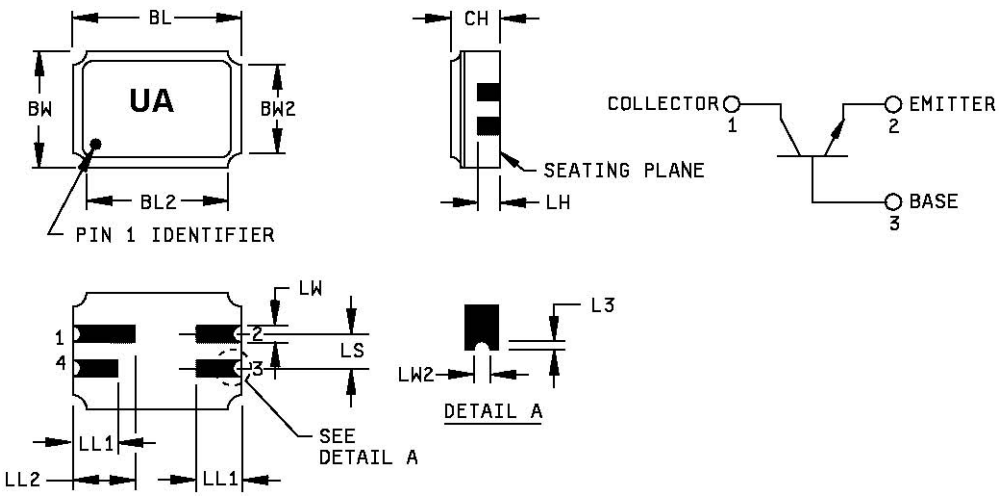

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003	.007	0.08	0.18	5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

FIGURE 2. Physical dimensions, surface mount (2N3439UA, 2N3440UA) version.