MIC23060

Sequenced Power Management IC with HyperLight Load™ DC/DC and Dual Input LDO™

General Description

The MIC23060 is a highly efficient power management IC integrating a high frequency DC/DC converter with HyperLight Load™ mode and a low input voltage capable LDO. The MIC23060 offers two output voltages at very high efficiency on both outputs while maintaining a low total system cost.

The MIC23060 also provides sequencing of the two outputs in every potential combination of turn-on and turn-off sequencing by connecting two pins either high or low, and using a single GPIO to enable and disable the device. The LDO is designed both to post regulate from the output of the DC/DC converter for high system efficiency, and/or power directly from the battery. For sequences where the LDO is enabled prior to the DC/DC output, the LDO is first powered by the input voltage (typically the battery source) and then after the DCDC soft start is complete, seamlessly transition LDO input power to draw from the output of the DC/DC converter for higher efficiency operation through post-regulation.

The DC/DC converter in the MIC23060 is a HyperLight Load™ converter with very high efficiency at light load and at full operating current, maintaining high efficiency across all operating modes in portable electronics.

The MIC23060 is a µCap design, operating with small ceramic output capacitors and tiny inductors for stability, reducing required board space and component cost and is available in the tiny 2.5mm x 2.5mm Thin MLF® package.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Features

- 2.7V to 5.5V supply voltage range
- Tiny 12-pin 2.5mm x 2.5mm Thin MLF® package
- Integrated sequencing
  - Dual Input LDO™ can turn-on prior to DC/DC converter and automatically switch to post regulation from the DC/DC converter after it starts
  - Power for LDO from input during start-up
  - Adjustable delay time between outputs
- Zero-current off mode
- Current-limit and thermal shutdown protection

HyperLight Load™ DC/DC Converter

- Up to 600mA output current in PWM mode (shared between switcher and linear LDO regulator outputs)
- 4MHz frequency in continuous PWM mode
- Tiny 2.2µH inductor, 4.7µF capacitor
- 85% Efficiency at 1mA output current
- >90% peak efficiency
- Low output voltage ripple across all loads

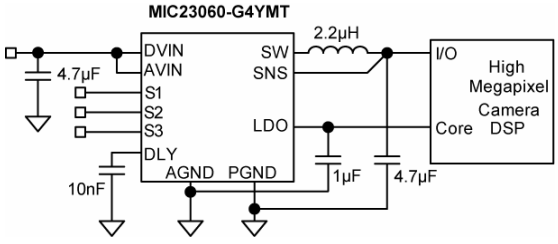
LDO Regulator

- Low Input voltage LDO regulator
- Stable with ceramic output capacitors
- Regulates from the output of the DC/DC converter
- 300mA output current capability
- High Accuracy: ±3% over temperature
- High PSRR: greater than 60dB
- Very low quiescent current: 16µA

Applications

- Mobile phones
- PDAs/pocket PCs
- Digital cameras/DSP power supply

Typical Application



S3	S2	S1	Sequence
X	0	0	ALL OFF
0	0	EN	DC-DC ON 1st / OFF 1st
0	EN	0	LDO ON 1st / OFF 1st
1	0	EN	DC-DC ON 1st / OFF 2nd
1	EN	0	LDO ON 1st / OFF 2nd
X	1	1	ALL ON

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MLF and *Micro*Lead frame are registered trademarks of Amkor Technology Inc.

> 2Mpixel Camera DSP power Supply

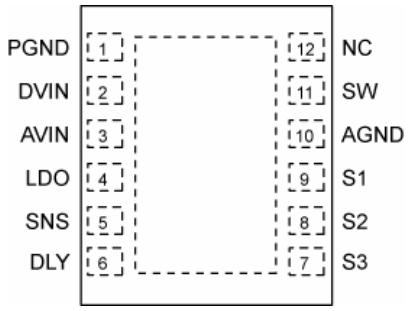
Ordering Information

Part Number	Marking Code	Nominal Output Voltage[1]	Junction Temp. Range	Package[2]
MIC23060-G4YMT	XG4	1.8V/1.2V	–40° to +125°C	12-Pin 2.5mm x 2.5mm Thin MLF®

Note:

1. Refers to output voltage of DC/DC & LDO respectively. Other voltage options available. Contact Micrel for details.
   a. DC/DC Converter Voltage Range: 1.7V to 2.5V
   b. LDO Output Voltage Range: 0.8V to 2.5V
2. Thin MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



12-Pin 2.5mm x 2.5mm Thin MLF® (MT)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND	Power Ground.
2	DVIN	DC/DC Supply Input Voltage.
3	AVIN	Small signal circuitry and Auxiliary LDO Supply Input Voltage.
4	LDO	LDO Regulator Output.
5	SNS	Main LDO input supply and feedback for DC-DC converter. Connect to DC/DC V_{OUT} to sense output voltage.
6	DLY	Delay. Capacitor to AGND sets a delay time between the first regulator reaching 90% of its regulated voltage and enabling the second regulator. Also programs the turn-off delay, setting the time between the disable of each output. The on/off sequence of the regulators is set by pins S1, S2 and S3. Do not ground.
7	S3	SET Input (3). Active High Input. Logic High = On; Logic Low = Off; do not leave floating. See applications information for set pin configurations.
8	S2	SET Input (2). Active High Input. Logic High = On; Logic Low = Off; do not leave floating. See applications information for set pin configurations.
9	S1	SET Input (1). Active High Input. Logic High = On; Logic Low = Off; do not leave floating. See applications information for set pin configurations.
10	AGND	Analog Ground.
11	SW	Switch (Output): Internal power MOSFET output switches.
12	NC	Not Internally connected.
ePAD	ePAD	Not internally connected, connect to ground plane to maximize heat dissipation.

Absolute Maximum Ratings[1]

Supply Voltage (V_{AVIN}, V_{DVIN})..... 0V to 6V
Switch Voltage (V_{SW})..... 0V to 6V
Switch Current (I_{SW}) 2A
Logic Input Voltage ($V_{S1/2/3}$)..... 0V to V_{IN}+0.3V
Lead Temperature (soldering, 10sec.).....260°C
Storage Temperature (Ts).....-65°C to +150°C
ESD Rating[4].....ESD Sensitive

Operating Ratings[2]

Supply Voltage (V_{AVIN}, V_{DVIN})..... +2.7V to +5.5V
Output Voltage (V_{LDO})..... 0V to 5.5V
Logic Input Voltage ($V_{S1/2/3}$)..... 0V to V_{IN}
Ambient Temperature (T_J)[3].....–40°C to +125°C
Thermal Resistance
2.5mmx2.5mm Thin MLF-12L (θ_{JA}) .....66°C/W
2.5mmx2.5mm Thin MLF-12L (θ_{JC}) .....37°C/W

Electrical Characteristics[5]

V_{AVIN} = V_{DVIN} = 3.6V; I_{DC-DC} = 20mA, I_{LDO} = 100µA; L = 2.2µH; C_{OUT} = 4.7µF; C_{OUTLDO} = 1µF; T_A = 25°C.

Bold values indicate –40°C≤ T_J ≤ +125°C, unless noted.

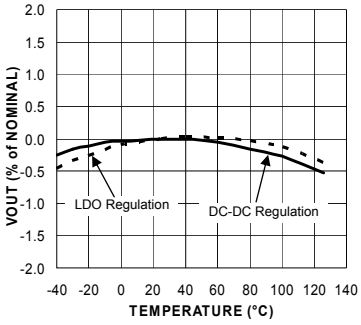
Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range		**2.7**		**5.5**	V
Under-Voltage Lockout Threshold	(Rising)	**2.45**	2.55	**2.65**	V
UVLO Hysteresis			50		mV
Total Quiescent Current	$V_{S1/2}$ = High		43		µA
DLY Pin Current Source	V_{DLY} = 0V	0.75	1.25	1.75	µA
DLY Pin Threshold Voltage			1.25		V
S1/S2/S3 Input Voltage	Logic Low			**0.2**	V
	Logic High	**1.2**			
S1/S2/S3 Input Current	V_{IL} = < 0.2V		0.01	**1**	µA
	V_{IH} = >1.2V		0.01	**1**	µA
DC/DC Converter					
Quiescent Current, Hyper LL mode	I_{OUT} = 0mA		25	35	µA
Shutdown Current	S1 = S2 = S3 = 0V		0.01	5	µA
Output Voltage Accuracy	Nominal V_{OUT} tolerance	**-2.5**		**+2.5**	%
Current Limit in PWM Mode		**0.65**	1	1.7	A
Output Voltage Line regulation	V_{AVIN} = V_{DVIN} = 3.0V to 5.5V, I_{LOAD} = 20mA		0.7		%
Output Voltage Load regulation	20mA < $I_{LOAD\ DC/DC}$ < 300mA $I_{OUT\ LDO}$ = 0mA		0.5		%
PWM Switch ON-Resistance	I_{SW} = 100mA PMOS I_{SW} = -100mA NMOS		0.55 0.6		Ω
Frequency	$I_{LOAD\ DC/DC}$ = 170mA, V_{OUT} = 1.8V		4		MHz
Soft-start time	V_{OUT} = 0 to 90%, V_{AVIN} = V_{DVIN} = 3.6V		280		µs
Thermal Shutdown			160		°C
Thermal Shutdown Hysteresis			20		°C

Parameter	Condition	Min	Typ	Max	Units
LDO Regulator					
Output Voltage Accuracy		**-3.0**		**+3.0**	%
Load Regulation [6]	$I_{OUT\ LDO}$ = 100µA to 150mA		0.7	**1.0**	%
Ground Pin Current	$I_{OUT\ LDO}$ = 100µA to 300mA		20		µA
Ripple Rejection	F = up to 1kHz: $C_{OUT\ LDO}$ = 1.0uF		70		dB
	F = 1kHz to 20kHz; $C_{OUT\ LDO}$ = 1.0µF		45		dB
Current Limit	V_{OUT} = 0V	350	600	800	mA
Output Voltage Noise	$C_{OUT\ LDO}$ = 1.0µF, 10Hz to 100kHz		55		μV_{RMS}

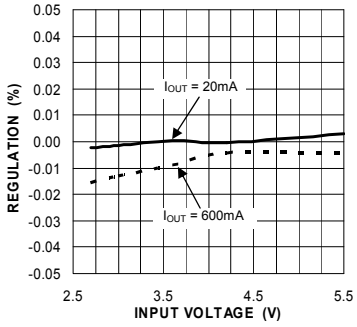
Notes:
1. Exceeding maximum rating may damage the device.
2. The device is not guaranteed to work outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.
6. Regulation is measured at constant junction temperature using low duty cycle pulse testing; changes in the output voltage due to heating effects are covered by the thermal regulation specification.

Typical Characteristics

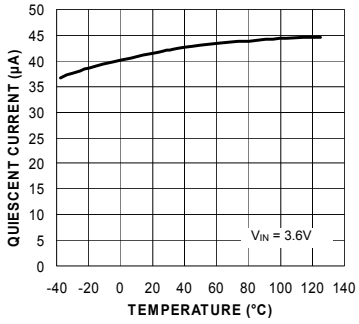
Voltage Accuracy vs. Temperature



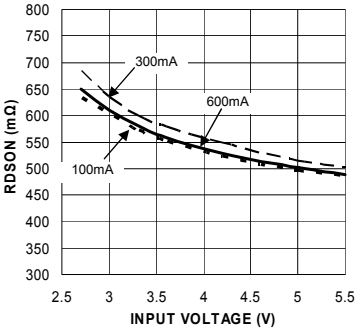
DC-DC Line Regulation



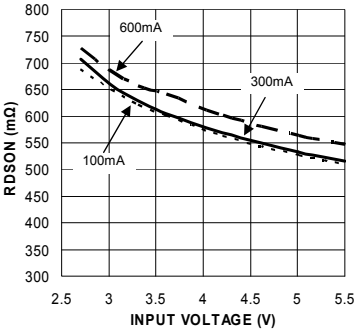
Quiescent Current vs. Temperature



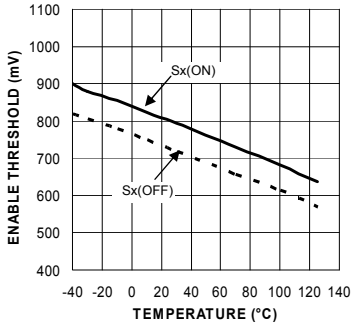
DC/DC P-Channel RDS_{ON} vs. Input Voltage



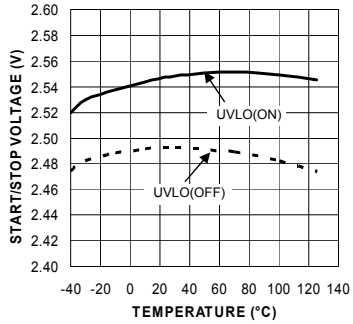
DC/DC N-Channel RDS_{ON} vs. Input Voltage



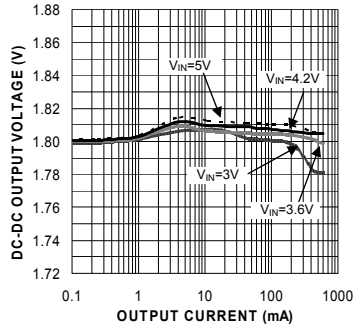
S1/S2/S3 Enable Threshold vs. Temperature



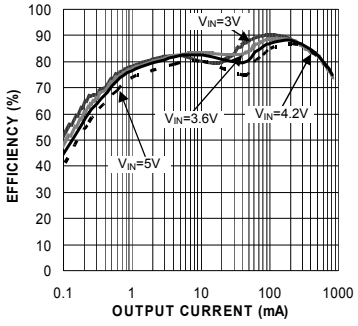
UVLO vs.Temperature



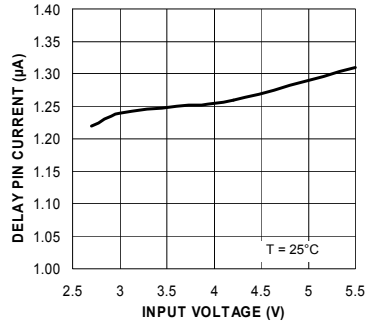
DC/DC Load Regulation



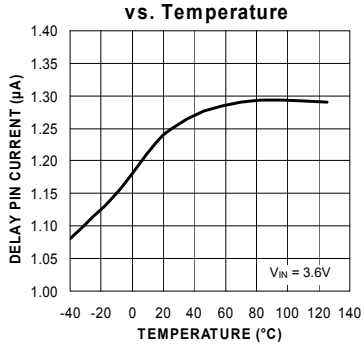
DC/DC Efficiency vs. Output Current



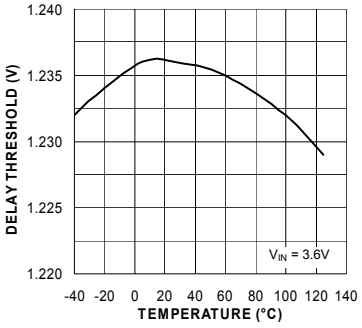
Delay Pin Current vs. Input Voltage



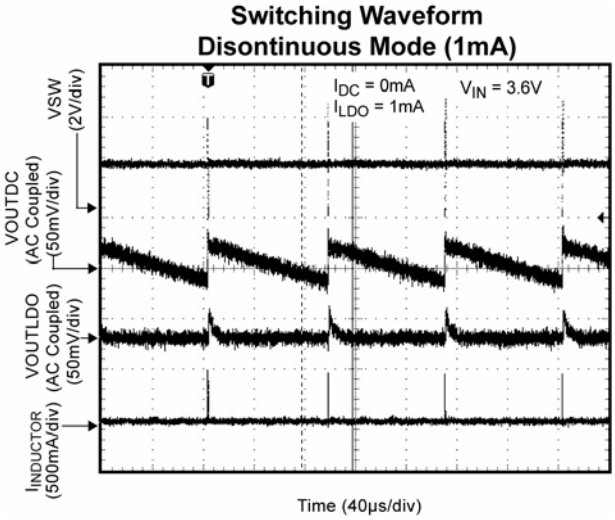
Delay Pin Current vs. Temperature

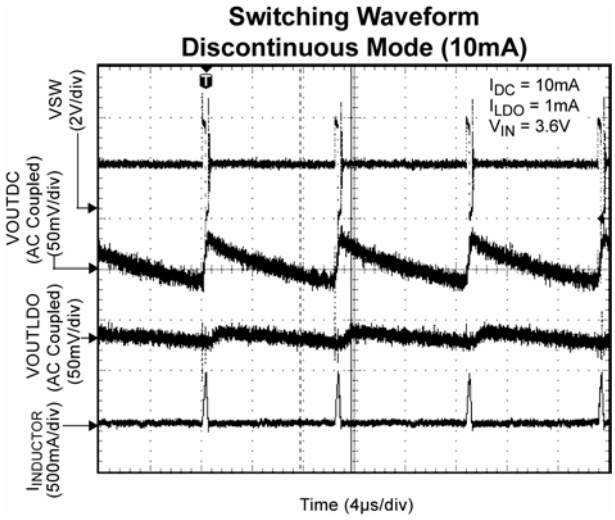


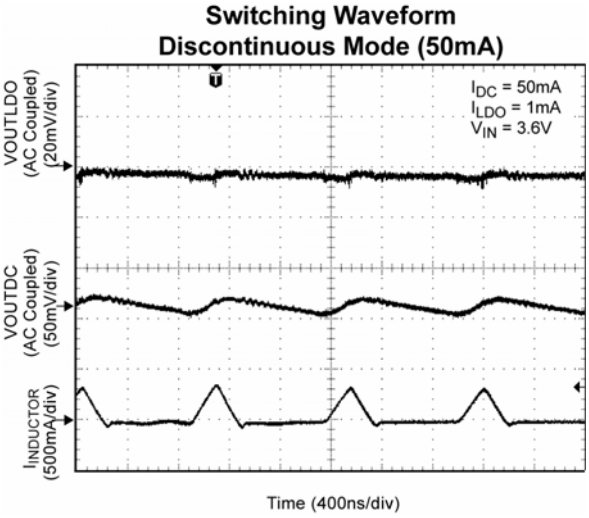
Delay Threshold vs. Temperature

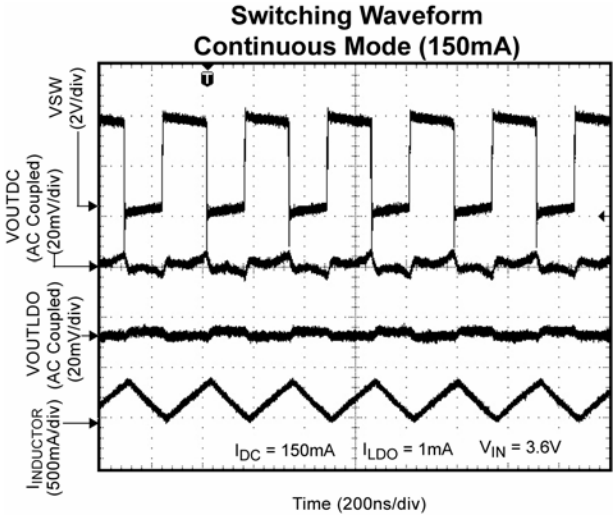


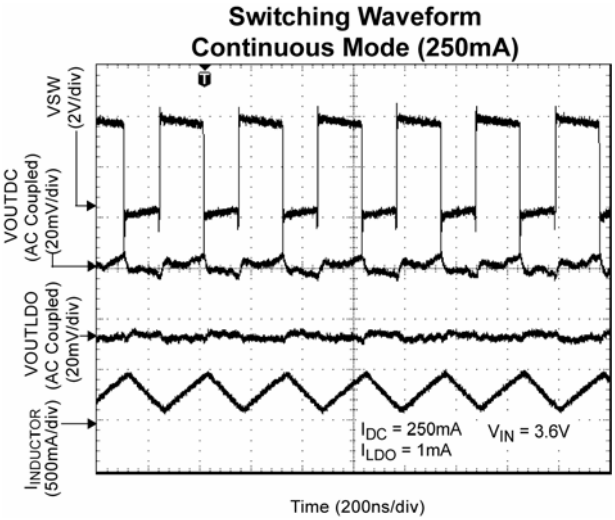
Functional Characteristics

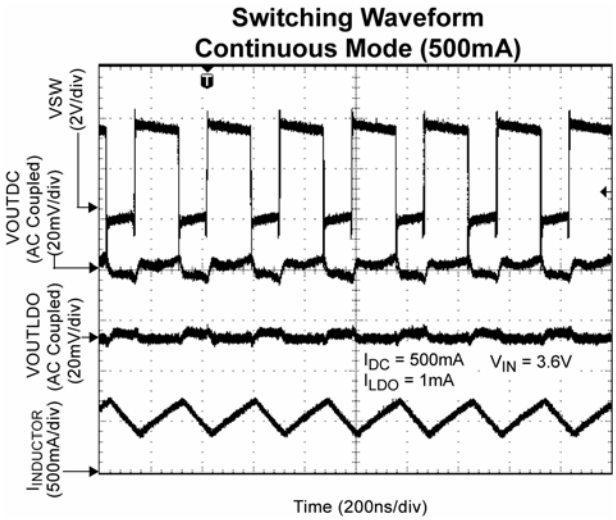






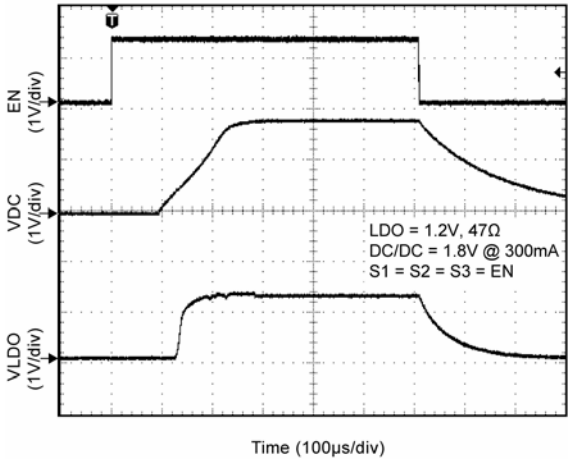




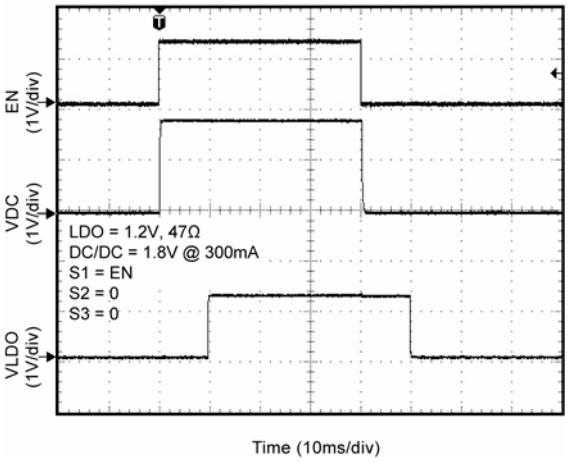


Functional Characteristics (Continued)

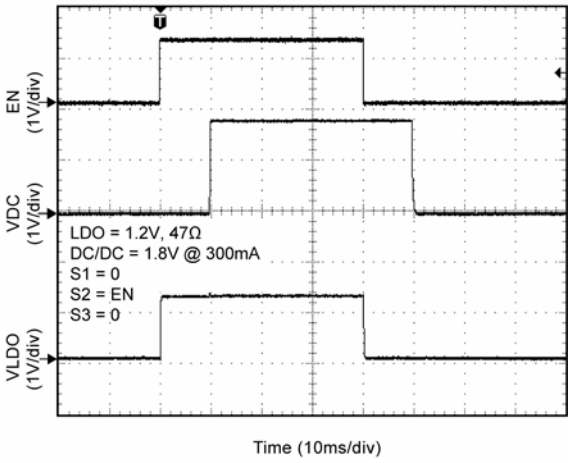
Start-Up Sequence (CDLY = 100pF)



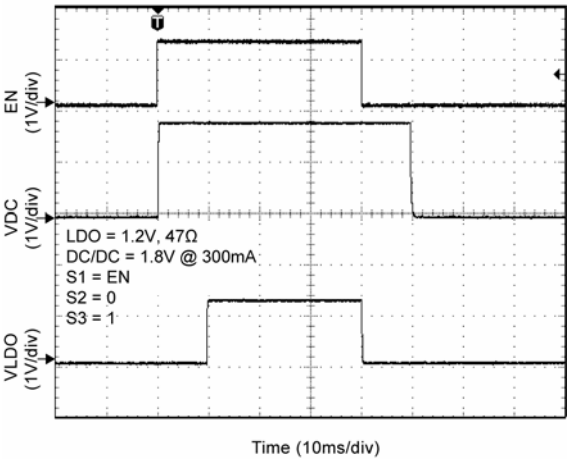
Start-Up Sequence (CDLY = 10nF)



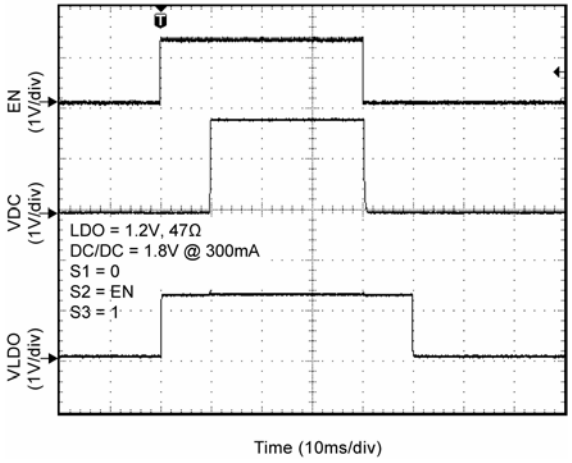
Start-Up Sequence (CDLY = 10nF)



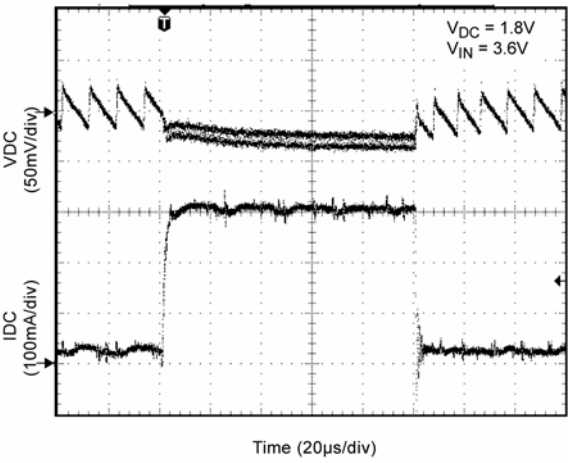
Start-Up Sequence (CDLY = 10nF)



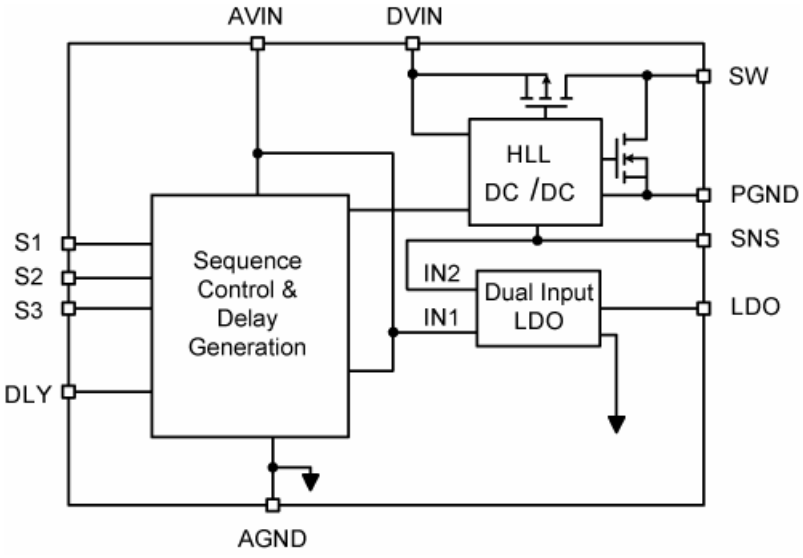
Start-Up Sequence (CDLY = 10nF)



Transient Response (10mA to 300mA)



Functional Diagram



MIC23060 Block Diagram

Functional Description

DVIN

The main input supply (DVIN) provides power to the internal MOSFETs for the switch mode regulator. The DVIN operating range is 2.7V to 5.5V, so an input capacitor, with a minimum voltage rating of 6.3V is recommended. Due to the high switching speed, a minimum 2.2µF bypass capacitor placed close to DVIN and the power ground (PGND) pin is required. For best performance a 4.7µF capacitor is recommended, refer to the layout recommendations for details.

AVIN

The Analog input supply (AVIN) provides power to the low power, biasing and control circuitry. Due to the high switching speed of the DC/DC converter, this should ideally be connected away from the DVIN bypass capacitor at the input supply. Refer to layout recommendations for more details.

S1/S2/S3

A logic high signal on the Set pins activates the output voltage of the devices in various sequencing modes. A logic low signal on the Set pins deactivates the outputs in various sequences and reduces supply current to 0.01µA. Full details of start-up/shutdown sequencing are given in the Application Information section. The MIC23060 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. Do not leave these pins floating.

SW

The switch (SW) pin connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible.

SNS

The feedback (SNS) pin is connected to the output of the DC/DC converter to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to the layout recommendations for more details.

LDO

The LDO Output (LDO) pin is the output of the Dual Input LDO™. Power is provided by the DC/DC output during normal operation and briefly by V_{AVIN} during some start-up and Shutdown sequences. A ceramic bypass capacitor of at least 1µF is required.

DLY

The delay (DLY) pin is connected to an external capacitor and AGND to set the delay time between the first regulator output reaching 90% of its regulated voltage and enabling the second regulator. The same delay time is also used during shutdown.

AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the layout recommendations for more details.

PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop as applicable. Refer to the layout recommendations for more details.

Application Information

The MIC23060 is a high performance DC/DC step down regulator plus Dual input Low Dropout linear regulator offering a small solution size. Supporting a recommended maximum output current of 300mA and 300mA respectively inside a tiny 2.5mm x 2.5mm Thin MLF® package and requiring only four external components, the MIC23060 meets today's miniature portable electronic device needs. Using the HyperLight Load™ switching scheme, the MIC23060 DC/DC converter is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

Input Capacitor

A 4.7µF ceramic capacitor should be placed close to the DVIN pin and PGND pin for decoupling the high di/dt pulses of the DC-DC section from the LDO section. A TDK C1608X5R0J475K, size 0603, 4.7µF ceramic capacitor is recommended based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The MIC23060 was designed for use with a 2.2µF or greater ceramic output capacitor for the DC-DC section and 1µF for the LDO. Increasing the output capacitance will lower output ripple and improve load transient response but could increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the TDK C1608X5R0J475K, size 0603, 4.7µF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23060 was designed for use with a 0.47µH to 2.2µH inductor. Typically, a 1µH inductor is recommended for a balance of transient response, efficiency and output ripple. For faster transient response, a 0.47µH inductor will yield the best result. For lower output ripple and improved regulation, a 2.2µH inductor is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as follows:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \times \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right]$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

Compensation

The MIC23060 is designed to be stable with a 0.47µH to 2.2µH inductor with a minimum of 4.7µF ceramic (X5R) output capacitor for the DC/DC output (SNS) and 1µF ceramic (X5R) for the LDO (LDO). For 0.47µH inductors, a 10µF capacitor is recommended to reduce ripple and improve stability.

Enable Sequencing (S1/S2/S3)

The MIC23060 offers complete flexibility of start-up sequencing of its two outputs. The sequence mode is set in hardware (pin-strapping) which requires that only a single GPIO be used for enable toggling. The Dual Input LDO™ can turn-on prior to the DC/DC converter and automatically switch to post regulation from the DC/DC converter after it starts.

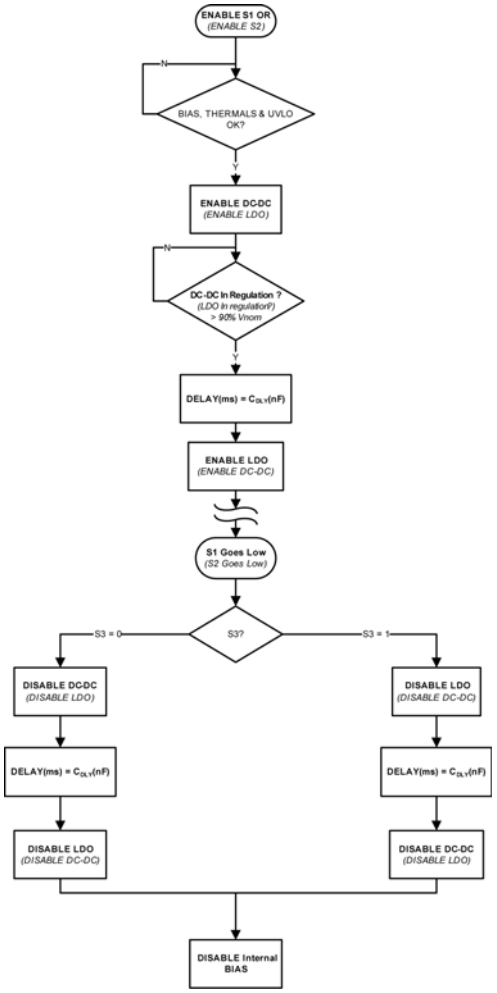
There are 3 modes available:

- S1=S2: Simultaneous (SIM)
- S3 = 0: First On/First Off (FOFO)
- S3 = 1: First On/Last Off (FOLO)

S3 is responsible for controlling the First-on/First-Off

modes, S2 controls the LDO sequence and S1 controls the DC/DC sequence. Here is a Truth Table followed by a flow chart of the sequencing events:

S3	S2	S1	Sequence
X	0	0	ALL OFF
0	0	EN	DC-DC ON 1st / OFF 1st
0	EN	0	LDO ON 1st / OFF 1st
1	0	EN	DC-DC ON 1st / OFF 2nd
1	EN	0	LDO ON 1st / OFF 2nd
X	1	1	ALL ON



Flow Chart of the Enable & Disable sequence

DLY

The value of capacitor on this pin is used to program the enable and disable delay times. The delay time follows the following equation:

$$T_{DLY} = V_{DLY}.C_{DLY} / I_{DLY}$$

Where nominally: V_{DLY} = 1.25V, I_{DLY} = 1.25µA

$$\therefore T_{DLY}(ms) = C_{DLY}(nF)$$

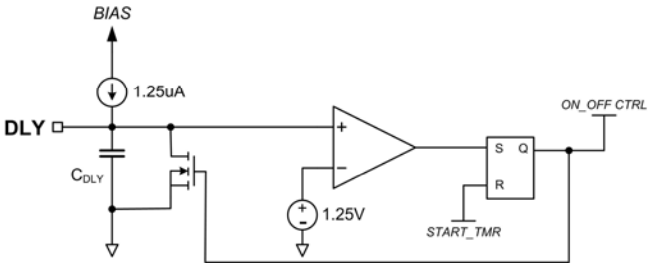
For example, an application where the LDO should be enabled 50ms before the DC/DC and disabled 50ms after the DC-DC, the pins should be set as follows:

S1 = 0

S3 = 1

C_{DLY} = 50nF

S2 = Enable stimulus



Detail of the delay timer circuit.

Duty Cycle

The typical maximum duty cycle of the MIC23060 is 80%.

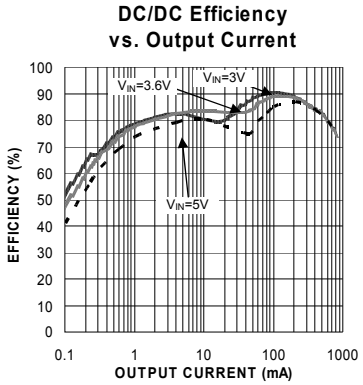
Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency}(\%) = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, simplifying thermal design considerations, and it reduces current consumption for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET R_{DSON} multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 4MHz frequency and the switching transitions make up the switching losses.



The figure above shows an efficiency curve. From no load to 100mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load™ mode, the MIC23060 is able to maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the Gate-to-Source drive at the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$\text{DCR Loss} = I_{OUT}^2 \times \text{DCR}$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency\_Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L\_P_D}\right)\right] \times 100$$

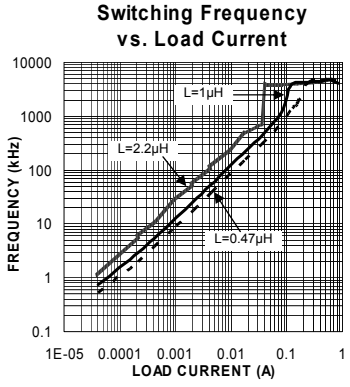
Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

HyperLight Load™ Mode

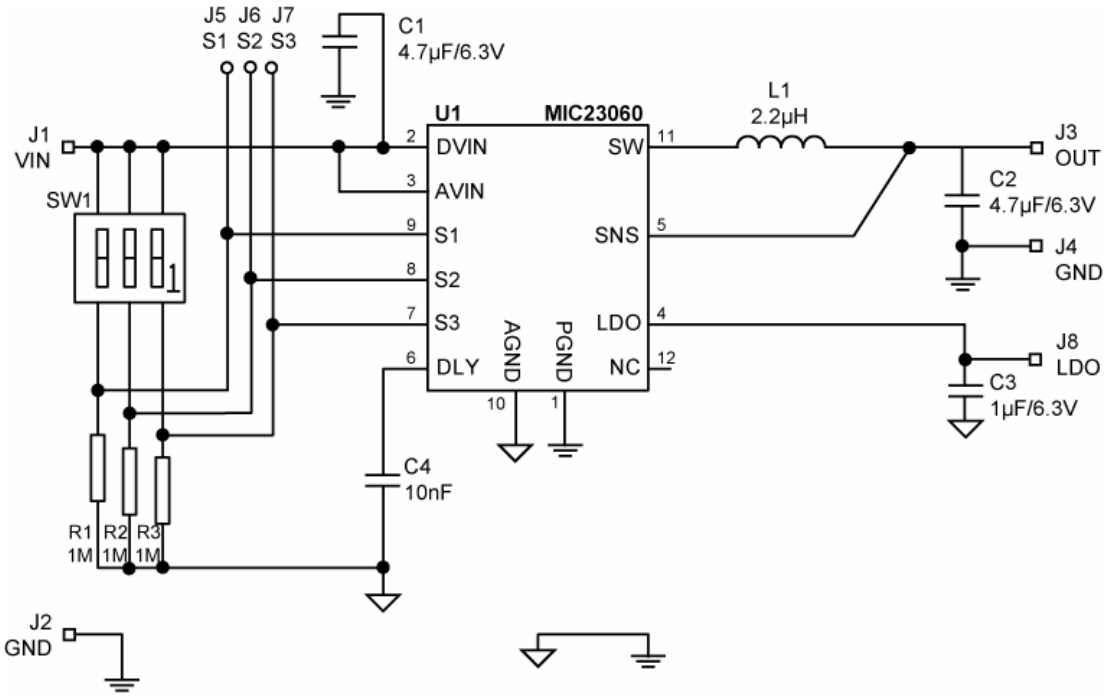
MIC23060 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23060 works in pulse frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23060 during light load currents by only switching when it is needed. As the load current increases, the MIC23060 goes into continuous conduction mode (CCM) and switches at a frequency centred at 4MHz. The equation to calculate the load when the MIC23060 goes into continuous conduction mode may be approximated by the following formula:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f}\right)$$

As shown in the previous equation, the load at which MIC23060 transitions from HyperLight Load™ mode to PWM mode is a function of the input voltage (V_{DVIN}), output voltage (VOUT), duty cycle (D), inductance (L) and frequency (f). As shown in the figure below, as the Output Current increases, the switching frequency also increases until the MIC23060 goes from HyperLight Load™ mode to PWM mode at approximately 120mA. The MIC23060 will switch at a relatively constant frequency around 4MHz once the output current is over 120mA.



Evaluation Board Schematic



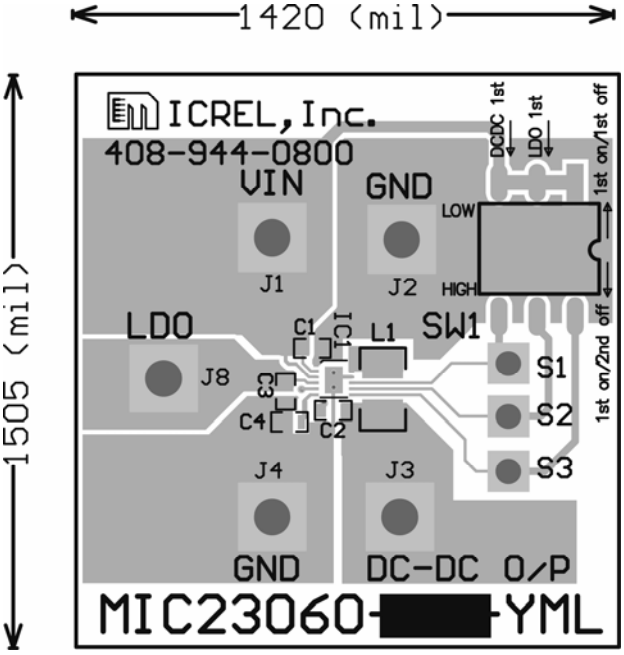
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2	GRM188R60J475KE19D	Murata[1]	Ceramic Capacitor, 4.7µF, 6.3V, X5R	2
	C1608X5R0J475K	TDK[2]		
C3	GRM188R71C105KA12D	Murata	Ceramic Capacitor, 1µF, 6.3V, X7R	1
C4	GRM188R71C103K	Murata	Ceramic Capacitor, 10nF, 6.3V, X7R	1
L1	LQM2MPN2R2NG0L	Murata	2mm x 1.6mm Multilayer Inductor, 2.2µH, 1.2A	1
	VLS201610ET-2R2M	TDK	2mm x 1.6mm Power Inductor, 2.2µH, 1A	
SW1	418121270803	Wurth[3]	2.54mm small SMD DIP Switch (w/raised actuator)	1
R1, R2, R3	CRCW06031004FKEYE3	Vishay[4]	Resistor, 1M, 1%. 1/16W, Size 0603	3
U1	**MIC23060-G4YMT**	**Micrel, Inc.[5]**	**Sequenced digital power management IC**	**1**

Notes:

1. Murata: www.murata.com
2. TDK: www.tdk.com
3. Wurth Elektrik: www.we-online.com
4. Vishay: www.vishay.com.
5. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations



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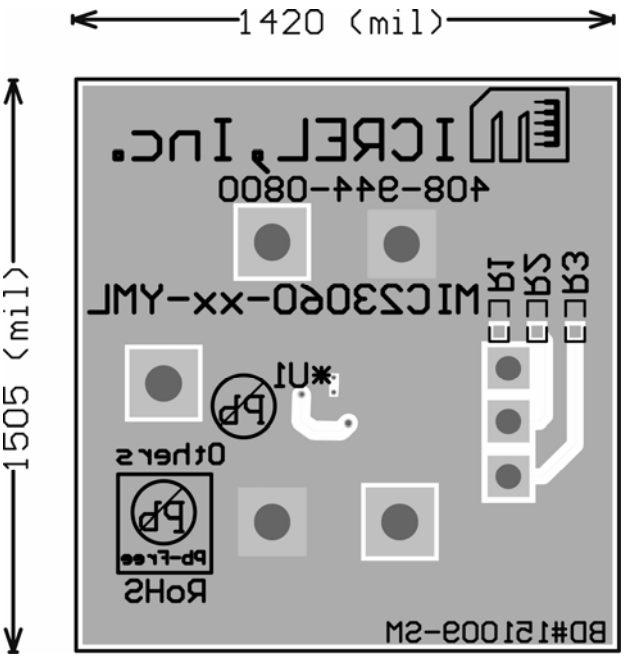
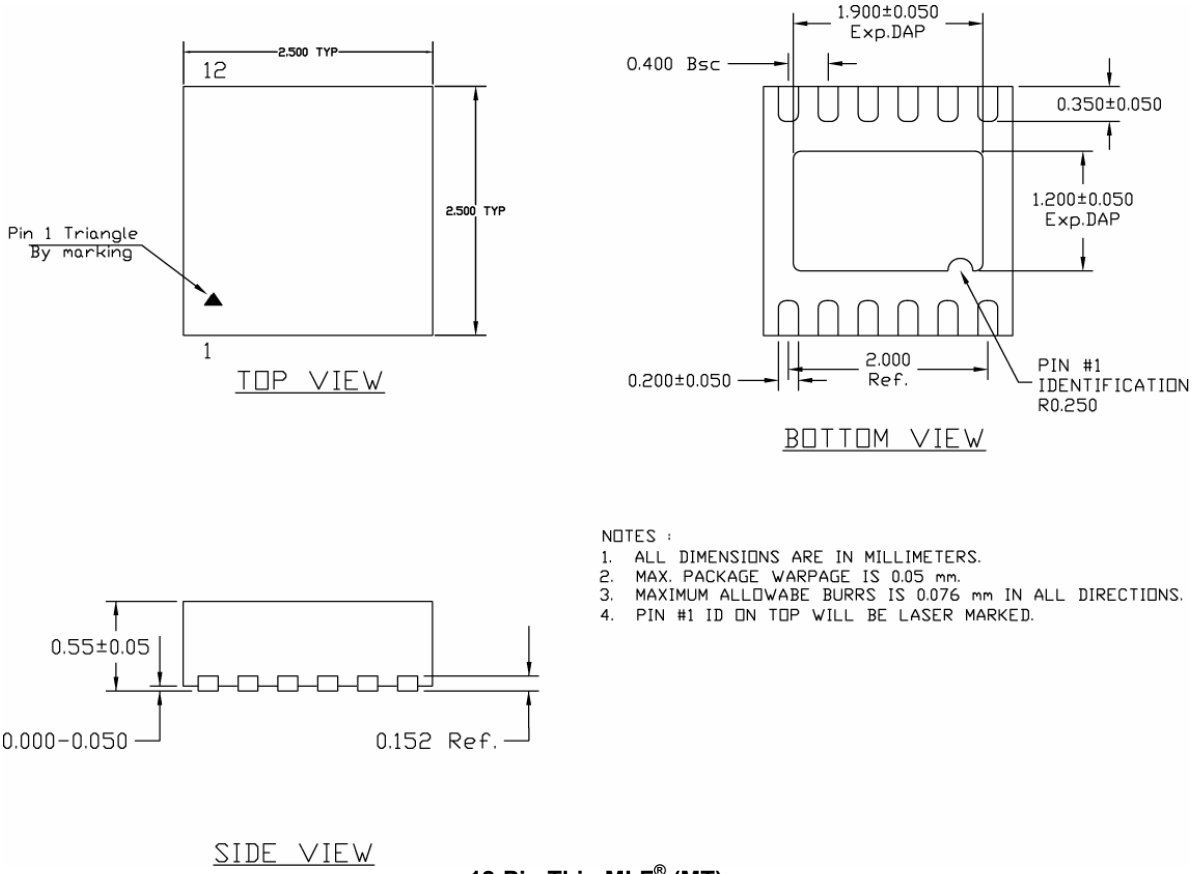


Bottom Layer

Package Information



12-Pin Thin MLF® (MT)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com