



# NAND Flash and Mobile LPDRAM

## 152-Ball Package-on-Package (PoP) Combination Memory (TI OMAP™) MT29C Family

Current production part numbers: See Table 1 on page 3

### Features

- Micron® NAND Flash and Mobile LPDRAM components
- RoHS-compliant, “green” package
- Separate NAND Flash and Mobile LPDRAM interfaces
- Space-saving package-on-package combination
- Low-voltage operation (1.70–1.95V)
- Industrial temperature range: –40°C to +85°C

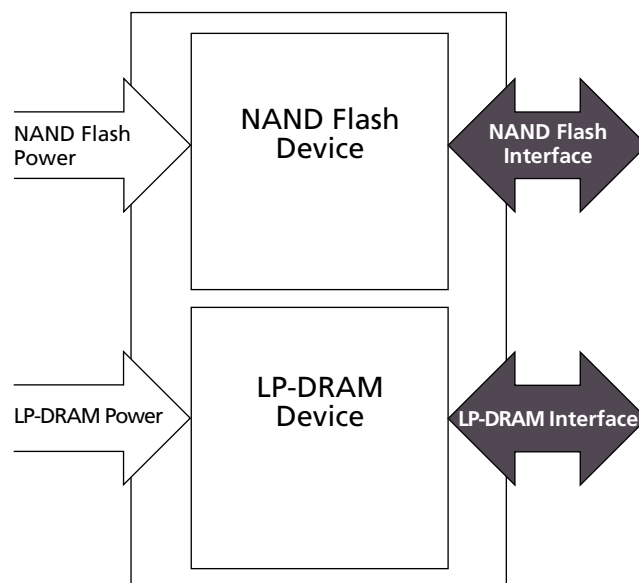
### NAND Flash-Specific Features

- Organization
  - Page size
    - x8: 2112 bytes (2048 + 64 bytes)
    - x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)

### Mobile LPDRAM-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- STATUS REGISTER READ (SRR) supported<sup>1</sup>

**Figure 1: PoP Block Diagram**



### Options

- LP-DRAM
  - 166 MHz CL3<sup>2</sup>
  - 133 MHz CL3

### Marking

-6  
-75

Notes: 1. Contact factory for remapped SRR output.  
2. CL = CAS (READ) latency.

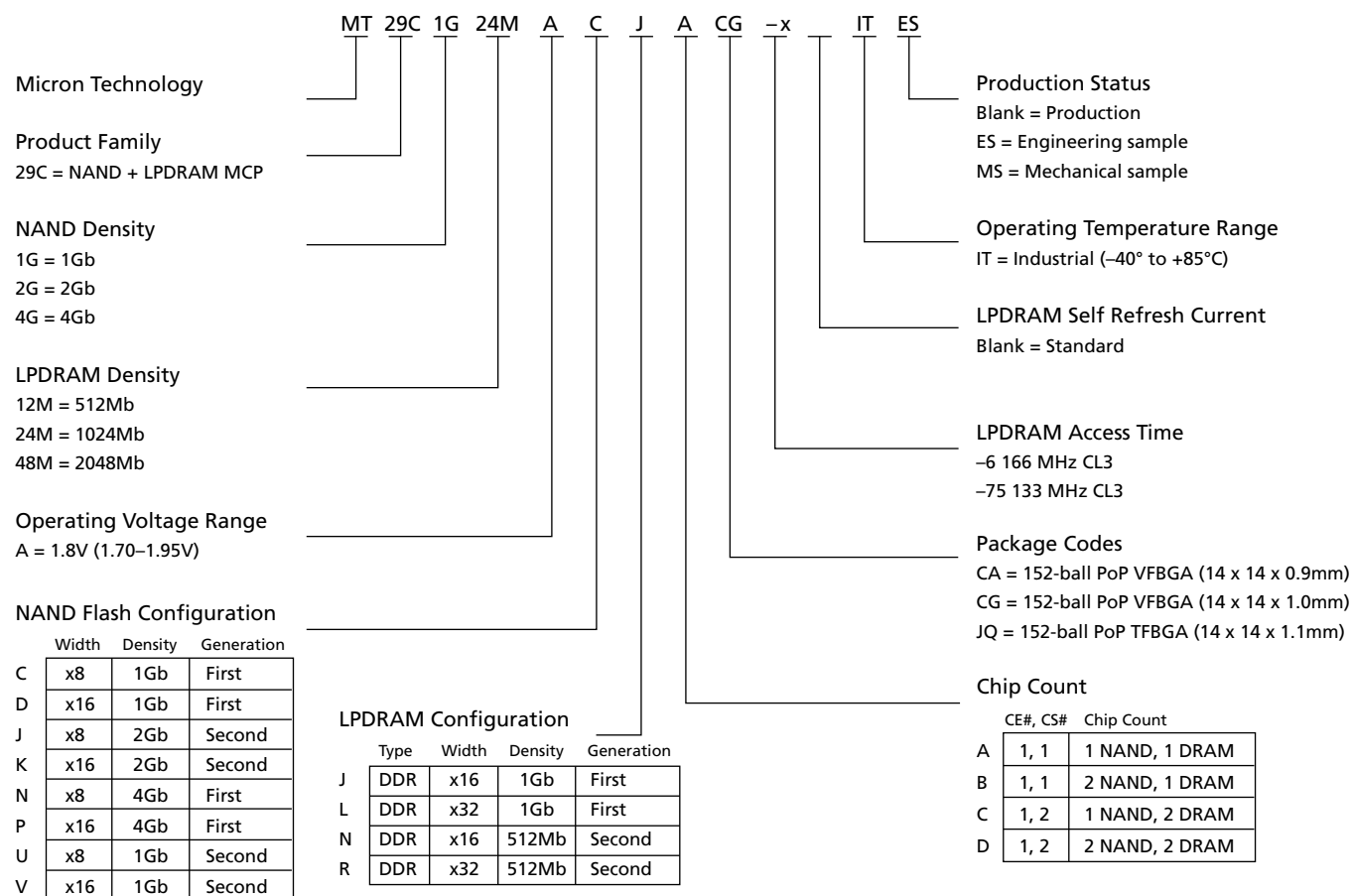


# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Part Numbering Information – 152-Ball PoP

## Part Numbering Information – 152-Ball PoP

Micron NAND Flash and LPDRAM devices are available in different configurations and densities.

**Figure 2: 152-Ball Part Number Chart**



**Note:** Not all possible combinations are available. Contact factory for availability.



# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Device Marking

**Table 1: Production Part Numbers**

| Part Number            | NAND Product        | LPDDR Product     | Physical Part Marking |
|------------------------|---------------------|-------------------|-----------------------|
| MT29C4G48MAPLCCA-6 IT  | MT46H32M32LFJG-6 IT | MT29F4G16ABCWC-ET | JW399                 |
| MT29C4G48MAPLCCA-75 IT | MT46H32M32LFJG-6 IT | MT29F4G16ABCWC-ET | JW400                 |
| MT29C4G48MAPLCJQ-6 IT  | MT46H32M32LFJG-6 IT | MT29F4G16ABCWC-ET | JW297                 |
| MT29C4G48MAPLCJQ-75 IT | MT46H32M32LFJG-6 IT | MT29F4G16ABCWC-ET | JW296                 |
| MT29C1G12MADRACG-6 IT  | MT46H16M32LFCM-6 IT | MT29F1G16ABBHC-ET | JW226                 |
| MT29C1G12MADRACG-75 IT | MT46H16M32LFCM-6 IT | MT29F1G16ABBHC-ET | JW227                 |
| MT29C2G24MAKLACG-6 IT  | MT46H32M32LFJG-6 IT | MT29F2G16ABDHC-ET | JW188                 |
| MT29C2G24MAKLACG-75 IT | MT46H32M32LFJG-6 IT | MT29F2G16ABDHC-ET | JW189                 |
| MT29C1G12MAURACA-6 IT  | MT46H16M32LFCM-6 IT | MT29F1G08ABCHC-ET | JW385                 |
| MT29C1G12MAURACA-75 IT | MT46H16M32LFCM-6 IT | MT29F1G08ABCHC-ET | JW384                 |
| MT29C1G12MAVRACA-6 IT  | MT46H16M32LFCM-6 IT | MT29F1G16ABCHC-ET | JW375                 |
| MT29C1G12MAVRACA-75 IT | MT46H16M32LFCM-6 IT | MT29F1G16ABCHC-ET | JW374                 |

## Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: [www.micron.com/decoder](http://www.micron.com/decoder). To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at [www.micron.com/csn](http://www.micron.com/csn).



## 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP General Description

### General Description

Micron package-on-package (PoP) products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile LPDRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (i.e.,  $V_{SS}$  is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction. Operational characteristics for the NAND Flash and Mobile LPDRAM devices are found in the standard Micron data sheets for each of the discrete devices.

For device specifications and complete Micron NAND Flash features documentation, please refer to the component data sheet at [www.micron.com/products/nand](http://www.micron.com/products/nand), or contact your local Micron sales office.

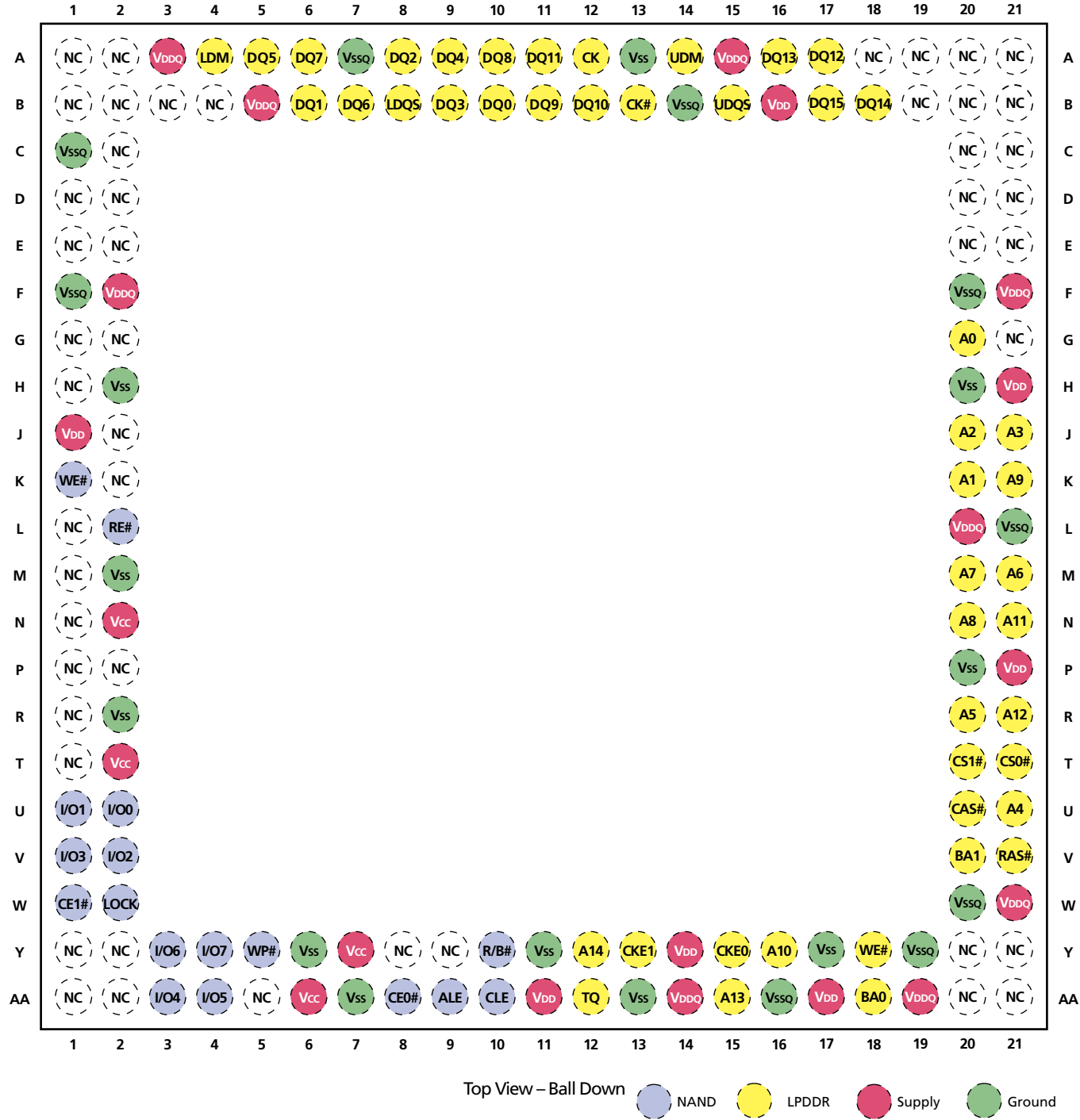
For device specifications and complete Mobile LPDRAM features documentation, please refer to the component data sheet at [www.micron.com/products/mobileDRAM](http://www.micron.com/products/mobileDRAM), or contact your local Micron sales office.



# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Ball Assignments and Descriptions

## Ball Assignments and Descriptions

Figure 3: 152-Ball VFBGA Ball Assignments (NAND x8; LPDDR x16)

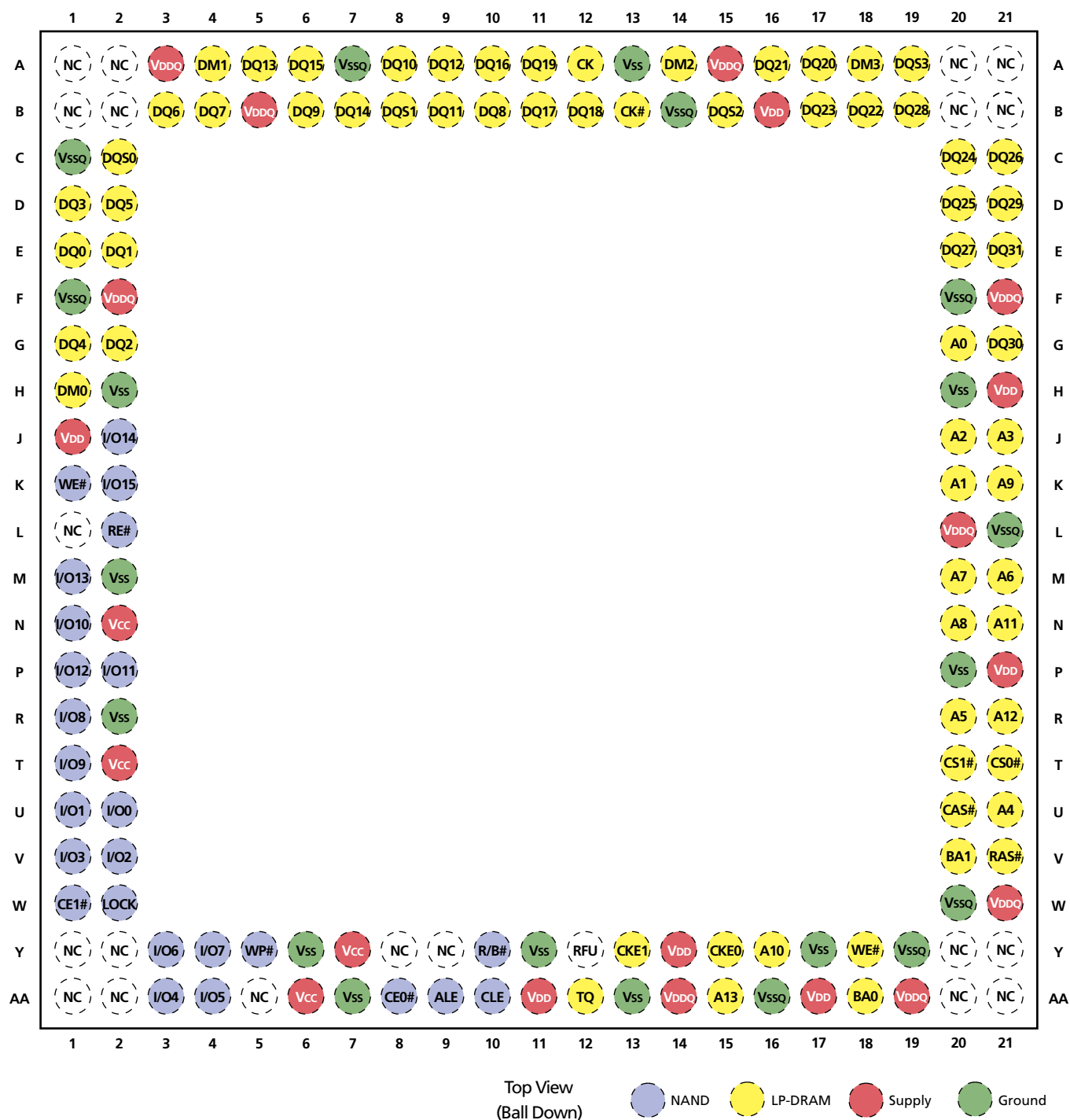


Note: Contact factory for availability of x16 LPDDR configuration.



# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Ball Assignments and Descriptions

**Figure 4: 152-Ball VFBGA Ball Assignments (NAND x16; LPDDR x32)**





# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Ball Assignments and Descriptions

**Table 2: x8/x16 NAND Ball Descriptions**

| Symbol                                     | Type             | Description                                                                                                                                                                                                                          |
|--------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ALE                                        | Input            | Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.                                                                                                                                |
| CE1#, CE0#                                 | Input            | Chip enable: Gates transfers between the host system and the NAND Flash device.                                                                                                                                                      |
| CLE                                        | Input            | Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.                                                                                                                                 |
| LOCK                                       | Input            | When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to V <sub>SS</sub> during power-up, or leave it unconnected (internal pull-down).                                         |
| RE#                                        | Input            | Read enable: Gates information from the NAND device to the host system.                                                                                                                                                              |
| WE#                                        | Input            | Write enable: Gates information from the host system to the NAND device.                                                                                                                                                             |
| WP#                                        | Input            | Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.                                                                                                                                                                  |
| I/O[7:0]<br>(x8)<br><br>I/O[15:0]<br>(x16) | Input/<br>output | Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs. I/O[15:8] are RFU <sup>1</sup> for NAND x8 devices. |
| R/B#                                       | Output           | Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress.                                                                                                                                  |
| V <sub>CC</sub>                            | Supply           | V <sub>CC</sub> : NAND power supply.                                                                                                                                                                                                 |

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.



# 152-Ball NAND Flash and Mobile LPDDR PoP (TI OMAP) MCP Ball Assignments and Descriptions

**Table 3: x16/x32 LPDDR Ball Descriptions**

| Symbol                                       | Type             | Description                                                                                                                                                                                                                                                                                          |
|----------------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[14:0]                                      | Input            | Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR address is determined by density and configuration. Consult the LPDDR product data sheet for the maximum address for a given density and configuration. Unused address pins become RFU. |
| BA1, BA0                                     | Input            | Bank address inputs: Specifies one of the 4 banks.                                                                                                                                                                                                                                                   |
| CAS#                                         | Input            | Column select: Specifies the command to execute.                                                                                                                                                                                                                                                     |
| CK, CK#                                      | Input            | CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.                                                                                                  |
| CKE0, CKE1                                   | Input            | Clock enable:<br>CKE0 is used for a single LPDDR product.<br>CKE1 is used for dual LPDDR products.                                                                                                                                                                                                   |
| CS1#, CS0#                                   | Input            | Chip select:<br>CS0# is used for a single LPDDR product.<br>CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.                                                                                                                                                        |
| LDM, UDM<br>(x16)<br><br>DM[3:0]<br>(x32)    | Input            | Data mask: Determines which bytes are written during WRITE operations.<br>For x16 LPDDR, unused DM balls become RFU.                                                                                                                                                                                 |
| RAS#                                         | Input            | Row select: Specifies the command to execute.                                                                                                                                                                                                                                                        |
| WE#                                          | Input            | Write enable: Specifies the command to execute.                                                                                                                                                                                                                                                      |
| DQ[15:0]<br>(x16)<br><br>DQ[31:0]<br>(x32)   | Input/<br>output | Data bus: Data inputs/outputs.<br>DQ[31:16] are RFU for x16 LPDDR devices.                                                                                                                                                                                                                           |
| LDQS, UDQS<br>(x16)<br><br>DQS[3:0]<br>(x32) | Input/<br>output | Data strobe: Coordinates READ/WRITE transfers of data; one DQS per DQ byte.<br>For x16 LPDDR, unused DQS balls become RFU.                                                                                                                                                                           |
| TQ                                           | Output           | Temperature sensor output: TQ HIGH when LPDDR T <sub>j</sub> exceeds 85°C.                                                                                                                                                                                                                           |
| V <sub>DD</sub>                              | Supply           | V <sub>DD</sub> : LPDDR power supply.                                                                                                                                                                                                                                                                |
| V <sub>DDQ</sub>                             | Supply           | V <sub>DDQ</sub> : LPDDR I/O power supply.                                                                                                                                                                                                                                                           |
| V <sub>SSQ</sub>                             | Supply           | V <sub>SSQ</sub> : LPDDR I/O ground.                                                                                                                                                                                                                                                                 |

**Table 4: Non-Device-Specific Ball Descriptions**

| Symbol           | Type   | Description                           |
|------------------|--------|---------------------------------------|
| V <sub>SS</sub>  | Supply | V <sub>SS</sub> : Shared ground.      |
| NC               | –      | No connect: Not internally connected. |
| RFU <sup>1</sup> | –      | Reserved for future use.              |

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.





# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Electrical Specifications

## Electrical Specifications

**Table 5: Absolute Maximum Ratings**

| Parameters/Conditions                                               | Symbol                          | Min  | Max                                                            | Unit |
|---------------------------------------------------------------------|---------------------------------|------|----------------------------------------------------------------|------|
| $V_{CC}$ , $V_{DD}$ , $V_{DDQ}$ supply voltage relative to $V_{SS}$ | $V_{CC}$ , $V_{DD}$ , $V_{DDQ}$ | -1.0 | 2.4                                                            | V    |
| Voltage on any pin relative to $V_{SS}$                             | $V_{IN}$                        | -0.5 | 2.4 or (supply voltage <sup>1</sup> + 0.3V), whichever is less | V    |
| Storage temperature range                                           | —                               | -55  | +150                                                           | °C   |

Notes: 1. Supply voltage references either  $V_{CC}$ ,  $V_{DD}$ , or  $V_{DDQ}$ .

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 6: Recommended Operating Conditions**

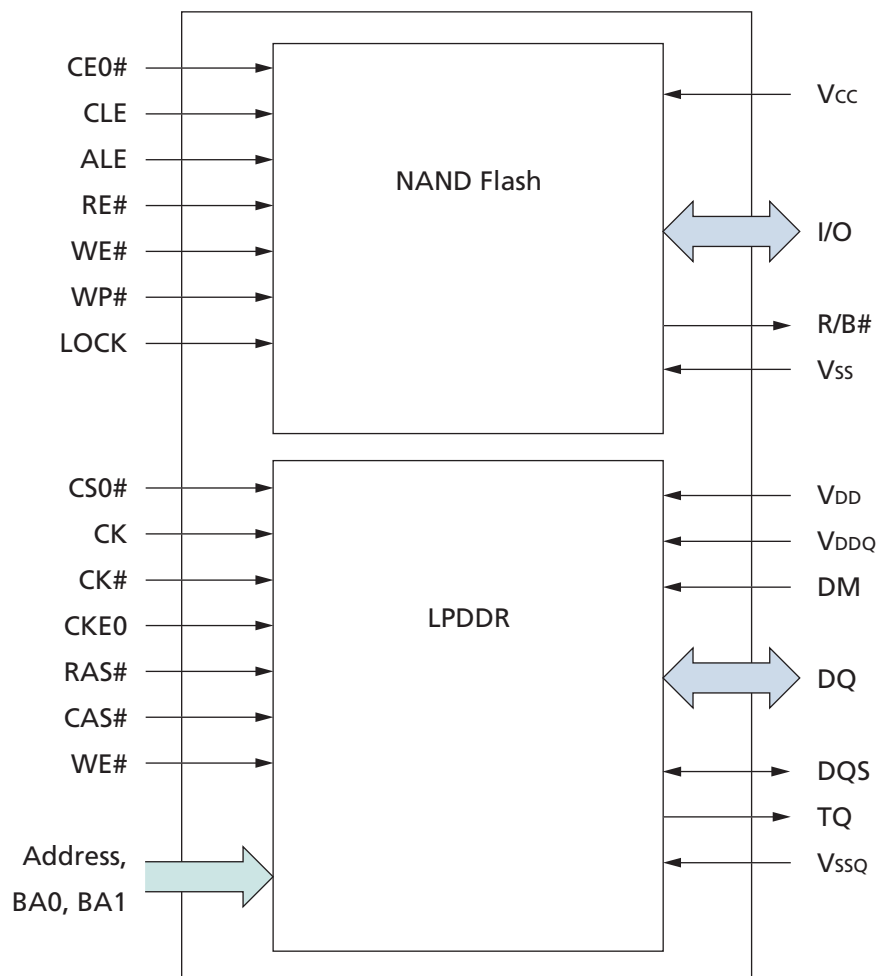
| Parameters                  | Symbol              | Min  | Typ  | Max  | Unit |
|-----------------------------|---------------------|------|------|------|------|
| Supply voltage              | $V_{CC}$ , $V_{DD}$ | 1.70 | 1.80 | 1.95 | V    |
| I/O supply voltage          | $V_{DDQ}$           | 1.70 | 1.80 | 1.95 | V    |
| Operating temperature range | —                   | -40  | —    | +85  | °C   |



# 152-Ball NAND Flash and Mobile LPDDR PoP (TI OMAP) MCP Device Diagrams

## Device Diagrams

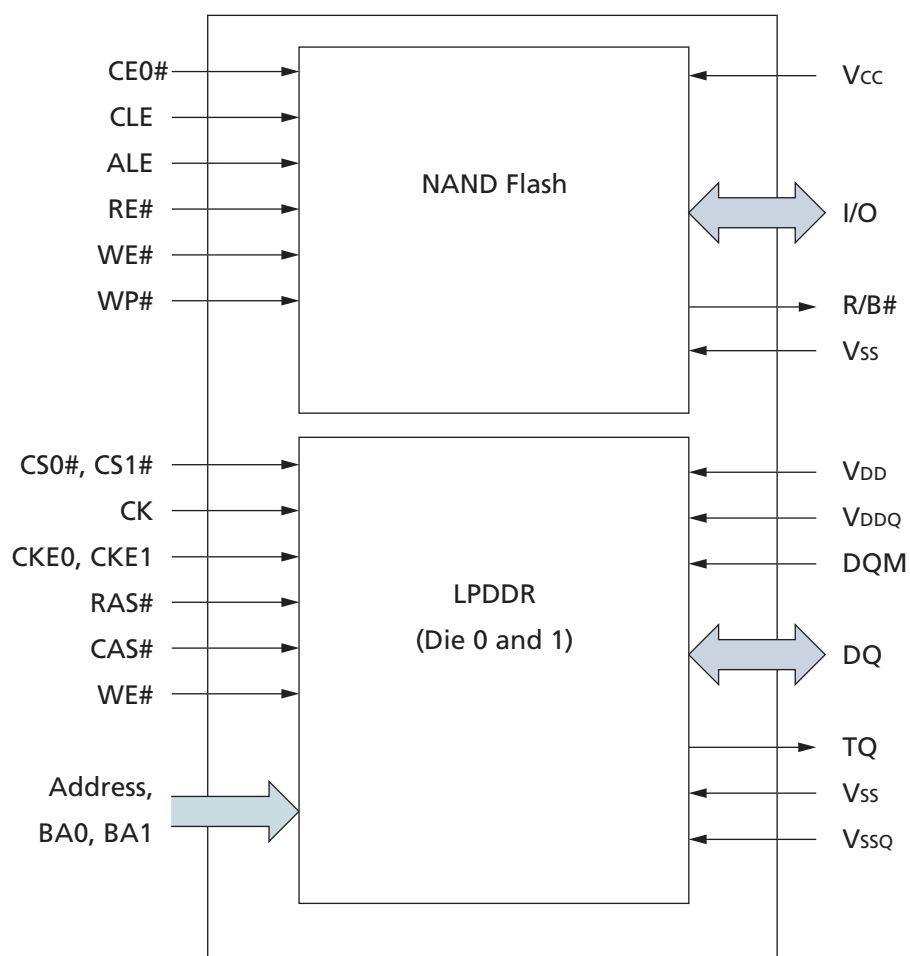
Figure 5: 152-Ball Functional Block Diagram (Single LPDDR)





# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Device Diagrams

**Figure 6: 152-Ball Functional Block Diagram (Dual LPDDR)**

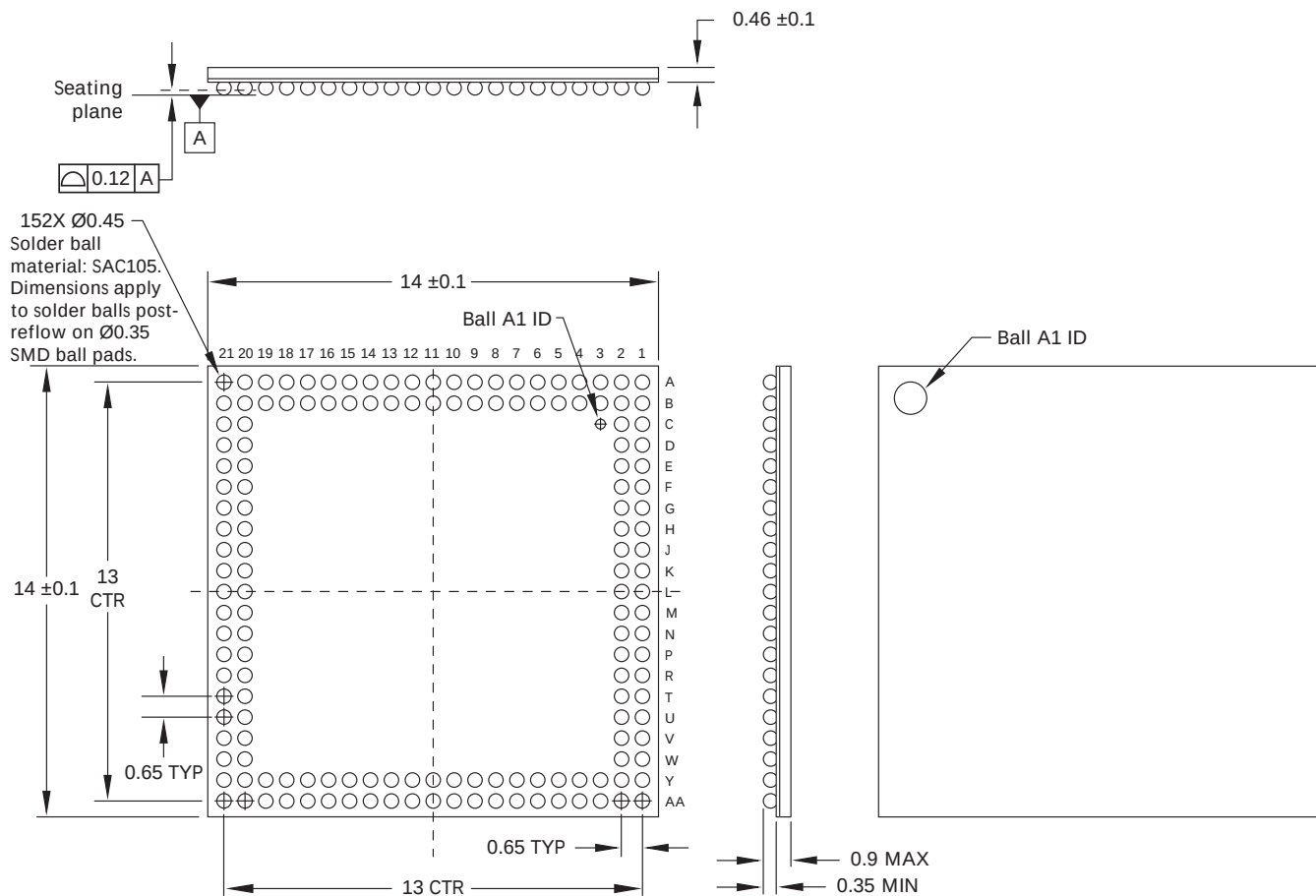




# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Package Dimensions

## Package Dimensions

**Figure 7: 152-Ball VFBGA (Package Code: CA)**

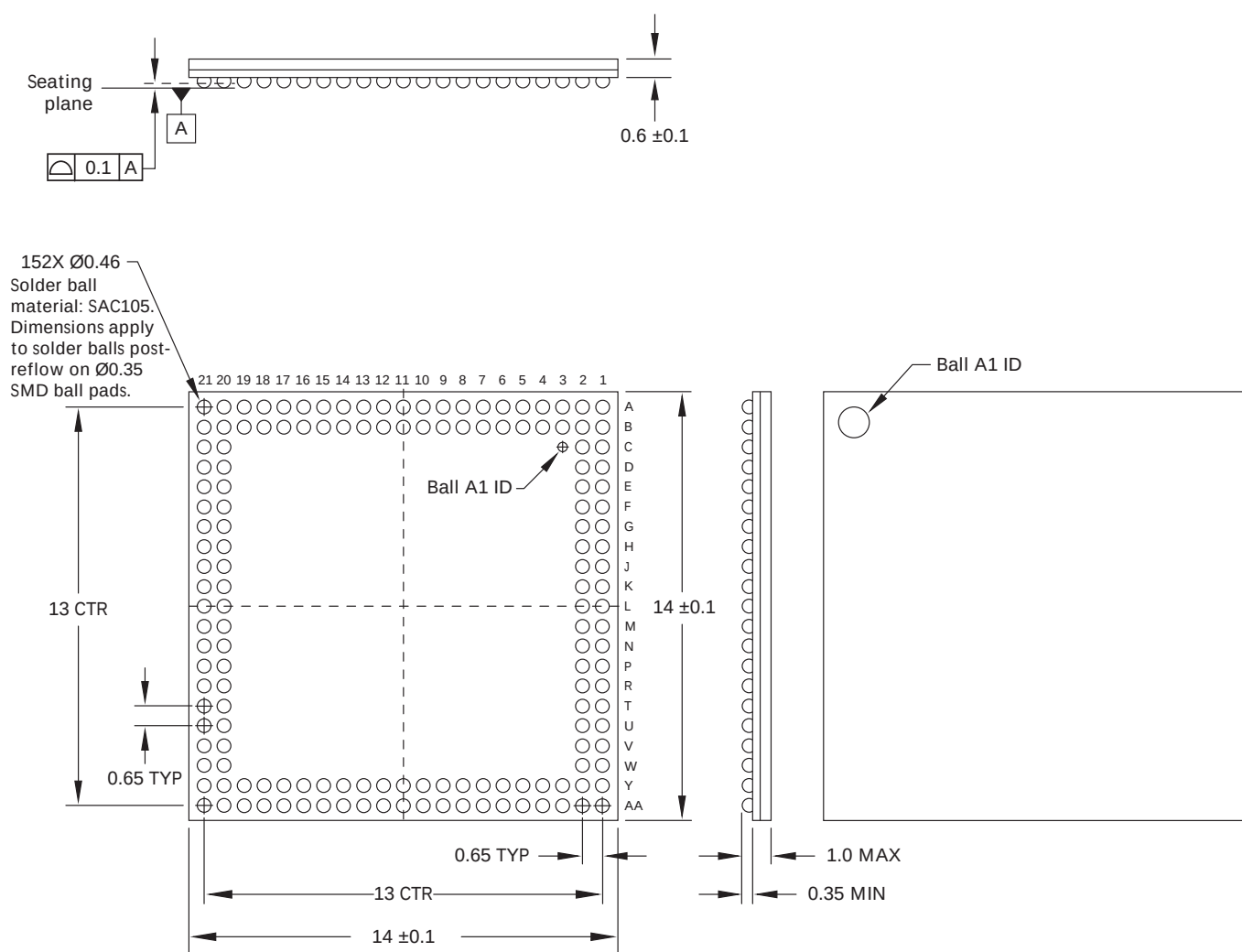


Note: All dimensions are in millimeters.



# 152-Ball NAND Flash and Mobile LPDRAM PoP (TI OMAP) MCP Package Dimensions

**Figure 8: 152-Ball VFBGA (Package Code: CG)**



Note: All dimensions are in millimeters.





## Revision History

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |              |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| <b>Rev. E, Preliminary</b> .....                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>4/09</b>  |
| <ul style="list-style-type: none"> <li>• “NAND Flash-Specific Features” on page 1: Deleted device size bullet.</li> <li>• Figure 2: “152-Ball Part Number Chart,” on page 2: Added U and V options under NAND Flash configurations; deleted low-power option under LPDRAM self refresh current; added dimensions to package codes; added CS# to first column under chip count; changed CE# from 2 to 1 for B and D under chip count.</li> <li>• Table 1, “Production Part Numbers,” on page 3: Replaced former table 1.</li> <li>• Figure 3: “152-Ball VFBGA Ball Assignments (NAND x8; LPDDR x16),” on page 5: Updated figure.</li> <li>• Figure 4: “152-Ball VFBGA Ball Assignments (NAND x16; LPDDR x32),” on page 6: Updated figure.</li> <li>• Table 2, “x8/x16 NAND Ball Descriptions,” on page 7: Updated table.</li> <li>• Table 3, “x16/x32 LPDDR Ball Descriptions,” on page 8: Updated table.</li> <li>• Table 4, “Non-Device-Specific Ball Descriptions,” on page 8: Updated table.</li> <li>• Table 5, “Absolute Maximum Ratings,” on page 9: Updated table.</li> <li>• Table 6, “Recommended Operating Conditions,” on page 9: Updated table.</li> <li>• Figure 5: “152-Ball Functional Block Diagram (Single LPDDR),” on page 10: Updated figure title; updated figure.</li> <li>• Figure 6: “152-Ball Functional Block Diagram (Dual LPDDR),” on page 11: Added figure.</li> </ul> |              |
| <b>Rev. D, Preliminary</b> .....                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>11/08</b> |
| <ul style="list-style-type: none"> <li>• Updated template; ready for external publication.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |              |
| <b>Rev. C, Preliminary</b> .....                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>8/08</b>  |
| <ul style="list-style-type: none"> <li>• Added part number for JQ package code, page 1.</li> <li>• Figure 2, Marketing Part Number Example, on page 2: added JQ package code.</li> <li>• Added JQ package diagram, Figure 9, 152-Ball TFBGA (Package Code: JQ), on page 14.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |              |
| <b>Rev. B, Preliminary</b> .....                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>4/08</b>  |
| <ul style="list-style-type: none"> <li>• On page 1, added part number for CA package code.</li> <li>• Figure 2: Marketing Part Number Example on page 2: Added CA package code.</li> <li>• Removed former capacitance tables. See component data sheets for capacitance.</li> <li>• Figure 7: 152-Ball VFBGA (Package Code: CA) on page 12, and Figure 8: 152-Ball VFBGA (Package Code: CG) on page 13: Updated figures.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |              |
| <b>Rev. A, Preliminary</b> .....                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>2/08</b>  |
| <ul style="list-style-type: none"> <li>• Initial release.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |