

1Mx32 3.3V NOR FLASH MODULE

FEATURES

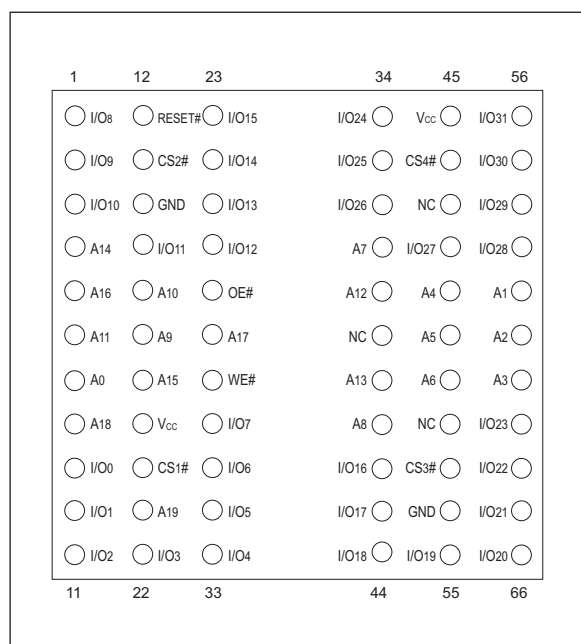
- Access Times of 100, 120, 150ns
- Packaging
 - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
 - 68 lead, Low Profile CQFP (G2U), 3.5mm (0.140") square (Package 510)
- 1,000,000 Erase/Program Cycles
- Sector Architecture
 - One 16KByte, two 8KBytes, one 32KByte, and fifteen 64kBytes (each chip)
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 1Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Boot Code Sector Architecture (Bottom)
- Low Power CMOS, 1.0mA Standby
- Embedded Erase and Program Algorithms
- Built-in Decoupling Caps for Low Noise Operation
- Erase Suspend/Resume
 - Supports reading data from or programming data to a sector not being erased
- Low Current Consumption
- Typical values at 5MHz:
 - 40mA Active Read Current
 - 80mA Program/Erase Current
- Weight
 - WF1M32B-XG2UX3 -8 grams typical
 - WF1M32B-XH1X3 -13 grams typical

Note: For programming information refer to Flash Programming 8M3 Application Note.

This product is subject to change without notice.

PIN CONFIGURATION FOR WF1M32B-XH1X3

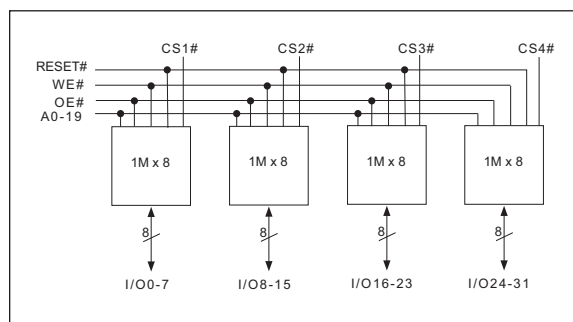
TOP VIEW

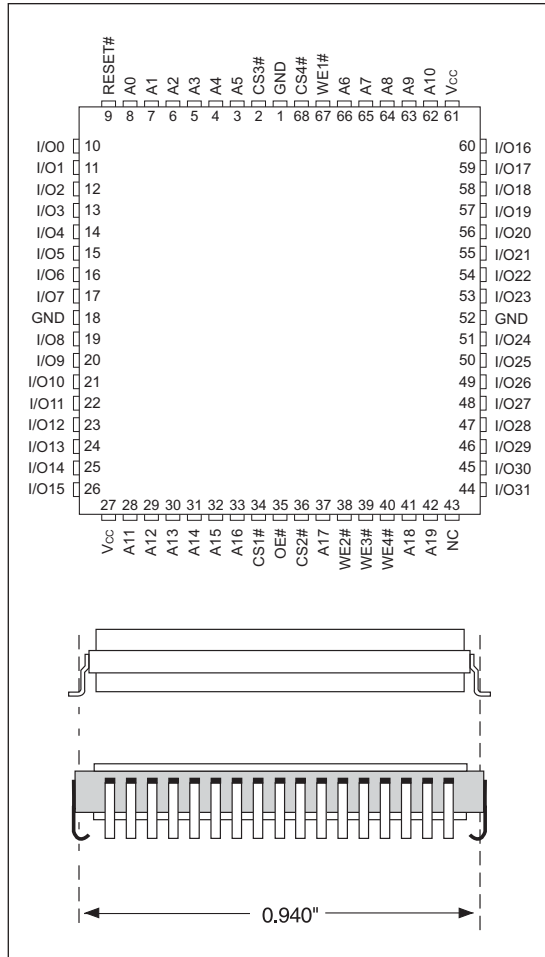


PIN DESCRIPTION

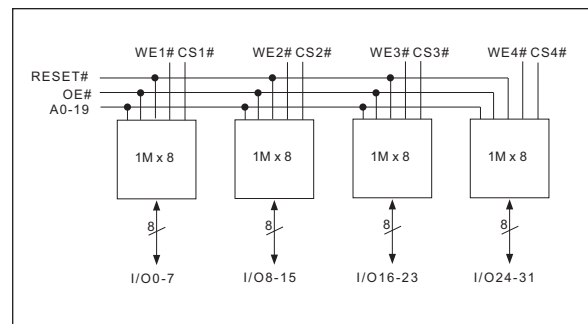
I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE#	Write Enable
CS1-4#	Chip Selects
OE#	Output Enable
RESET#	Reset
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



PIN CONFIGURATION FOR WF1M32B-XG2UX3
TOP VIEW

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE1-4#	Write Enables
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Vcc	Power Supply
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BLOCK DIAGRAM


The Microsemi 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature (M, Q)	-55 to +125	°C
Supply Voltage Range (V _{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to V _{CC} +0.5	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

 T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
WE1-4# capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	0.7 x V _{CC}	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS – CMOS COMPATIBLE

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = V _{CC MAX} , V _{IN} = GND or V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = V _{CC MAX} , V _{OUT} = GND or V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		120	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	CS# = V _{IL} , OE# = V _{IH}		140	mA
V _{CC} Standby Current	I _{CC3}	CS#, RESET# = V _{CC} ± 0.3V		200	μA
Output Low Voltage	V _{OL}	I _{OL} = 4.0 mA, V _{CC} = V _{CC MIN}		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.0 mA, V _{CC} = V _{CC MIN}	2.4		V
Low V _{CC} Lock-Out Voltage (3)	V _{LKO}		2.3	2.5	V

NOTES:

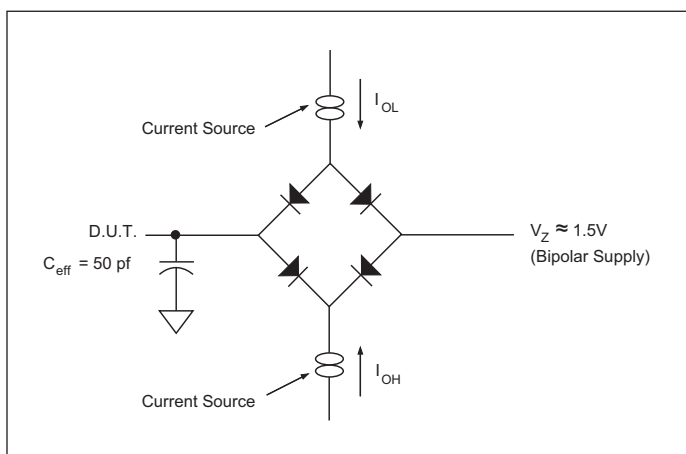
- The current listed as typically less than 8 mA/MHz, with OE# at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- Guaranteed by design, but not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	50		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	50		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	50		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μ s
Sector Erase Time	t_{WHWH2}			21		21		21	sec
Read Recovery Time (2)	t_{GHLEL}		0		0		0		μ s
Chip Programming Time				50		50		50	sec

NOTES:

1. Typical value for t_{WHWH1} is 9 μ s.
2. Guaranteed by design, but not tested.

AC TEST CIRCUIT

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

- V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	100		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	50		50		65		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	50		50		65		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	50		50		65		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase	t _{WHWH2}			15		15		15	sec
Read Recovery Time before Write (3)	t _{GHWL}		0		0		0		μs
Vcc Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time				50		50		50	sec
Output Enable Setup Time		t _{OES}	0		0		0		ns
Output Enable Hold Time (2)		t _{OEH}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 9μs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

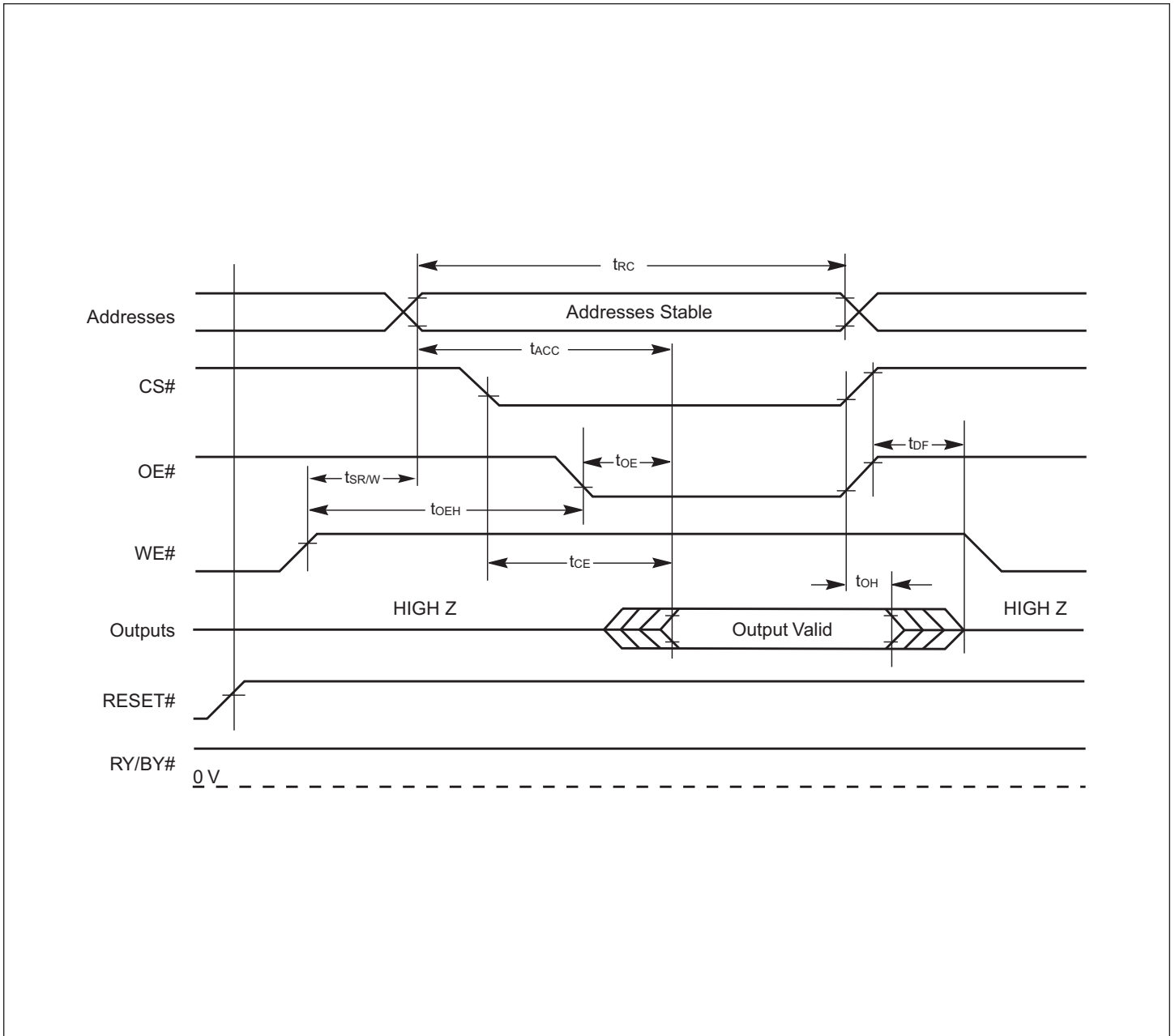
AC CHARACTERISTICS – READ-ONLY OPERATIONS

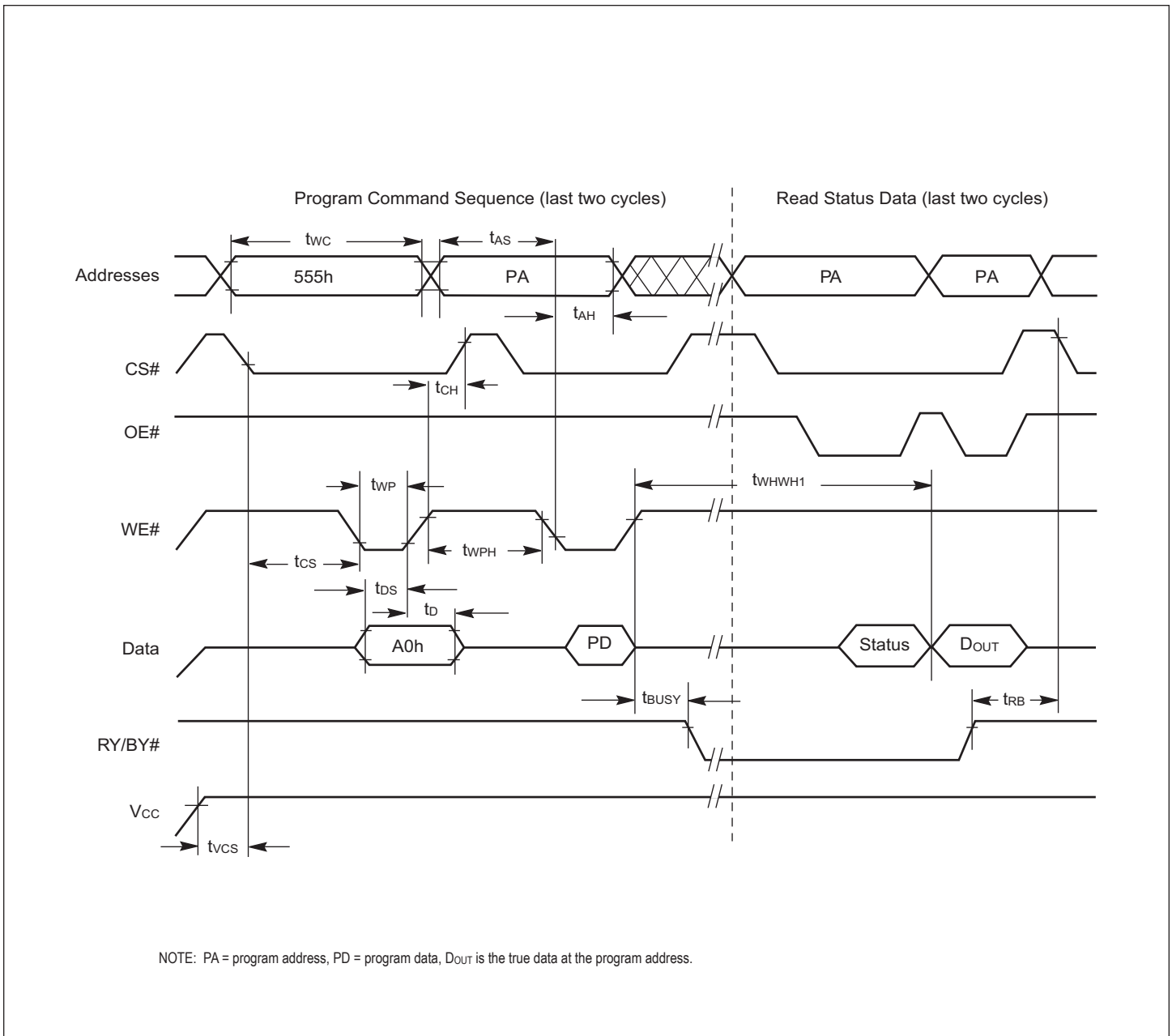
Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	100		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		100		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		100		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		30		30		40	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		30		30		40	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First (1)	t _{AXQX}	t _{OH}	0		0		0		ns

1. Guaranteed by design, not tested.



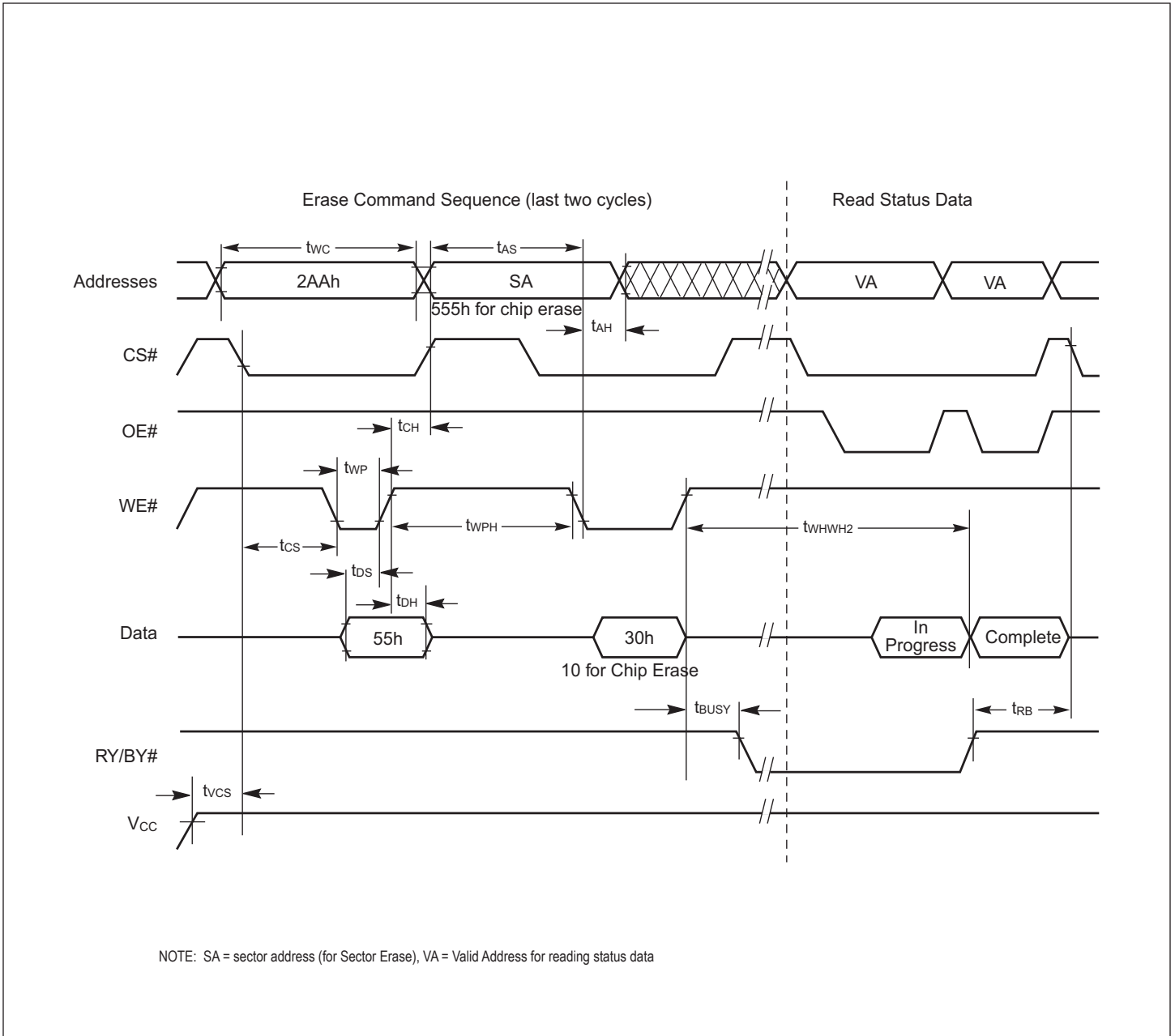
AC WAVEFORMS FOR READ OPERATIONS



WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED


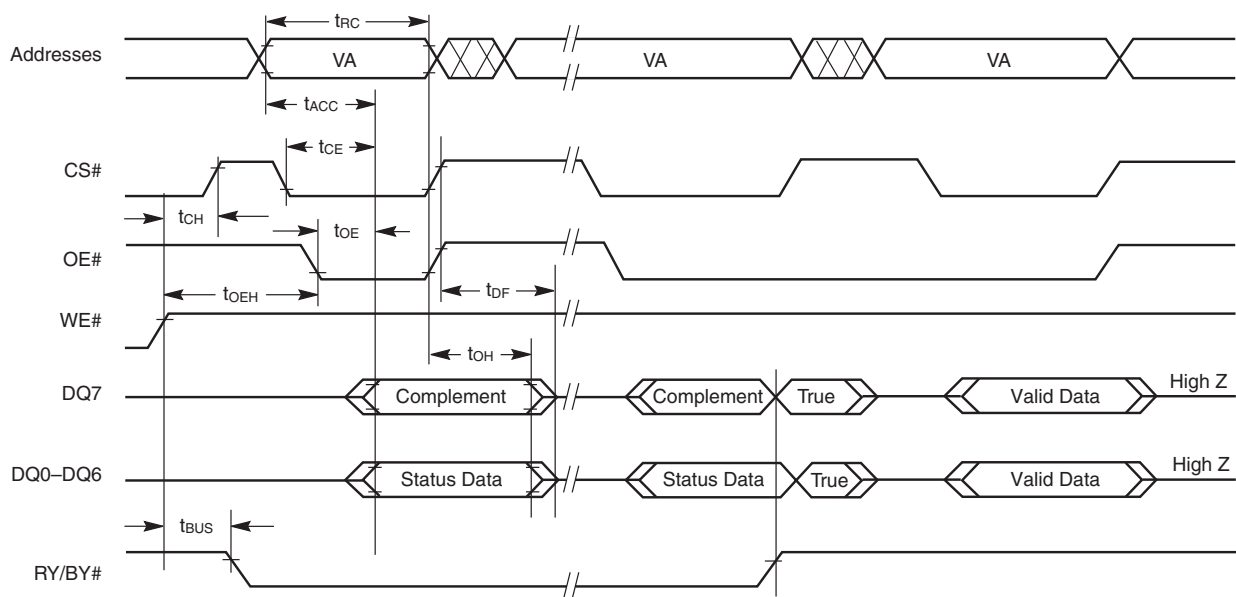


AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS





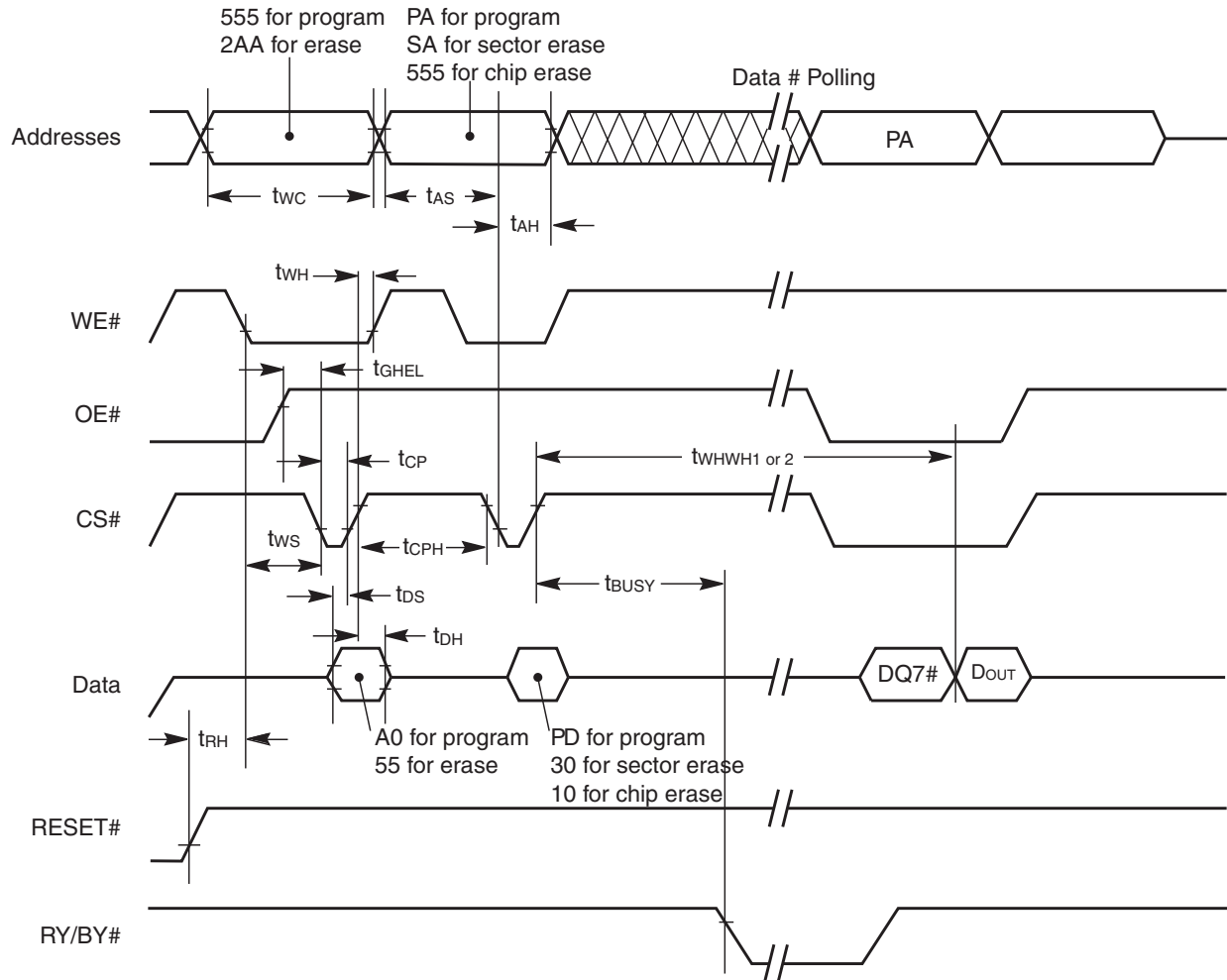
AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS



NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

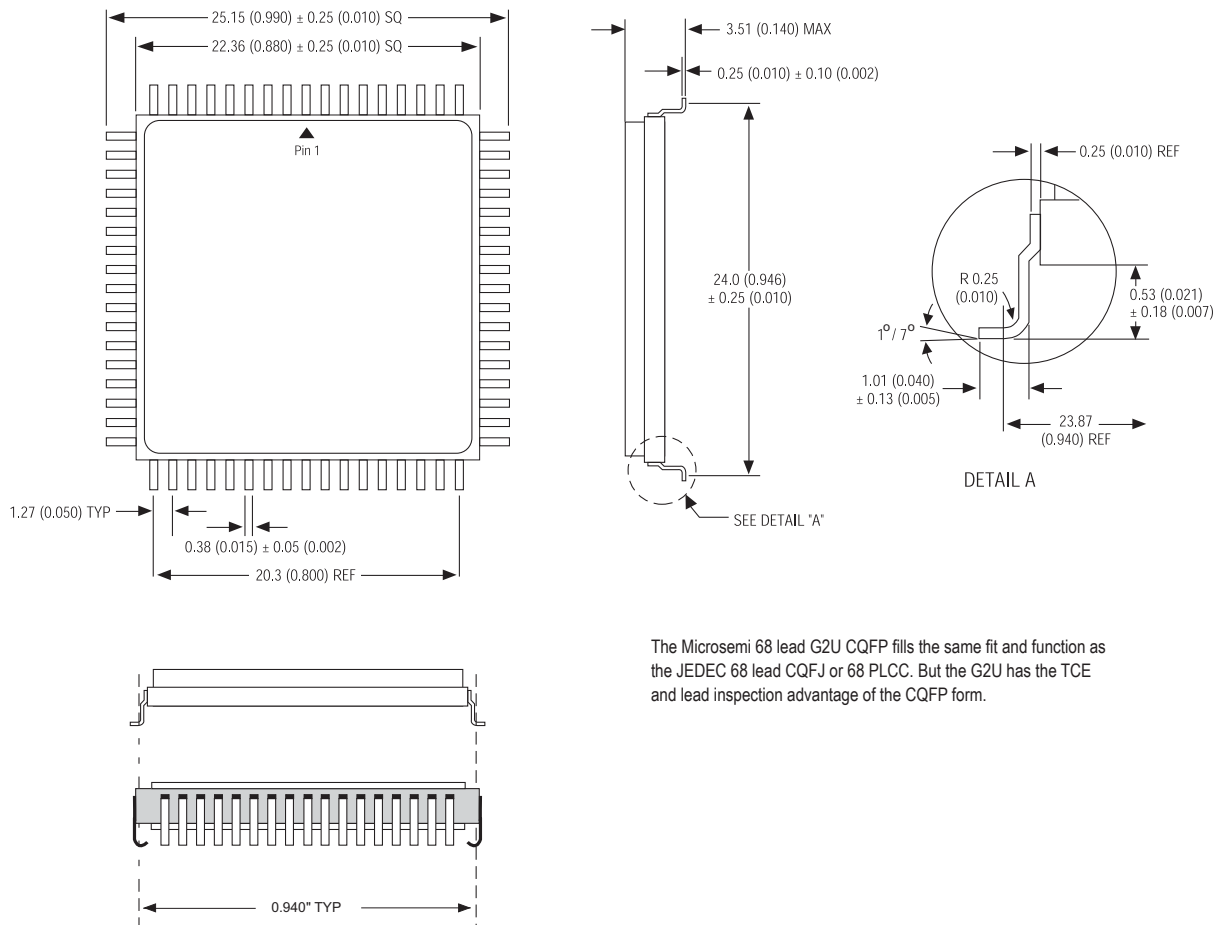


ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



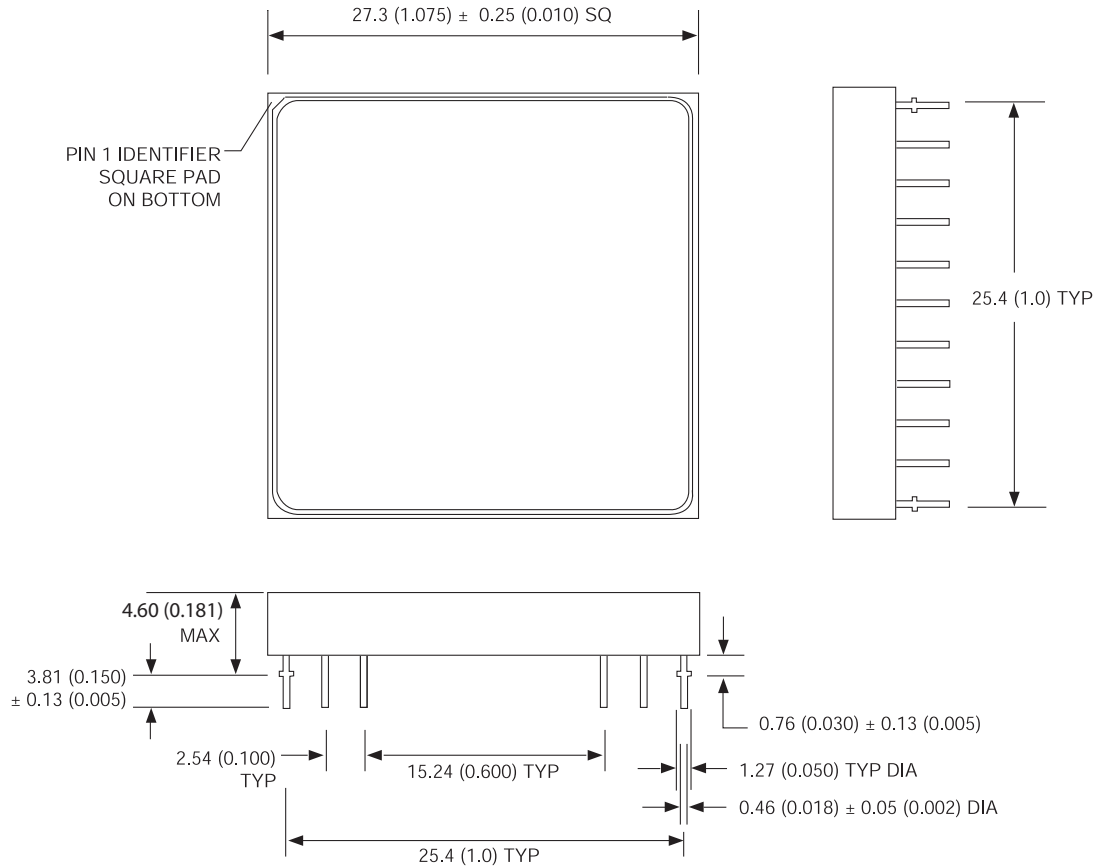
NOTES:

1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, DOUT = data written to the device.
2. Figure indicates the last two bus cycles of command sequence.

PACKAGE 510 – 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)


The Microsemi 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

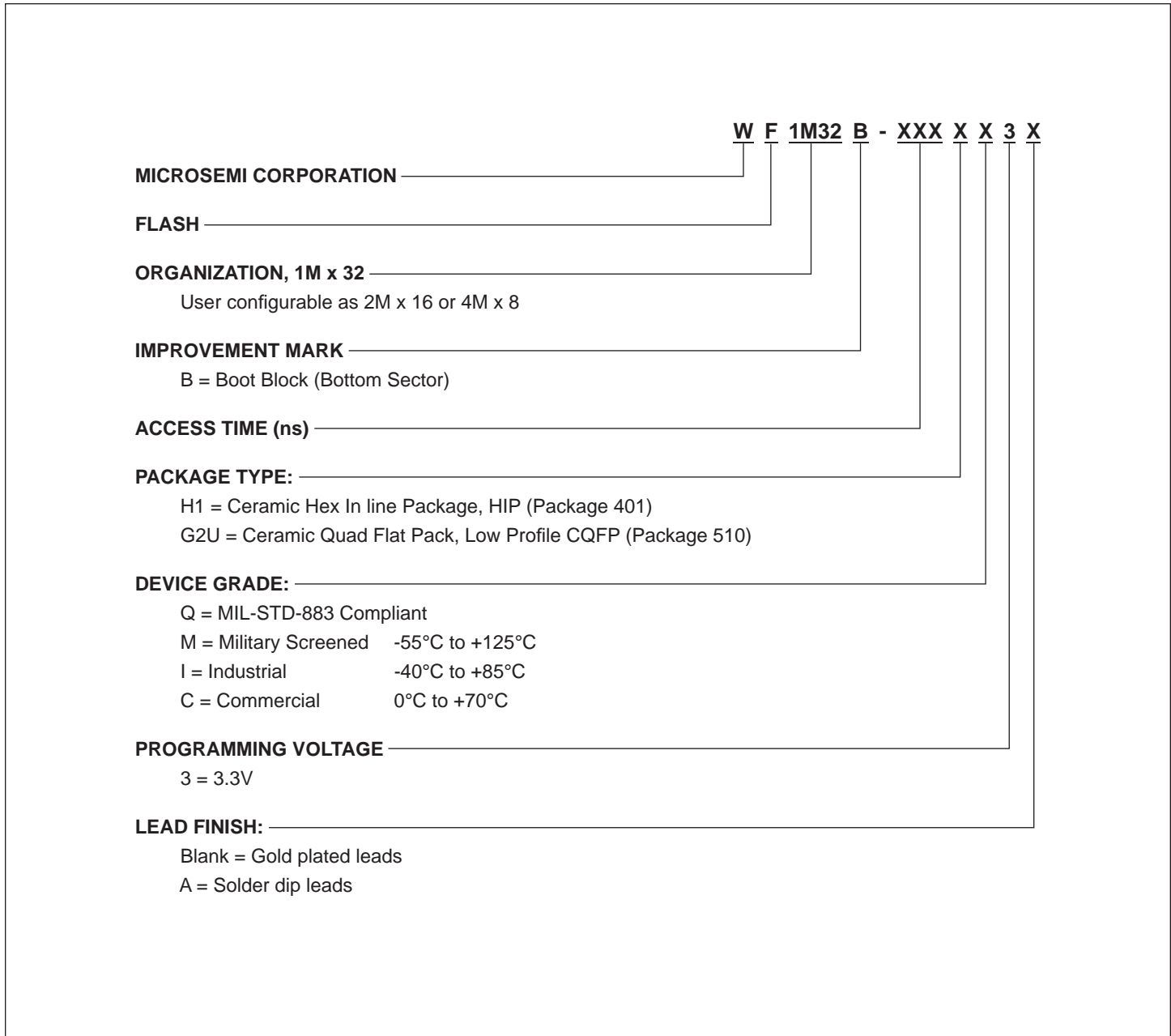
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION



Document Title

1Mx32 3.3V NOR FLASH MODULE

Revision History

Rev #	History	Release Date	Status
Rev 8	Changes (Pg. 1-14) 8.1 Change document layout from White Electronic Designs to Microsemi 8.2 Add document Revision History page	June 2011	Final
Rev 9	Changes (Pg. 1, 14) 9.1 Add "NOR" to headline	August 2011	Final
Rev 10	Changes (Pg. 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) 10.1 Change "in byte mote" to "each chip" in the first sub-bullet under Sector Architecture 10.2 Add "#" to WE1-4, CS1-4, OE and RESET in Pin Description on page 2 10.3 Add (M, Q) to Operation Temperature in Absolute Maximum Ratings chart 10.4 Add "#" to CS1-4 in Capacitance chart on page 3 10.5 Delete subhead from DC Characteristics – CMOS Compatible chart 10.6 Update DC Characteristics – CMOS Compatible chart 10.7 Update AC Characteristics chart...CS# Controlled 10.8 Update AC Characteristics chart...WE# Controlled 10.9 Update AC Characteristics chart...Read-Only Operations 10.10 Update AC Waveforms For Read Operations diagram 10.11 Update Write/Erase/Program Operation, WE# Controlled diagram 10.12 Update AC Waveforms Chip/Sector Erase Operations diagram 10.13 Update AC Waveforms For Data# Polling During Embedded Algorithm Operations diagram 10.14 Alternate CS# Controlled Programming Operation Timings	April 2012	Final