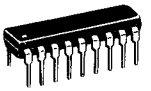
MOTOROLA

Advance Information

Integrated Pulse Dialer With Redial
Low-Power Silicon-Gate CMOS



P SUFFIX
PLASTIC
CASE 707

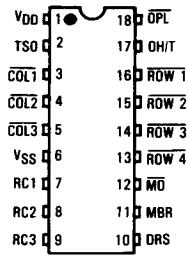
The MC145409 is a monolithic CMOS integrated circuit which converts 2-of-7 keyboard inputs into pulse signals that simulate a rotary telephone dialer. All of the features necessary for implementing a pulse dialer are provided, as well as redial. It uses an inexpensive RC oscillator, operates directly off telephone line supply, and consumes only microamperes of current when not outpulsing.

When off hook, the oscillator is enabled when a valid key input is detected. The MC145409 senses key depressions, verifies that a single key is depressed, and stores the key's code in on-chip memory. Up to 17 digits can be stored in the redial memory. After a predigital pause while memory is cleared, outpulsing begins and continues until the last entered digit is outpulsed. If the receiver has been on-hook for the minimum time, redial can be initiated by pressing either * or #.

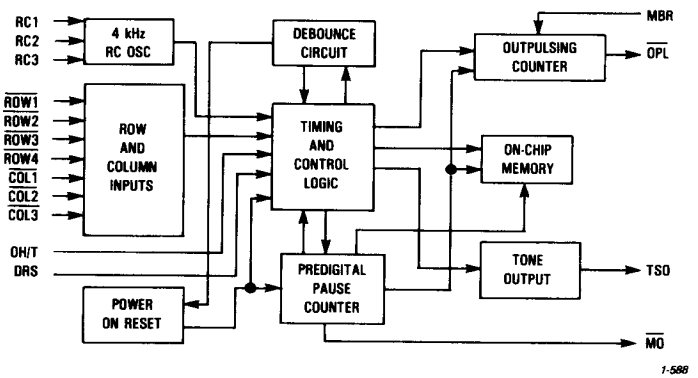
When on-hook the oscillator is disabled, preventing excessive current draw. In this condition, key inputs will not be recognized.

- Direct Telephone Line Operation
- Silicon Gate CMOS Technology for Low-Power Operation
- 2.5 to 6.0 Volt Supply Range
- Selectable Make-Break Ratio (60% or 66%)
- Selectable Dialing Rate (10 pps or 20 pps)
- Continuous Mute
- Tone Signal Output
- Memory Redial with * or #
- Inexpensive RC Oscillator
- Uses Standard 2-of-7 Matrix with Negative Common or the Inexpensive Class-A Type Keyboard
- Pin Compatible with LR-40993

PIN ASSIGNMENTS



BLOCK DIAGRAM



1-586

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ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	−0.3 to +6.0	V
Operating Temperature	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	500	mW
Voltage On Any Pin Relative to V_{SS}	V_{in1}	−0.3	V
On Any Pin Relative to V_{DD}	V_{in2}	+0.3	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
DC Supply Voltage (V_{SS} = 0 V)		V_{DD}	2.5	—	6.0	V
Operating Current (Off Hook, No Load on Outputs)		I_{DD}				μA
After Key Depression (During Outpulsing)	V_{DD} = 2.5 V		—	30	—	
	V_{DD} = 6.0 V		—	100	150	
During Key Depression	V_{DD} = 2.5 V		—	65	—	
	V_{DD} = 6.0 V		—	200	270	
Stand-by Current	V_{DD} = 2.5 V	I_{SB}	—	200	—	μA
(Off-Hook, Oscillator Disabled)	V_{DD} = 6.0 V		—	4.5	6.0	
Memory Retention Current (On-Hook)		—	—	5.0	10.0	nA
Input Voltage	"0" level	V_{IL}	—	20% of V_{DD}	—	V
MBR, DRS, OH/T, and Key Inputs (2-of-7 input mode)	"1" level	V_{IH}	—	80% of V_{DD}	—	
Keyboard Pull-up Resistance, $\overline{COL}$ 1-3, $\overline{ROW}$ 1-4		—	—	TBD	—	kΩ
Keyboard Pull-down Resistance, $\overline{COL}$ 1-3, $\overline{ROW}$ 1-4		—	—	TBD	—	kΩ
Mute Sink Current, $\overline{MO}$	V_{DD} = 2.5 V	—	500	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Pulse Output Sink Current, $\overline{OPL}$	V_{DD} = 2.5 V	—	1.0	—	—	mA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Tone Output Sink Current, TSO	V_{DD} = 2.5 V	—	250	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Tone Output Source Current, TSO	V_{DD} = 2.5 V	—	250	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Mute or Pulse Off Leakage Current, MBR, $\overline{OPL}$	V_{DD} = 2.5 V	—	—	TBD	—	μA
($V_{out} \approx V_{DD}$)	V_{DD} = 6.0 V		—	0.001	1.0	
Key Contact Resistance		—	—	—	1	kΩ
Keyboard Capacitance		—	—	—	30	pF

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AC CHARACTERISTICS (T_A = 25°C, V_{DD} = 2.5 to 6.0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Clock Frequency		f_{CL}	–	4	–	kHz
Frequency Stability		–	–	±4	–	%
Clock Start-Up Time		t_{CL}	–	1	–	ms
Tone Frequency*	DRS = V_{SS}	–	–	1	–	kHz
	DRS = V_{DD}		–	2	–	
Percent Make-Break Ratio	MBR = V_{DD}	%MBR	–	66	–	%
	MBR = V_{SS}		–	60	–	
Outpulsing Rate*	DRS = V_{SS}	f_{OPL}	–	10	–	pps
	DRS = V_{DD}		–	20	–	
Pre-Digital Pause*	f_{OPL} = 10 pps	t_{PDP}	–	900	–	ms
	f_{OPL} = 20 pps		–	450	–	
Inter-Digit Time*	f_{OPL} = 10 pps	t_{ID}	–	900	–	ms
	f_{OPL} = 20 pps		–	450	–	
Key Input Debounce Time*		t_{DB}	–	10	–	ms
Key Down Time for Valid Entry*		–	–	40	–	ms
Key Down Time for Two Key Rollover*		–	–	5	–	ms
On-Hook Time Required to Clear Memory*		–	300	–	–	ms
Mute Valid After Last Outpulse*		t_{MO}	–	5	–	ms

*Directly proportional to oscillator frequency. Parameters for f_{CL} = 4 kHz

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 1)

Positive power, relative to V_{SS} can be supplied from regulated line power.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 6)

Negative power, relative to V_{DD}

DRS, DIALING RATE SELECT (PIN 10)

When Pin 10 is tied to V_{SS} an output pulse rate of 10 pulse-per-second is selected. Tying Pin 10 to V_{DD} selects 20 pulse-per-second.

MBR, MAKE-BREAK RATIO (PIN 11)

The make-break ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output as shown.

Make-Break Ratio (MBR)	Make	Break
V_{SS} (Pin 6)	40%	60%
V_{DD} (Pin 1)	34%	66%

$\overline{OPL}$, OUTPULSING (PIN 18)

The $\overline{OPL}$ output is an N-channel transistor in an open drain configuration designed to drive a bipolar transistor. This output pulls to V_{SS} during break and is open circuited during make.

$\overline{MO}$, MUTE OUTPUT (PIN 12)

The $\overline{MO}$ output is an N-channel transistor in an open drain configuration designed to drive a bipolar transistor. This output pulls to V_{SS} at the beginning of the predigital pause and remains there until the last digit is outpulsed. When not muting, this output is an open circuit.

TSO, TONE SIGNAL OUTPUT (PIN 2)

A tone signal is generated in response to a key depression for user feedback. The TSO pin is a CMOS output capable of driving an external bipolar transistor. The tone frequency is 1 kHz when a 10 pulse-per-second rate is selected and 2 kHz when 20 pulse-per-second is selected.

OH/T, ON-HOOK/TEST (PIN 17)

Connecting the OH/T pin to V_{SS} sets the MC145409 in the normal or off-hook mode. Allowing the pin to float or connecting it to V_{DD} selects the test mode.

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KEYBOARD INPUTS (PINS 3, 4, 5, 13, 14, 15, 16)

The keyboard inputs allow either a single contact (Class A) keyboard, or a standard 2-of-7 keyboard with negative common. A valid key entry occurs when either a single row is connected to a single column, or a single row and column are simultaneously connected to V_{SS}. Figure 1 shows typical keyboard configurations.

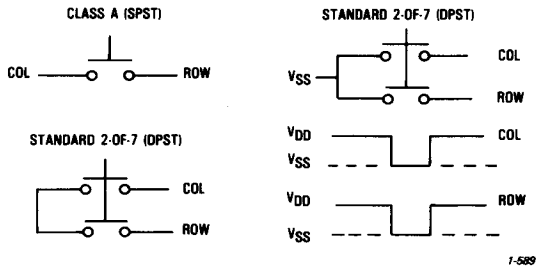
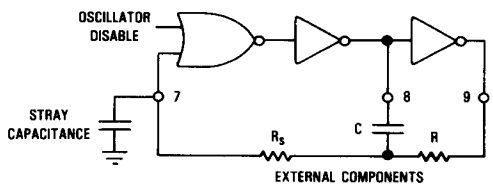


Figure 1. Keyboard Configuration

OSCILLATOR (PINS 7, 8, 9)

The MC145409 contains on-chip oscillator circuitry which will function with a minimum of external components. The oscillator is disabled when the circuit is idle. The circuit shown in Figure 2 will cause oscillation at 4 kHz with Rs = 2 MΩ, R = 220 kΩ, and C = 390 pF.



NOTE:
Minimizing the stray capacitance on pin 7 will enhance oscillator stability. The oscillator disable feature is internal to the device.

1-590

Figure 2. Oscillator Configuration

GENERAL DEVICE DESCRIPTION

When the MC145409 is on-hook, the row and column inputs are held high and keyboard entry is not accepted. A transition to off-hook resets the timing and control logic and the predigital pause counter. When in the off-hook mode, the keyboard remains static until a keyboard entry is sensed. This enables the oscillator. The row and column inputs are alternately scanned (by pulling high then low) to confirm input validity. The input is accepted only after it remains valid for 10 milliseconds of debounce time.

Once an input is accepted, the digit is stored in memory and outpulsing begins. The $\overline{OPL}$ output sends bursts of pulses equivalent to the digits of a telephone number stored in memory. This output drives an external bipolar transistor used to pulse the telephone line by momentarily connecting and disconnecting the speech network from line power.

During outpulsing, the $\overline{MO}$ output mutes the receiver, isolating it from the outpulsing transients.

When off-hook, the MC145409 accepts key inputs and functions in a normal fashion. After outpulsing the last digit, the oscillator is disabled and the circuit goes to a standby mode. If the MC145409 is switched to on-hook while outpulsing, the remaining digits are outpulsed at 100 times their normal rate,

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with a make-break ratio of 50/50 to facilitate testing. This is also an efficient means of resetting the circuit. Outpulsing in this mode can take up to 300 milliseconds, and when complete, the circuit is deactivated, drawing only enough current to sustain memory and the power-up-clear detect circuitry.

Returning to off-hook causes a positive transition on the mute output insuring connection of the speech network to the line. An initial key entry of # or * causes the number sequence stored in on-chip memory to be outpulsed. Pressing any other valid key clears memory, and the new number sequence will be outpulsed.

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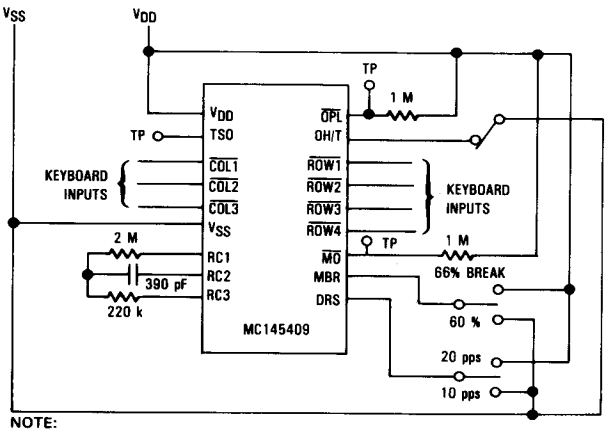

NOTE:
This circuit demonstrates operation of the device. Outputs can be observed at testpoints.

1-591

Figure 3. Evaluation Circuit

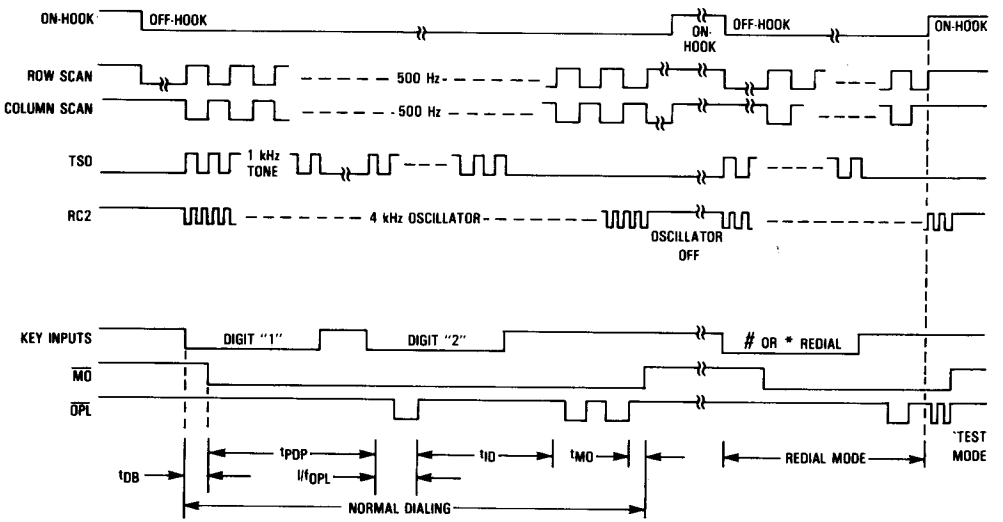

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Figure 4. Timing Diagram

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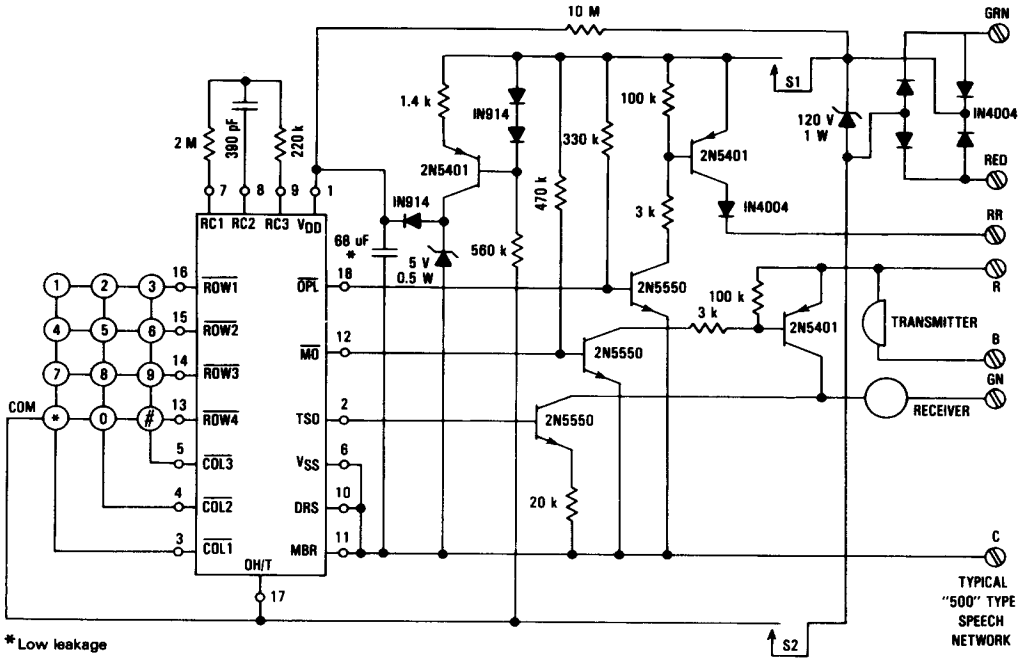

Figure 5. Telephone Dialer Application Circuit

1-593

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