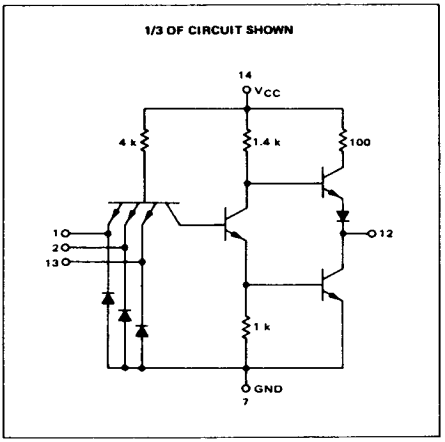
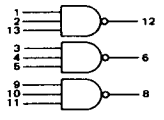
TRIPLE 3-INPUT "NAND" GATE

MC5410L *
MC7410P,L*



This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



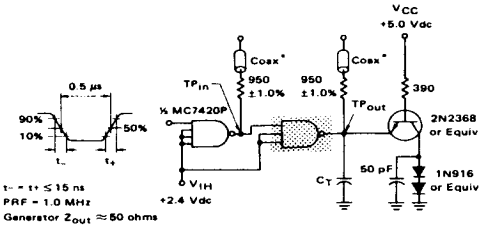
Positive Logic: $12 = \overline{1 + 2 + 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 13 ns typ

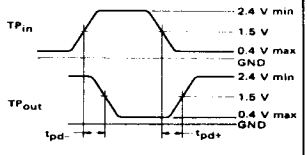
*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

SWITCHING TIME TEST CIRCUIT



$t_- = t_+ \leq 15$ ns
PRF = 1.0 MHz
Generator $Z_{out} \approx 50$ ohms

VOLTAGE WAVEFORMS AND DEFINITIONS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

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ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts										
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	
MC5410	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5	
MC7410	16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC5410 Test Limits −55 to +125°C Min	Max	Unit	MC7410 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_F	1	-	-1.6	mAdc	-	-1.6	mAdc	-	-	1	-	-	2,13	-	-	-	-	-	14	7*
Leakage Current	I_{R1}	1	-	40	µAdc	-	40	µAdc	-	-	-	1	-	-	-	-	-	-	-	14	2,7,13*
	I_{R2}	1	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	1	-	-	-	-	-	-	14	2,7,13*
Output																					
Output Voltage	V_{OL}	12	-	0.4	Vdc	-	0.4	Vdc	12	-	-	-	-	-	-	1,2,13	-	-	14	-	7*
	V_{OH}	12	2.4	-	Vdc	2.4	-	Vdc	-	12	-	-	-	2,13	-	-	1	-	14	-	7*
Short-Circuit Current	I_{SC}	12	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,2,7,12,13*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PDH}	14	-	15.3	mAdc	-	15.3	mAdc	-	-	-	-	-	-	1,2,3,4,5, 9,10,11,13	-	-	14	-	-	7
	I_{PDL}	14	-	5.4	mAdc	-	5.4	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	1,2,7,13*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,12	-	15**	ns	-	15**	ns	1	12	-	2,13	-	-	-	-	-	14	-	-	7*
Turn-Off Delay	t_{pd-}	1,12	-	29**	ns	-	29**	ns	1	12	-	2,13	-	-	-	-	-	14	-	-	7*

*Ground inputs to gates not under test.
**Tested only at 25°C.