



74HC4511; 74HCT4511

BCD to 7-segment latch/decoder/driver

Rev. 4 — 28 March 2024

Product data sheet

1. General description

The 74HC4511; 74HCT4511 is a BCD to 7-segment latch/decoder/driver with four address inputs (A, B, C, D), a latch enable input ($\overline{LE}$), a ripple blanking input ($\overline{BI}$), a lamp test input ($\overline{LT}$), and seven segment outputs (a to g). When $\overline{LE}$ is LOW, the state of the segment outputs (a to g) is determined by the data on A to D. When $\overline{LE}$ goes HIGH, the last data present on A to D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

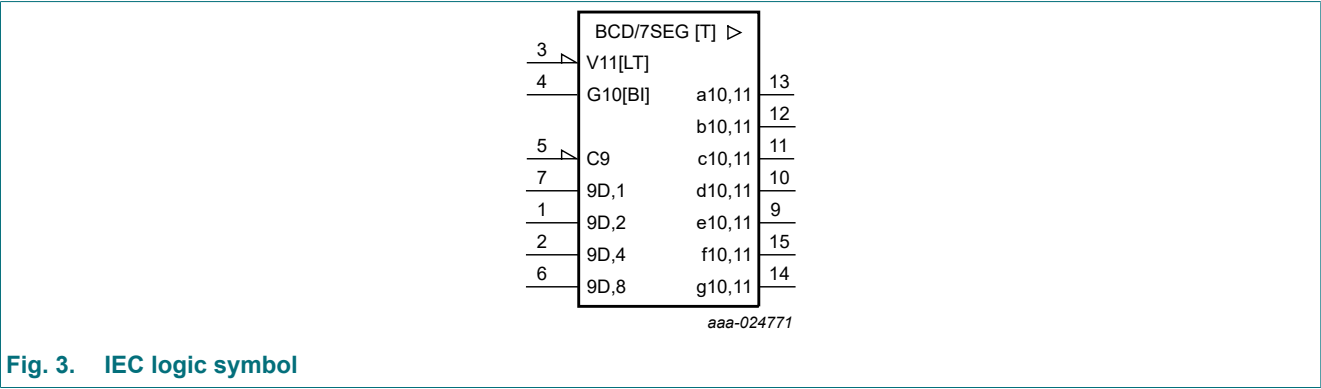
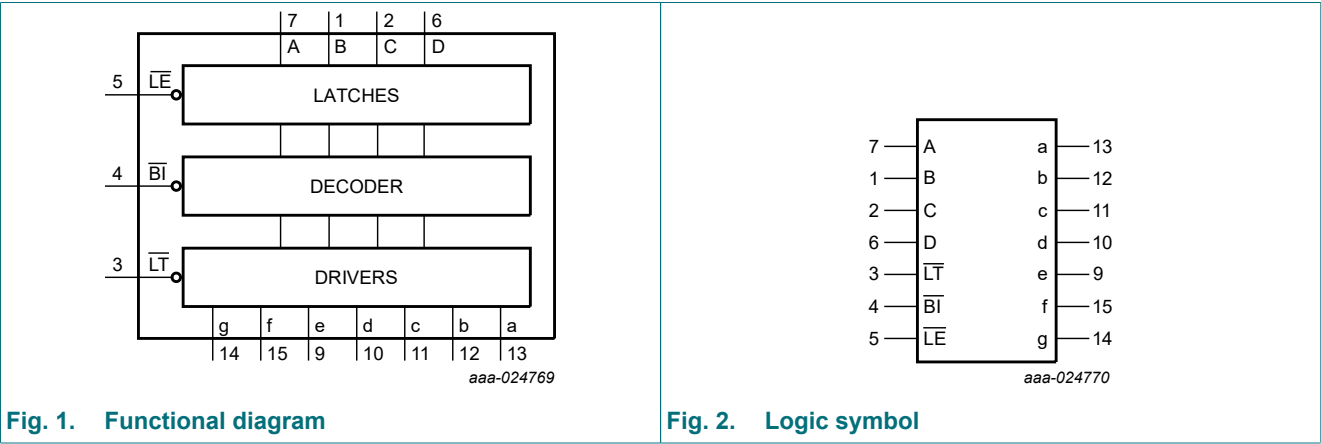
- Complies with JEDEC standard no. 7A
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC4511: CMOS level
 - For 74HCT4511: TTL level
- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4511D 74HCT4511D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram



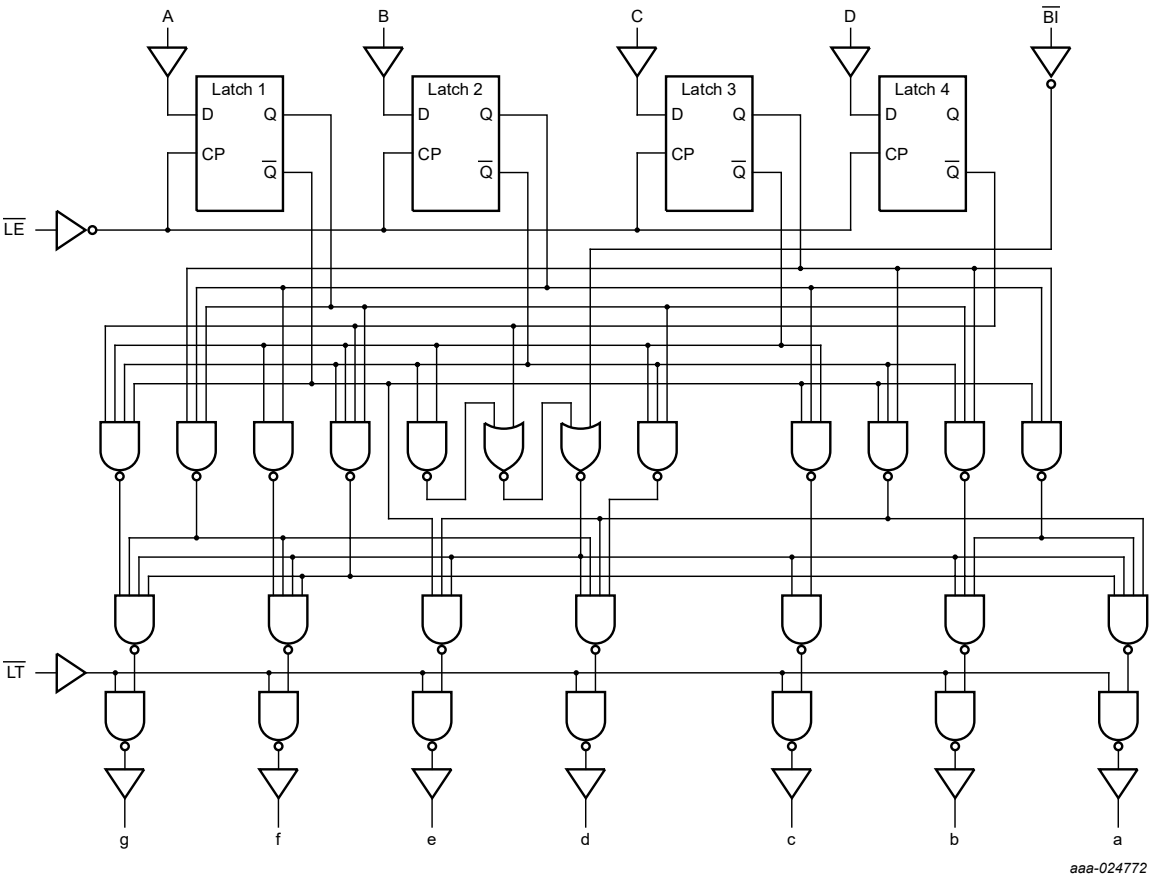
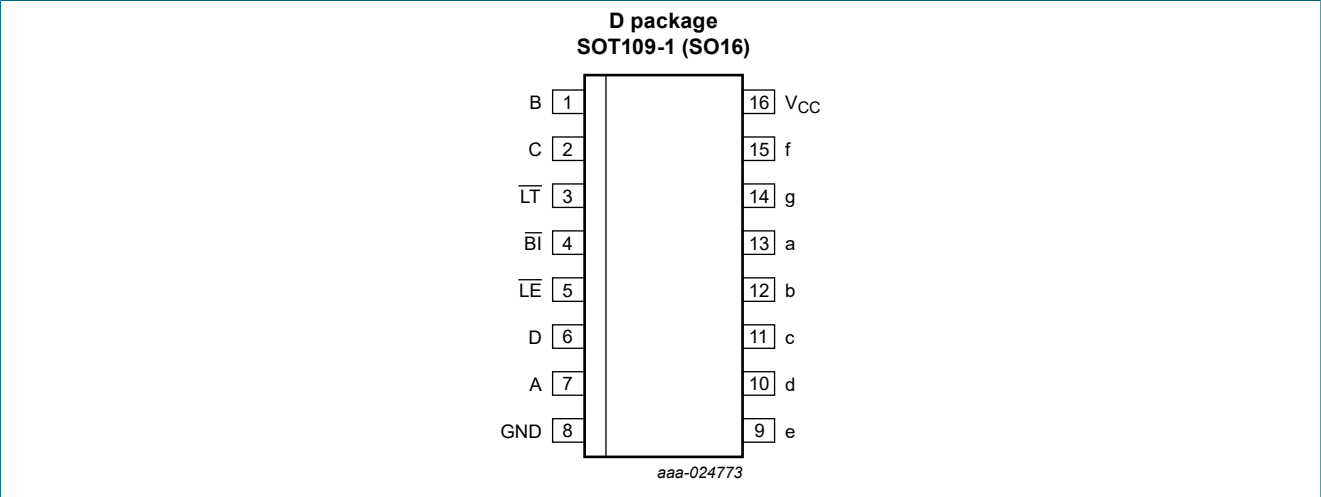


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{LT}$	3	lamp test input (active LOW)
$\overline{BI}$	4	ripple blanking input (active low)
$\overline{LE}$	5	latch enable input (active low)
A, B, C, D	7, 1, 2, 6	BCD address inputs
GND	8	ground (0 V)
a, b, c, d, e, f, g	13, 12, 11, 10, 9, 15, 14	segments outputs
V_{CC}	16	supply voltage

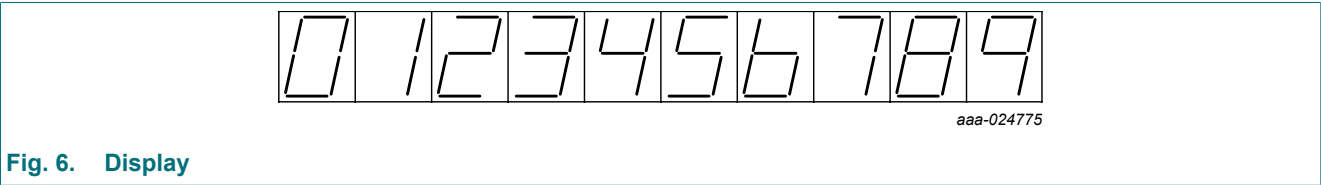
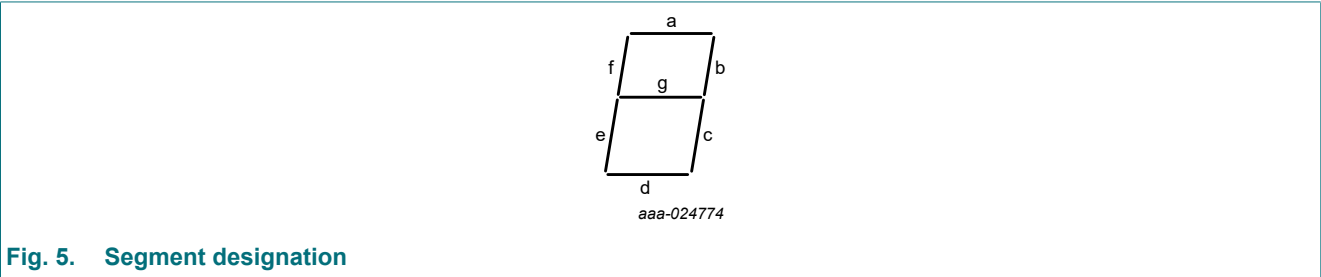
6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs							Outputs							Display
LE	B $\overline{\text{I}}$	LT	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	[1]							[1]

[1] Depends upon the BCD-code applied during the LOW-to-HIGH transition of LE.



7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	SO16 package [1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4511			74HCT4511			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4511										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -7.5 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = -10 mA; V _{CC} = 4.5 V	3.6	-	-	3.35	-	3.1	-	V
		I _O = -7.5 mA; V _{CC} = 6.0 V	5.6	-	-	5.45	-	5.35	-	V
		I _O = -10 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4511										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -7.5 mA	3.98	-	-	3.84	-	3.7	-	V
		I _O = -10 mA	3.6	-	-	3.35	-	3.1	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND								
		LT, LE inputs	-	150	540	-	675	-	735	µA
		B̄I, A, B, C, D inputs	-	30	108	-	135	-	147	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4511										
t _{pd}	propagation delay	A-D to a-g; see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	77	300	-	375	-	450	ns
		V _{CC} = 4.5 V	-	28	60	-	75	-	90	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	24	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	22	51	-	64	-	77	ns
		LE to a-g; see Fig. 8								
		V _{CC} = 2.0 V	-	74	270	-	330	-	405	ns
		V _{CC} = 4.5 V	-	27	54	-	68	-	81	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	23	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	22	46	-	58	-	69	ns
		BI to a-g; see Fig. 9								
		V _{CC} = 2.0 V	-	61	220	-	275	-	330	ns
		V _{CC} = 4.5 V	-	22	44	-	55	-	66	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	18	37	-	47	-	56	ns
		LT to a-g; see Fig. 7								
		V _{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	26	-	33	-	38	ns
t _t	transition time	see Fig. 7 , Fig. 8 and Fig. 9 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _W	pulse width	LE LOW; see Fig. 8								
		V _{CC} = 2.0 V	80	11	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	3	-	17	-	20	-	ns
t _{su}	set-up time	A-D to LE; see Fig. 10								
		V _{CC} = 2.0 V	60	14	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	4	-	13	-	15	-	ns
t _h	hold time	A-D to LE; see Fig. 10								
		V _{CC} = 2.0 V	0	-11	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-4	-	0	-	0	-	ns
		V _{CC} = 6.0 V	0	-3	-	0		0	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 5 V; f _i = 1 MHz [3]	-	64	-	-	-	-	-	pF
74HCT4511										
t _{pd}	propagation delay	A-D to a-g; see Fig. 7 [1]								
		V _{CC} = 4.5 V	-	28	60	-	75	-	90	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	24	-	-	-	-	-	ns
		LE to a-g; see Fig. 8								
		V _{CC} = 4.5 V	-	27	54	-	68	-	81	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	24	-	-	-	-	-	ns
		B $\bar{I}$ to a-g; see Fig. 9								
		V _{CC} = 4.5 V	-	23	44	-	55	-	66	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		LT to a-g; see Fig. 7								
		V _{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
t _t	transition time	see Fig. 7, Fig. 8 and Fig. 9 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	LE LOW; see Fig. 8								
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
t _{su}	set-up time	A-D to LE; see Fig. 10								
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
t _h	hold time	A-D to LE; see Fig. 10								
		V _{CC} = 4.5 V	0	-4	-	0	-	0	-	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} - 1.5 V; V _{CC} = 5 V; f _i = 1 MHz [3]	-	64	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ(C_L × V_{CC}² × f_o) = sum of outputs.

10.1. Waveforms and test circuit

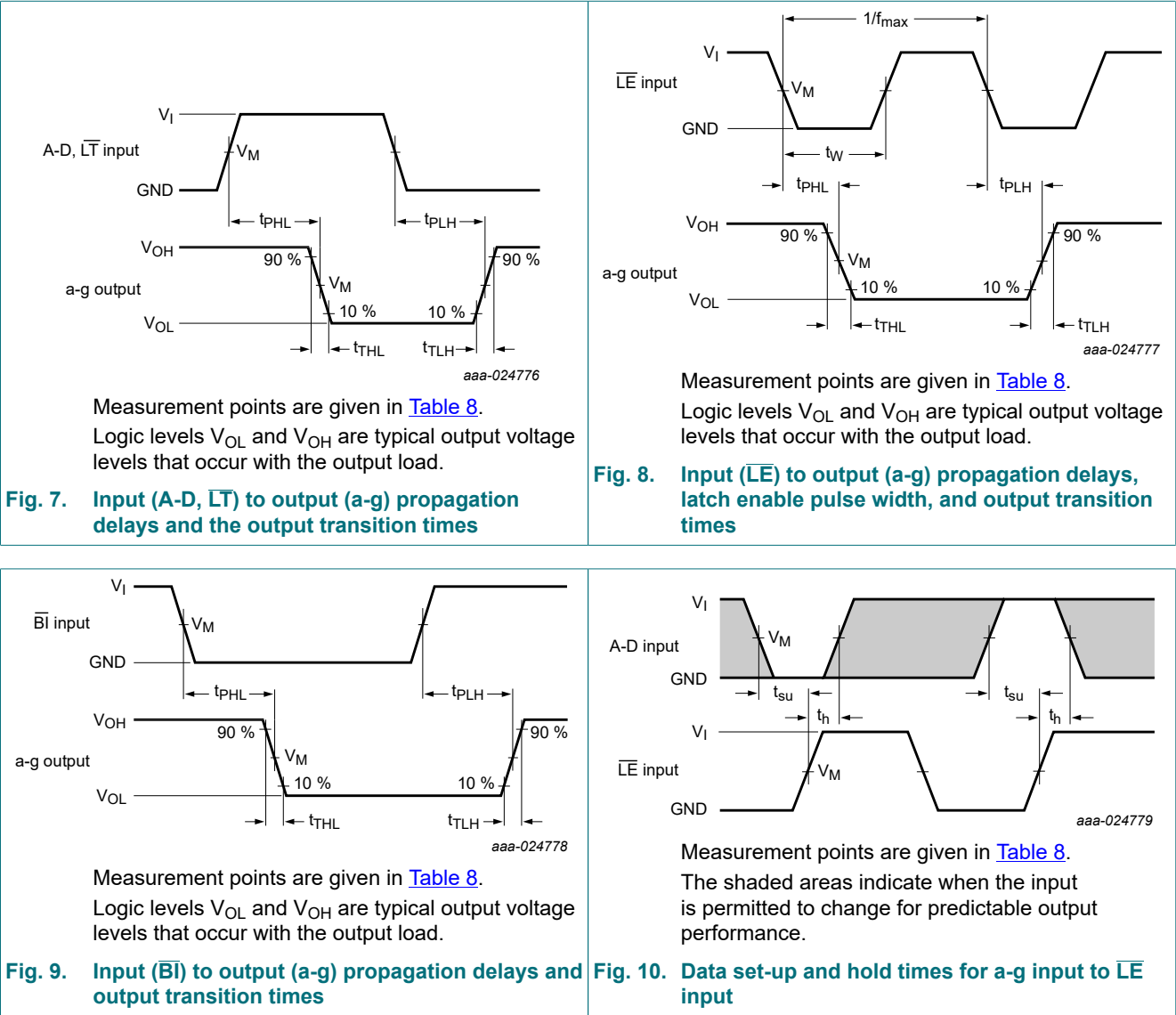
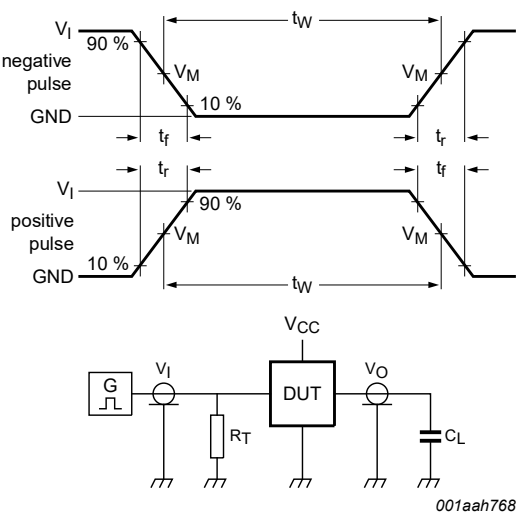


Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC4511	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT4511	1.3 V	GND to 3 V	1.3 V



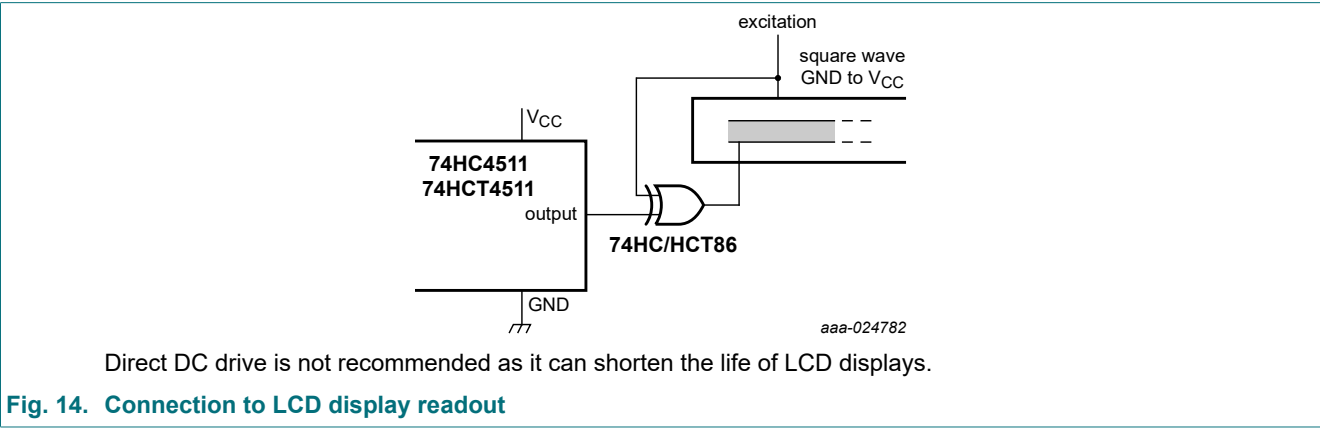
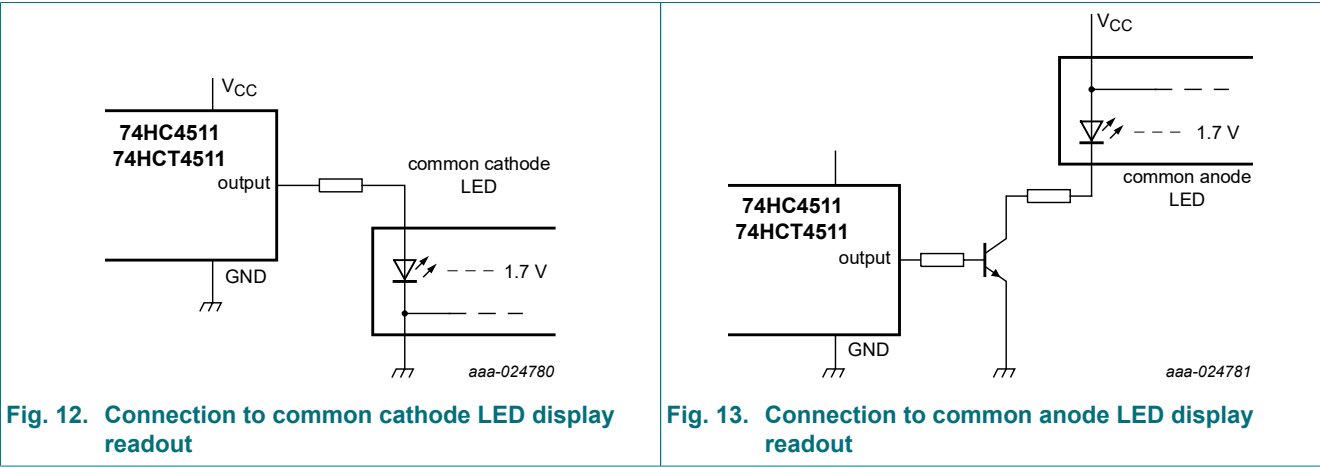
Test data is given in [Table 9](#).
Test circuit definitions:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
 C_L = Load capacitance including jig and probe capacitance;

Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC4511	V_{CC}	6 ns	15 pF, 50 pF	t_{PHL}, t_{PLH}
74HCT4511	3 V	6 ns	15 pF, 50 pF	t_{PHL}, t_{PLH}

11. Application information



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

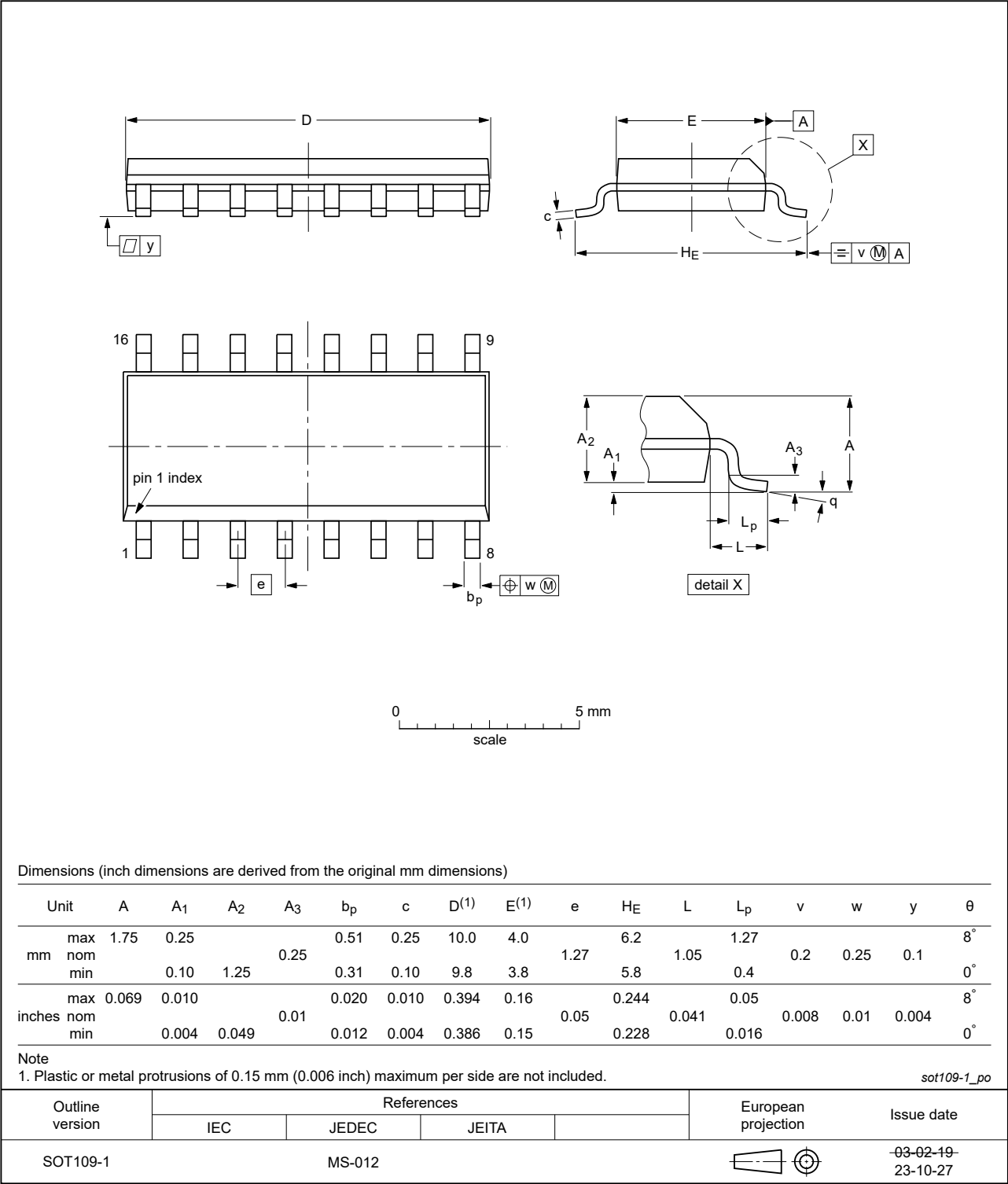


Fig. 15. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4511 v.4	20240328	Product data sheet	-	74HC_HCT4511 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 2: ESD specification updated according to the latest JEDEC standard. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 11 and Table 9 aligned with specification (errata). Fig. 15: Aligned SO package outline drawing to JEDEC MS-012			
74HC_HCT4511 v.3	20161115	Product data sheet	-	74HC_HCT4511 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74HC4511N, 74HCT4511N removed.			
74HC_HCT4511 v.2	19901201	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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