

74HC377; 74HCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 6 — 5 August 2024

Product data sheet

1. General description

The 74HC377; 74HCT377 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and data enable ($\bar{E}$) inputs. When $\bar{E}$ is LOW, the outputs Qn assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. Input $\bar{E}$ must be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Input levels:
 - For 74HC377: CMOS level
 - For 74HCT377: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC377D 74HCT377D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC377PW 74HCT377PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

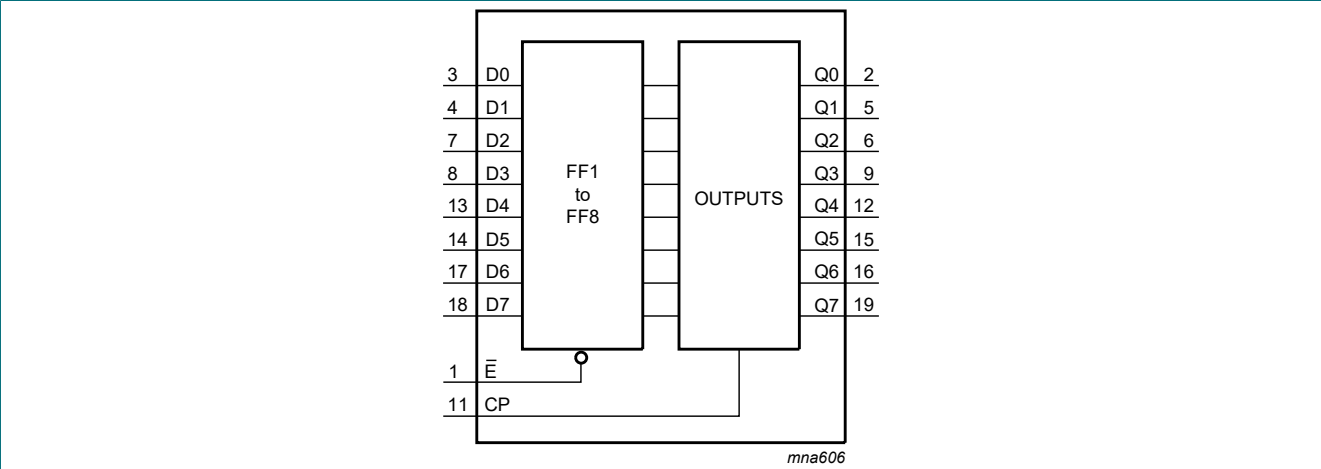


Fig. 1. Functional diagram

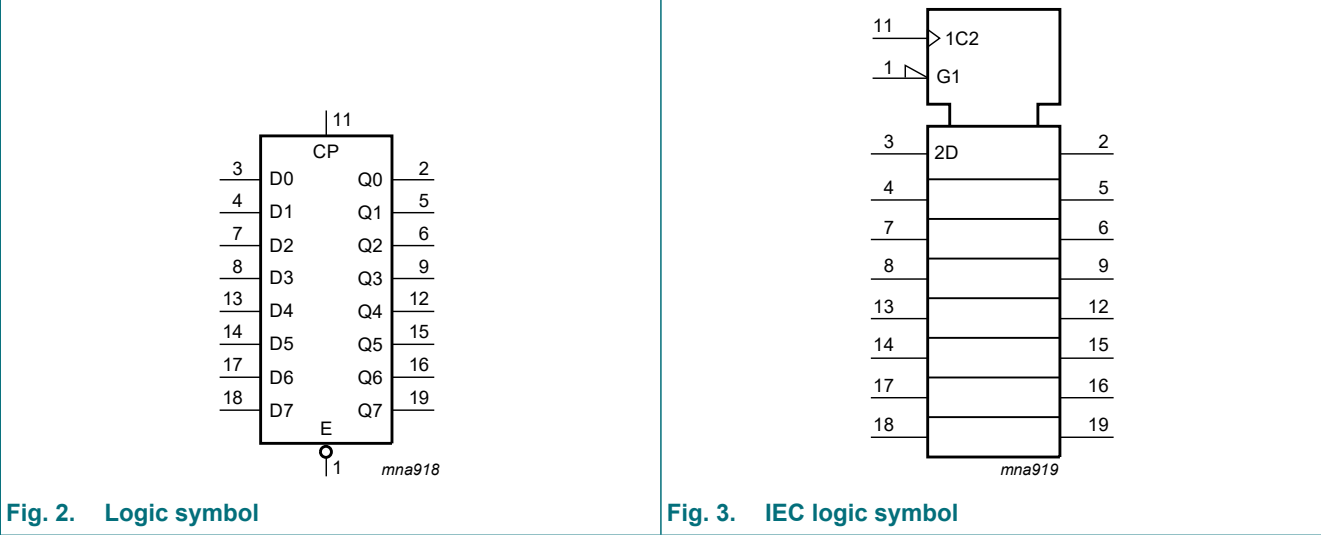


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

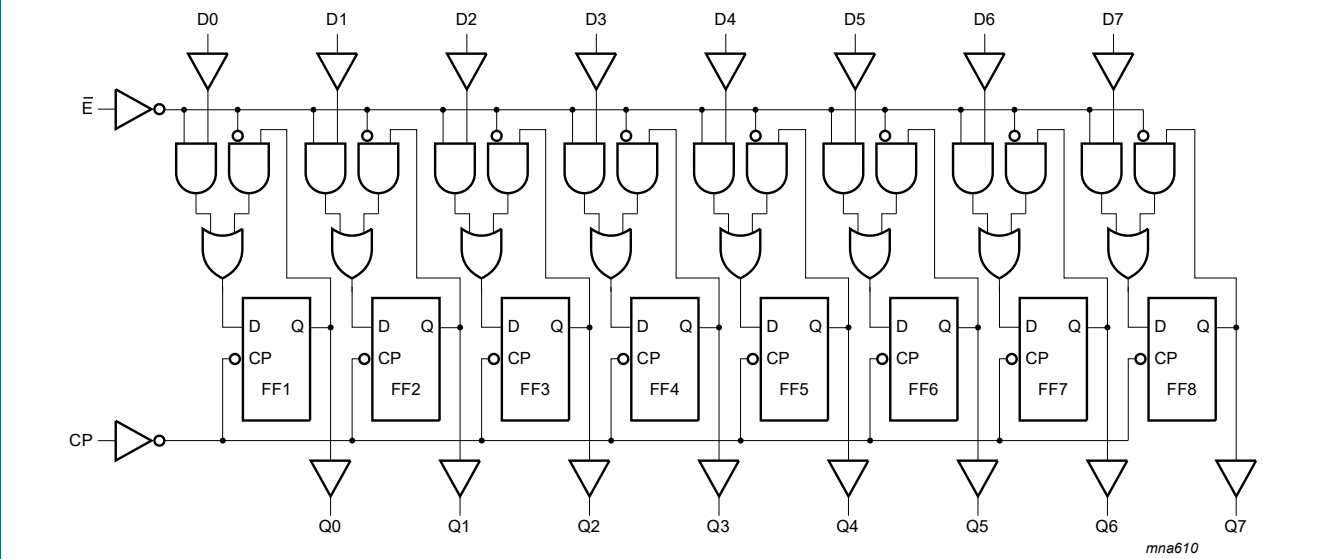
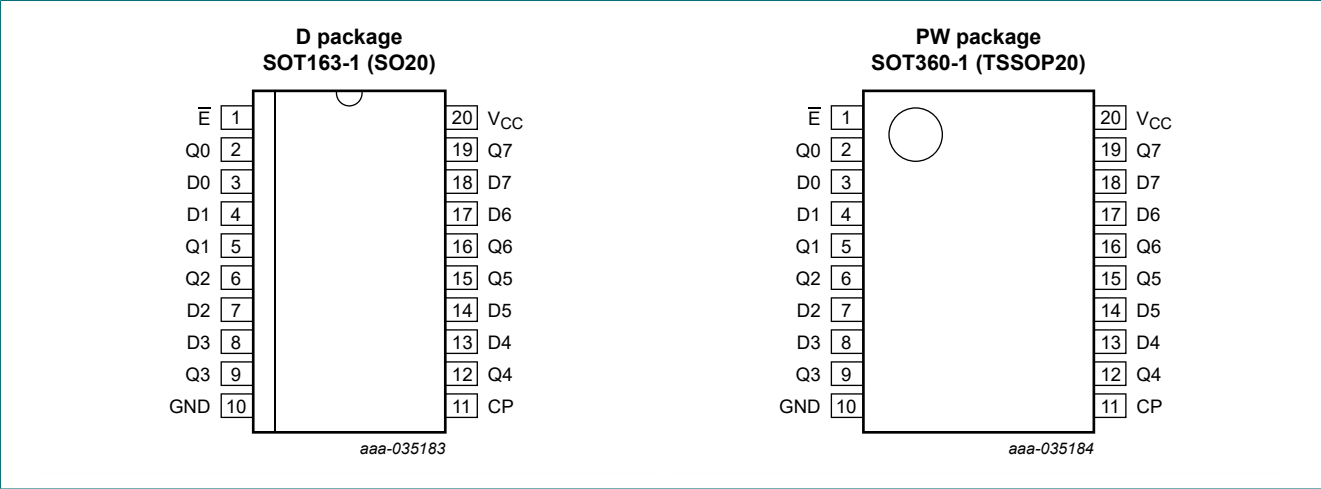


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	1	data enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.*

Operating modes	Inputs			Outputs
	CP	E	Dn	Qn
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC377			74HCT377			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC377										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Octal D-type flip-flop with data enable; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT377										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		E input	-	150	540	-	675	-	735	µA
		CP input	-	50	180	-	225	-	245	µA
		Dn input	-	20	72	-	90	-	98	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

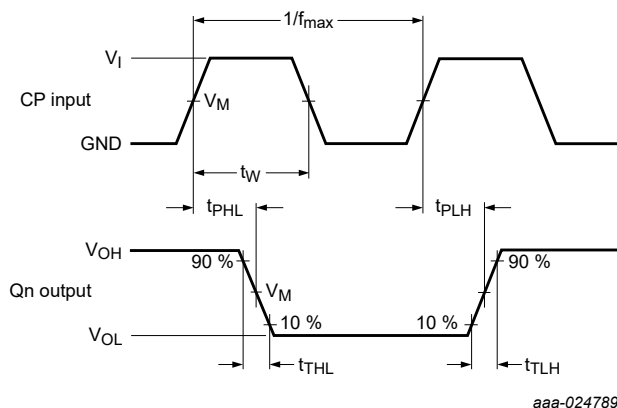
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC377										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	44	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	16	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	-
		V _{CC} = 6.0 V	-	13	27	-	34	-	41	ns
t _t	transition time	Qn output; see Fig. 5 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _W	pulse width	CP input HIGH or LOW; see Fig. 5								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 6								
		V _{CC} = 2.0 V	60	14	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	4	-	13	-	15	-	ns
		E to CP; see Fig. 6								
		V _{CC} = 2.0 V	60	6	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns
t _h	hold time	Dn to CP; see Fig. 6								
		V _{CC} = 2.0 V	3	-8	-	3	-	3	-	ns
		V _{CC} = 4.5 V	3	-3	-	3	-	3	-	ns
		V _{CC} = 6.0 V	3	-2	-	3	-	3	-	ns
		E to CP; see Fig. 6								
		V _{CC} = 2.0 V	4	-3	-	4	-	4	-	ns
		V _{CC} = 4.5 V	4	-1	-	4	-	4	-	ns
		V _{CC} = 6.0 V	4	-1	-	4	-	4	-	ns
f _{max}	maximum frequency	CP input; see Fig. 5								
		V _{CC} = 2.0 V	6	23	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	77	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	83	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	20	-	-	-	-	-	pF

Octal D-type flip-flop with data enable; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT377										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	17	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _t	transition time	Qn output; see Fig. 5 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	CP input; see Fig. 5								
		V _{CC} = 4.5 V	20	8	-	25	-	30	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 6								
		V _{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		$\overline{E}$ to CP; see Fig. 6								
		V _{CC} = 4.5 V	22	12	-	28	-	33	-	ns
t _h	hold time	Dn to CP; see Fig. 6								
		V _{CC} = 4.5 V	2	-4	-	2	-	2	-	ns
		$\overline{E}$ to CP; see Fig. 6								
		V _{CC} = 4.5 V	3	-2	-	3	-	3	-	ns
f _{max}	maximum frequency	CP input; see Fig. 5								
		V _{CC} = 4.5 V	27	48	-	22	-	18	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	53	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V [3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

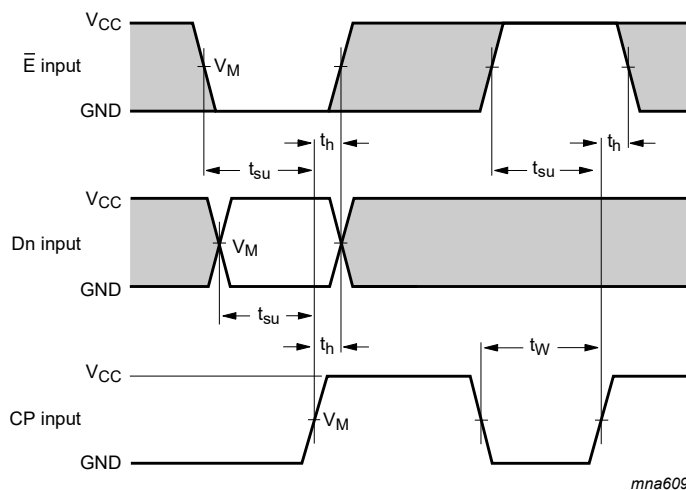
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Data set-up and hold times data input (Dn)

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC377	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT377	3 V	1.3 V	1.3 V

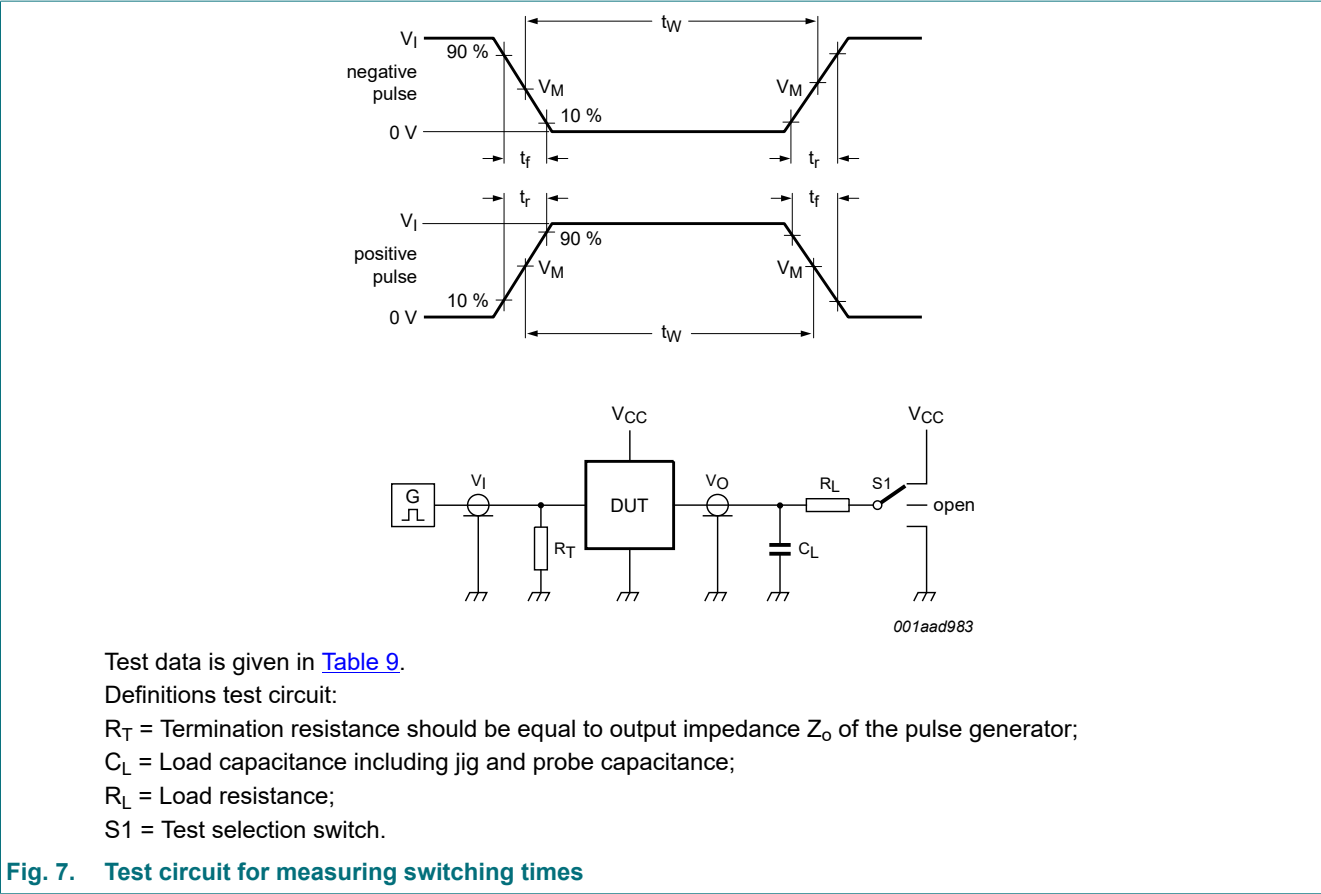


Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC377	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT377	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

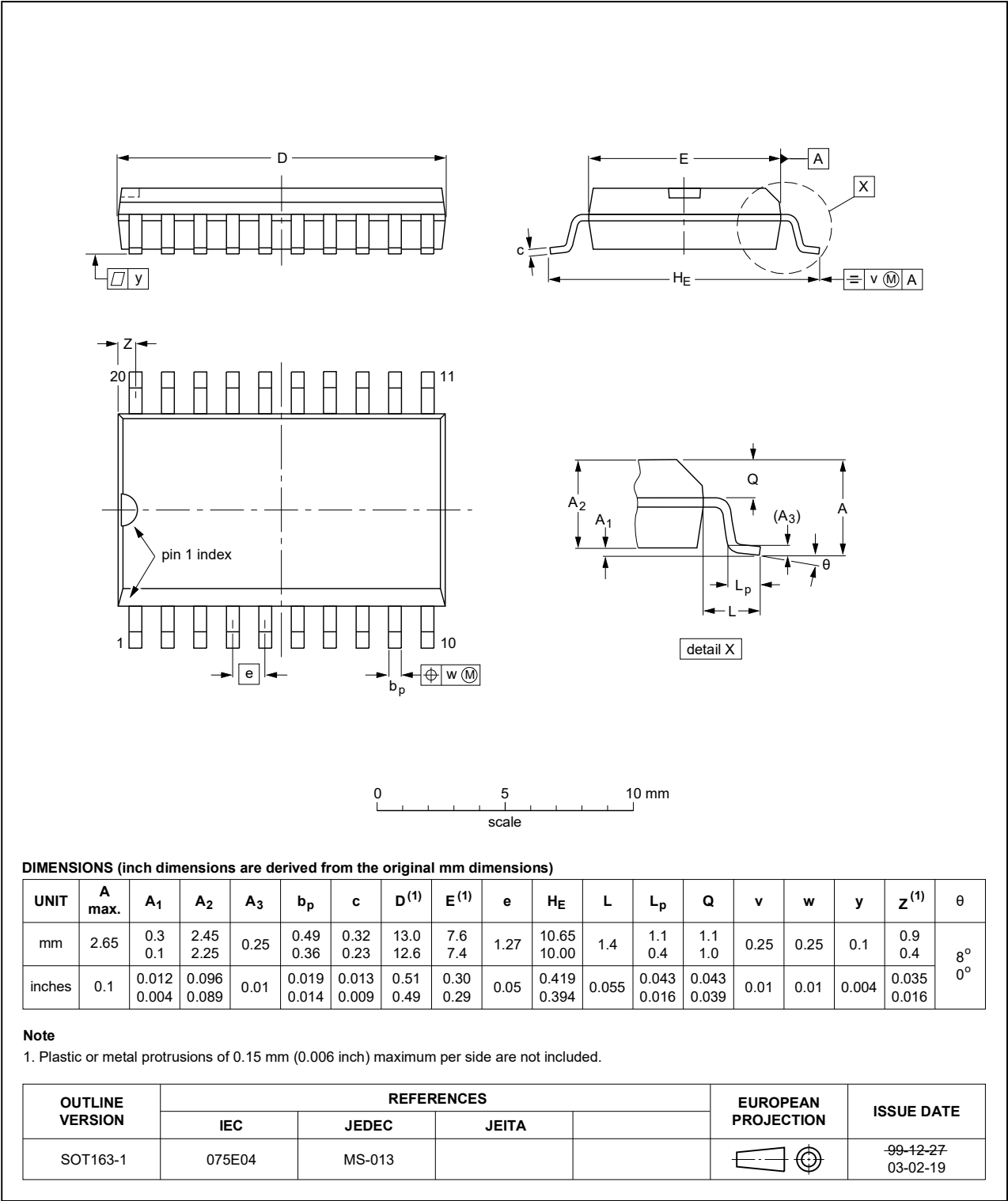


Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

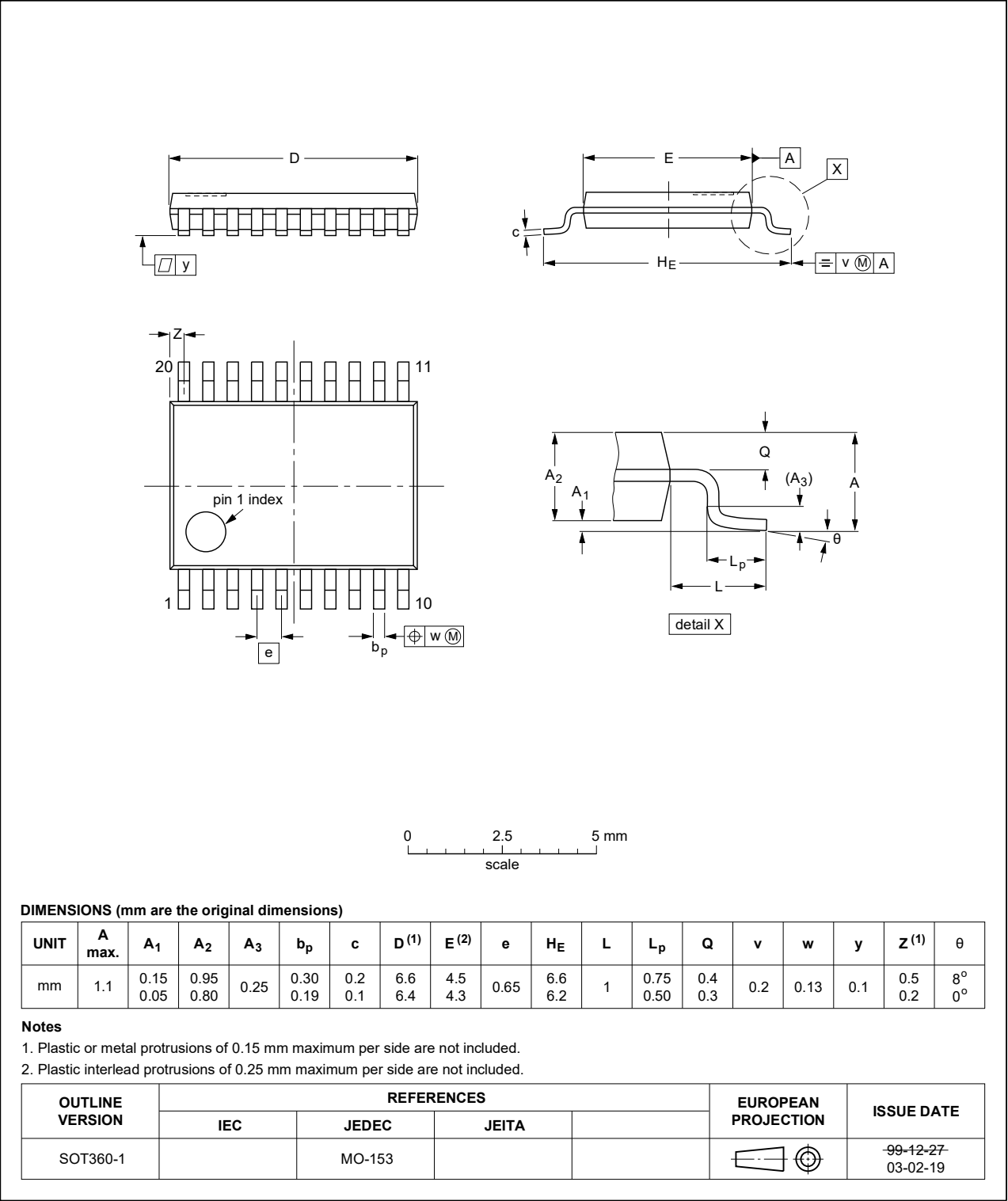


Fig. 9. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT377 v.6	20240805	Product data sheet	-	74HC_HCT377 v.5
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT377 v.5	20210225	Product data sheet	-	74HC_HCT377 v.4
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Section 2 updated. - Section 7: Derating values for P_{tot} total power dissipation updated. - Type numbers 74HC377DB and 74HCT377DB (SOT339-1 / SSOP20) removed.			
74HC_HCT377 v.4	20160224	Product data sheet	-	74HC_HCT377 v.3
Modifications:	Type numbers 74HC377N and 74HCT377N (SOT146-1) removed.			
74HC_HCT377 v.3	20130925	Product data sheet	-	74HC_HCT377_CNV v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT377_CNV v.2	19901227	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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